A NEW RESONANT DIODE-BRIDGE INSERTED BOOST PFC RECTIFIERS FOR POSITIVE AND NEGATIVE VOLTAGE OUTPUTS

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Abstract: *The boost type rectifiers have attracted progressively many applications; the profusion is due to the merits such as the subtle line current distortion and the close to unity power factor (UPF) for almost all the load conditions. The standards such as EN61000-3-2 have been imposing the power factor correction (PFC) in ac-dc power supplies. Apart from the front end PFC, the output voltage regulation, the component count waning, improved power density, gagging the device stresses, curbing the losses, abrogation of electromagnetic interference (EMI) etc. are also exhorted. Different PFC boost converter topologies are reviewed in this paper for their performance. Anew single phase resonant boost converter, a resonant diode-bridge inserted boost PFC rectifier (RDBIBPFCR), is suggested for switching loss minimized operation, and type-II compensator is designed to combat against perturbations (line, load and circuit component variations). The topology enjoys the provision of offering negative output voltage by a minimal alteration. The savvy of the proposed converter is tested in PSIM software and critically compared with three contemporary boost rectifiers (conventional, conventional single ended primary inductor converter (SEPIC) based and pseudo boost rectifiers) at the EN61000-3-2 hamstrung bench mark. The corroboration is performed on the Arduino's flagship board (UNO) colluded prototype arrangement.*

Keywords: *Boost rectifier, Power factor correction (PFC), type-II compensator, resonant diode bridge inserted boost PFC rectifier (RDBIBPFCR), EN61000-3-2 compliance, Line current harmonics.*

Nomenclature

α-Duration of mode 1
β-Duration of mode 2
γ-Duration of mode 3
d_1-Duty cycle
F-f_s/f_r is the normalized switching frequency
f_r (ω_r)-Base frequency
k-Dimensionless conduction parameter;

$$K=\frac{2L_1}{R_L T_S}$$

M-Voltage conversion ratio
T_s-Switching period
V_m-Peak of the input ac-line voltage
V_o-Output voltage

1. Introduction

The off-line power supplies very commonly used in personal computers, telecommunication, medical etc. applications feature a power factor corrected/correction (PFC) front end rectifier followed with a boost dc-dc converter [1]. Conventional diode rectifiers while used in front end engender harmonics and endure in low power factor operation. The prime reason for poor power factor in the line side is being waveform distortion besides load reactance [2]. The line current distortion evokes line harmonics, which have adverse effects as enlisted below [3]-[4].

1. Perilous neutral current values in three-phase power systems;
2. Thermal stress and life span reduction in induction machines;
3. Distortion in line voltage waveform;
4. Averting from full utilization of the installed service by upping the root mean square (rms) line current;
5. Additional losses
6. Treacherous currents in PFC capacitors and
7. Malfunctioning of switch gear and protection arrangements.

The conventional rectifiers are harmonic polluters in the distribution systems. Colossal international standards exist today that explicitly restrain the magnitudes of current harmonics, in both high power loads such as electric drives, and low power appliances such as electronic ballasts of fluorescent lamps and power supplies for office equipments [5]-[6]. The undesirable effects of harmonics distortion and low power factor are discussed and documented. Both of these issues are influenced by the converter topology, pulse

width modulation (PWM) employed, input/output filters etc.

In switched mode power conversions, the power factor (PF) is the ratio of the average power to the apparent power supplied to the load from the AC source. Considering an ideal voltage source, the PF can be articulated as the product of the distortion power factor (K_d) and the displacement power factor (K_θ), as given in (1). The K_d is the ratio of the rms current (I_{rms1}) to the total rms current (I_{rms}). The K_θ is the cosine of the displacement angle between the fundamental component of input current and the input voltage [7]. The presence of harmonics, hence total harmonic distortion (THD) sways the PF as evidenced in Fig.1, which is accomplished from the theoretical study performed on a conventional full wave rectifier. The reactive current instigates the voltage distortion in the ac supply. That's why the challenging part is to cope the rectification to have near unity power factor (UPF) functioning. Furthermore, a flawlessly sinusoidal current may have a pitiable power factor even though while feeding pure resistive load if there is bleak distortion in the current waveform. From (2) it is apparent that a 10% THD corresponds to a PF of approximately 0.995. Thus it is clear that specifying limits for each of the harmonics will help in the control of input current "contamination" better, both from the standpoint of minimizing the circulating currents and restraining the interference with other equipment. The process of shaping the input current is power factor correction and the prime aim is finding the effectiveness towards complying with international regulations.

$$\mathbf{PF} = \mathbf{K}_{\mathrm{d}}\mathbf{K}_{\theta} \tag{1}$$

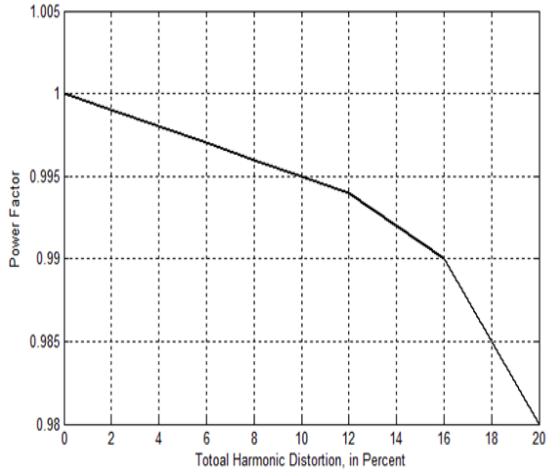


Fig. 1. Dependency of PF on THD

$$\mathrm{PF} = \frac{1}{\sqrt{1+\left(\frac{\mathrm{THD}(\%)}{100}\right)^2}} \tag{2}$$

Power supplies with active power factor correction (APFC) techniques are becoming necessary for many types of electronic equipment especially for telecommunication and computer industries [8]-[9]. The APFC methods aim to improve the power factor and diminish the THD of the power converters, where change in the topology is being the crux tenet. However, most of them suffer following drawbacks: 1) high component count; 2) components are not fully utilized by over whole ac line and 3) ripple in the dc outpu voltage.

Various ac-dc converters have also been attempted for PFC where the mainstay is placing a boost converter between a diode rectifier bridge and a dc-bus capacitor [10]-[14]. The conformist ac-to-dc rectifier topologies involving non-linear devices (diode, thyristor etc based bridges) cause bleak input current distortion and reactive power. Apart from these issues, with the hard switching these converter topologies exhibit high switching losses, hamper on switching frequency, increased device stress and are bulky in size [16]. The option of increasing the count of voltage sources by using a split-wound coupled inductor has been examined in a multi-level single-phase boost rectifier [16]. Instead of cancelling the current ripples by the high frequency ripple (arrived by interleaving), the proposed strategy has used high frequency multi-level PWM voltage waveforms. A host of single phase diode rectifiers adept to shape near sinusoidal current waveforms at UPF with high efficiency and waned voltage stress across the switches has been suggested [17]. The single switch operated with zero current switching (ZCS) for turning on and zero voltage switching (ZVS) as well as ZCS for turning off, uses the coupled inductors for these resonances. A soft-switched partial resonant link ac-dc converter circuit with four active switches, which eliminates the requirement of a four-quadrant ac switch, has been studied. The diminished active switches count and the high switching frequency offer the enhanced performance, and substantial reduction in size, weight and cost. Also the combination of SiC-MOSFET and Si-PiN Diode led a high efficiency operation [18]. An isolated three phase single-stage ac-dc converter has been coined for aircraft application [19]. The suggested converter uses the matrix (3x1) topology, space vector modulation (SVM) based switching scheme, a current doubler rectifier (CDR) and an active soft-switched lossless snubber circuit. A ZCS huddled resonant boost converter employing two auxiliary switches for achieving the APFC has been devised [20]. An innovative soft-switched, current-driven full-bridge converter has been developed in which a simple snubber has been involved in order to get ZVS for all the main switches [21]. The crux advantage of the soft-switching realization is independency of the load. The unremitting assessment on the literatures confirms that there exists a leeway to innovate the

boost rectifier structure/system towards PFC, switching loss minimization and regulate the output voltage against perturbations. The work suggests a single phase resonant boost converter and also develops a type-II compensator for regulating the output voltage. The performance of the developed a resonant diode-bridge inserted boost PFC rectifier (RDBIBPFCR) is compared with the competent rectifiers in PSIM 9.0.3 platform. The practical substantiation is done in the designed converter system using Arduino UNO board involving ATmega328 processor in the Arduino IDE 1.0.6 software environment.

2. Line Current Harmonics and Trend in PFC

2.1. Classifications of load and Harmonic Standards

All electrical/electronic equipments which are tied to the distribution systems must comply with EN 61000-3-2. Passive and active harmonic line current reduction solutions can be used to fulfil the limits of the standard which greatly influences the design of all power supplies [22]. There are four dissimilar classes in the EN 61000-3-2 that have different limit values and their harmonic limits are tabulated in Table 1. The regulation on even harmonics is a worthy guidance for design engineers.

Class A: Balanced three phase equipment, household appliances apart from equipment recognized as class D, tools, dimmers for incandescent lamps, audio equipment, excluding portable tools, and all other equipment, except that fixed in one of the subsequent classes.

Class B: Arc welding equipment, portable machine tools, which are not professional equipment

Class C: Lighting equipment.

Class D: Personal computers (PCs), PC monitors, radio, or television (TV) receivers.

Table 1
Harmonic current limit for Class A and Class D equipments (EN 61000-3-2)

Harmonic order (n)	Class A	Class D	
	Absolute limit (No Power limit)	Absolute limit (No Power limit)	Absolute limit (600W ≥P>75W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	00.21		
15 ≤n≤ 39 (Class A)	Use following equations		
13 ≤ n ≤ 39 (Class D)	2.25/n	3.85/n2.25/n	
Even Harmonics			
2	1.08	Not Applicable	
4	0.43		
6	0.30		
8 ≤ n ≤ 40 (Class A)	1.84/n		

2.2 Trend in PFC

Line current harmonic reduction can be achieved by using different techniques. The most common used techniques for harmonic current reduction are line filters, using passive components, and active electronic circuitry. Harmonic line current reduction using passive components (inductors and capacitors) introduces high impedance for the harmonics thus smoothing the input current to electronic equipment. Harmonic line current reduction using active electronic circuitry is shaping the input current and paves a sinusoidal shape in phase with the line voltage. The corresponding electronic circuitry is often called PFC circuitry, though PFC is not an appropriate wording but has become synonymous for harmonic line current diminution.

The principal behaviours of the ac line current with and without harmonic current reduction are very useful for understanding. Fig.2 (a) shows the line voltage and current waveforms of a typical single-phase rectifier with any harmonic suppression mechanism. Without any harmonic reduction circuitry the input current achieves very high limits as the current is only limited by the small input impedance (filter and cabling) of the power supply. Adding additional inductances (passive solution) reduce the input current as well as its harmonic content (Fig.2(b)). Best harmonic current reduction is achieved by APFC (Fig.2(c)).

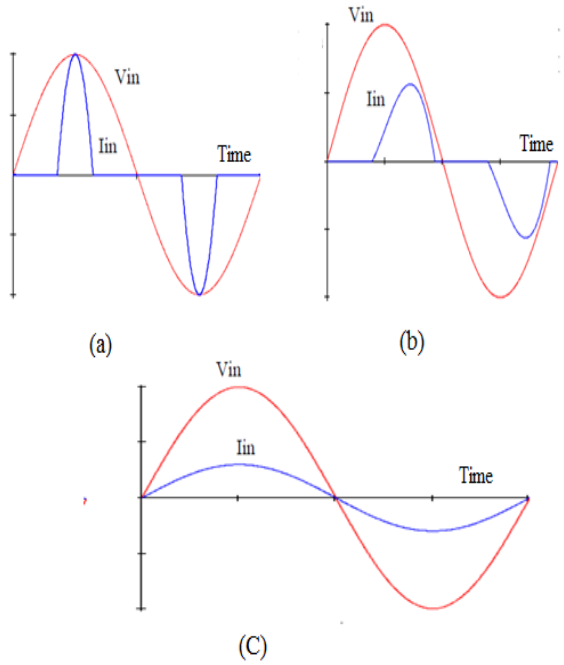


Fig. 2. Input voltage (V_{in}) and current (I_{in}) (a) without harmonic line current reduction, (b) with passive harmonic current reduction (c) with active harmonic current reduction

High-frequency APFC circuit are preferred for PFC. Any dc-dc converters can be used for this purpose, if a suitable control method is used to shape its input current or if it has inherent PFC properties. Converting dc voltage to t proper levels from a single energy source that might be depleting, like in battery applications, requires employment of energy storage elements (inductors) with associated power electronics devices. When switched ON-OFF at a certain rate, stored energy gets released to the load at the proper time to maintain the desired voltage level. PWM techniques are most popular in this application. Feedback loop methodologies are an integral part of dc-dc converters to regulate the load voltage, compensating for load variations and irregularities in the source voltage. Current and voltage ripples, and high frequency harmonic distortion are common by products of switching techniques. Many circuits and control methods using switched-mode topologies have been developed to comply with standard. The APFCs employ any one dc-dc converter following the front end diode rectifier. For instance buck converter based APFC cascades the buck converter after the diode rectifier. Similarly boost, buck-boost, Cuk, single ended primary inductor (SEPIC), ZETA etc. converters have also been involved [23]-[26]. Recently many attempts have been noticed with component reduced structure where the stage-I (diode rectifier) and stage-II (DC-DC converter) are integrated to form a component count waned single stage structure. Exploitation of resonant switching helps in gagging the switching losses to a great extends [28]-[30].

3. Proposed Resonant Diode-bridge Inserted Boost PFC Rectifier

The suggested RDBIBPFCR, pictured in Fig.3 (positive output) and Fig.4 (negative output), is incised to operate in discontinuous-conduction mode (DCM) in the switch turn-on interval and resonant mode during the switch turnoff intervals. Consequently, the switch current stress is akin to the conventional DCM PFC converter, while the switch voltage stress is high. Furthermore, the single switch (Q) based topology radically abridges the control circuitry. On the other hand, an isolated gate drive is necessitated for the power switch Q. The diode bridge (D_{s1} to D_{s4}) and Q form the bidirectional switch.

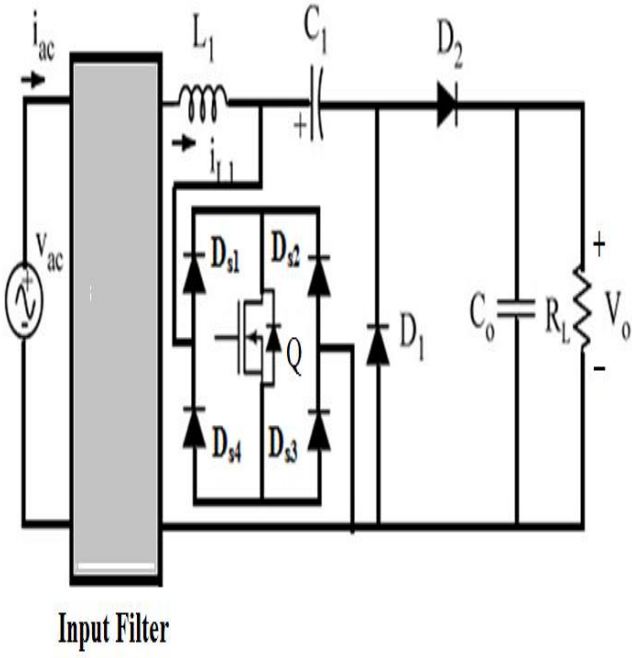


Fig. 3. RDBIBPFCR with positive polarity output

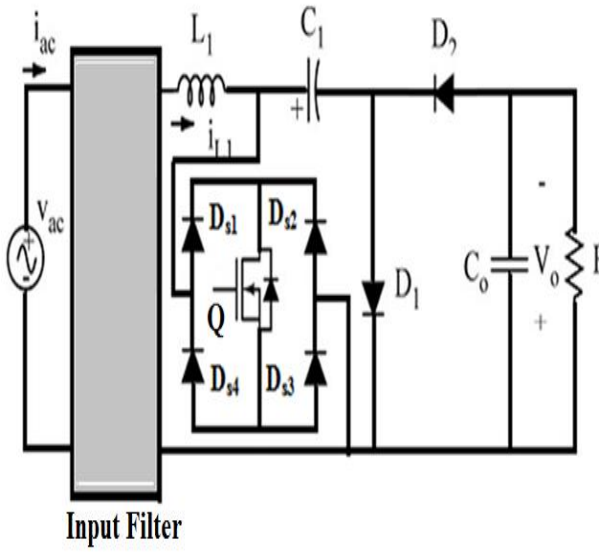
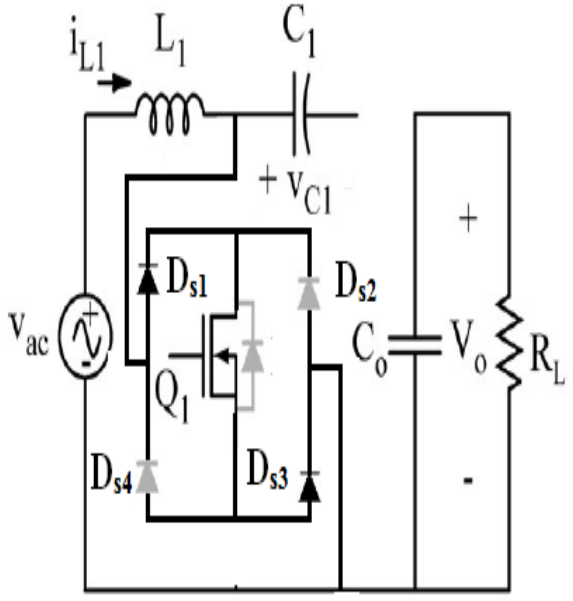
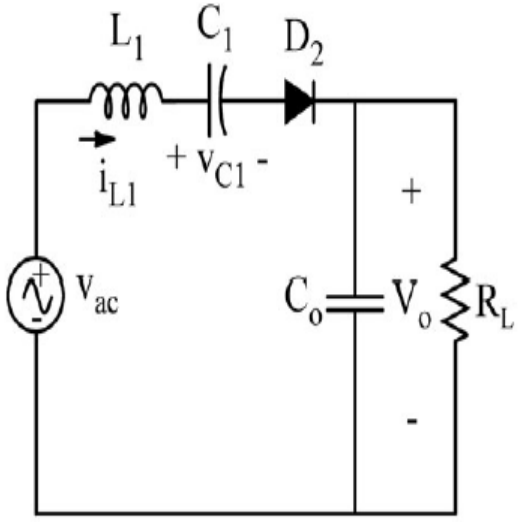


Fig. 4. RDBIBPFCR with negative polarity output

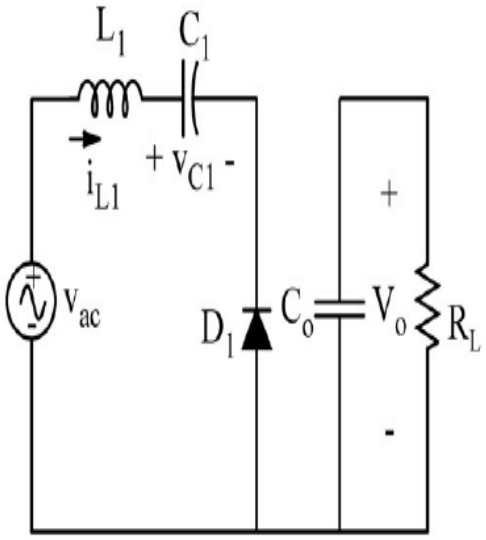
The assumptions, namely, operation under steady-state condition, pure sinusoidal input voltage, ideal (lossless) components, the higher switching frequency (f_s) than power line frequency (f_s), and the large enough output capacitor (C_o) to keep the output voltage constant. With the above postulations, the circuit operations in a switching period, T_s for the positive ac input cycle can be divided into four different modes. The equivalent circuits of each mode and the key waveforms during one switching period are shown for the positive output RDBIBPFCR (PORDBIBPFCR) respectively in Fig.5 and Fig.6.



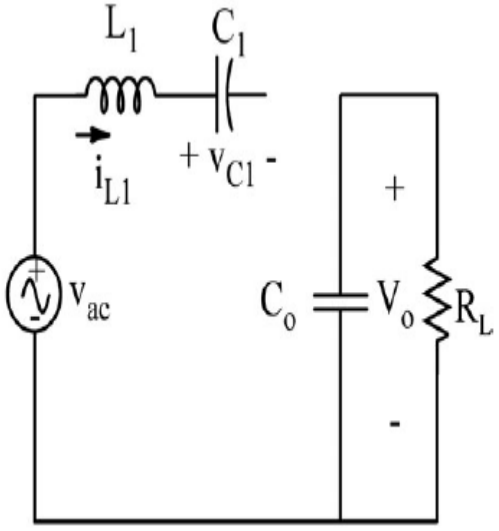
(a) Mode 1



(c) Mode 2



(c) Mode 3



(d) Mode 4

Fig. 5. Mode diagram

It is evidenced that during the negative half-cycle, the load is charged in the positive portion of the resonant cycle. Besides, the capacitor voltage, V_{C1} during the negative half-cycle is not symmetric with the positive half cycle. This is ascribed to the actuality that the V_{C1} amplitude is the summation of the output and input line voltages during the negative half-cycle while it is a difference during the positive one.

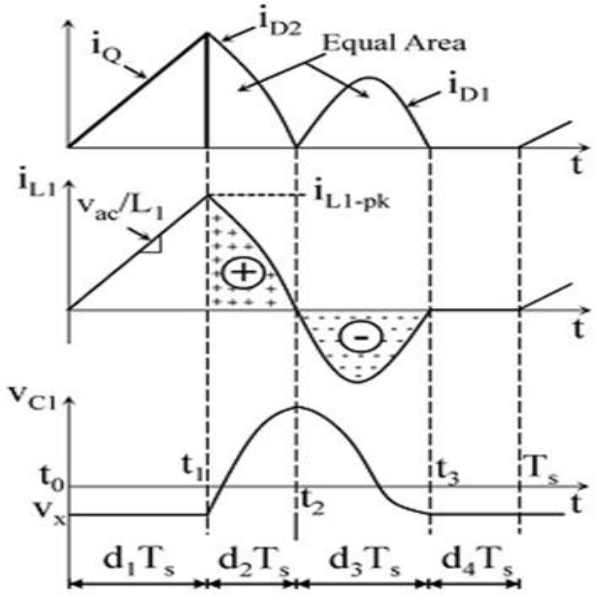


Fig. 6. Theoretical waveforms of PORDBIBPFCR

4. Design Procedure

In this section, a procedure for the RDBIBPFCR design is presented for a specific operating point. The uppermost values of α and β occurs at the peak input voltage. It shall be noted that due to the resonant, nonlinear behaviour of the rectifier, an iterative design procedure can only be persuaded. The design procedure is presented for the following power stage specifications: V_{ac}=85V(rms), V_o=240V, P_{out}=115W, and f_s=50kHz. From the aforementioned data, and assuming that the efficiency is 100% (lossless), the values of the circuit components are calculated as follows [30]:

$$M=\frac{v_o}{v_m}=\frac{240}{\sqrt{2}*85}=2$$

$$L_1=\frac{R_L T_S}{4}\left(\frac{F}{\pi}\right)^2=\frac{500*\left(\frac{1}{50e^3}\right)}{4}\left[\frac{0.8}{\pi}\right]^2=163\mu H$$

$$C_1=\frac{1}{L_1(2\pi f_r)^2}=\frac{1}{163e^{-6}(2\pi*50e^3)^2}=65nF$$

$$k=\frac{2L_1}{R_L T_S}=\frac{2*163\mu H}{500*\left(\frac{1}{50e^3}\right)}=0.0324$$

$$d_1=M\sqrt{2k}=2\sqrt{2*0.0324}=0.45$$

$$\alpha+\beta+\gamma\le\frac{2\pi}{F}$$

$$\omega_r d_1 T_S+\sin^{-1}\left(\frac{4jQ-pk}{4+j^2Q-pk}\right)+\pi=7.61\le\frac{2\pi}{F}=7.84$$

Fig.7 presents the formulaic steps involved in the computation of L_1, C_1 and duty cycle for any F value. Table 2 lists the designed strictures for different k values.

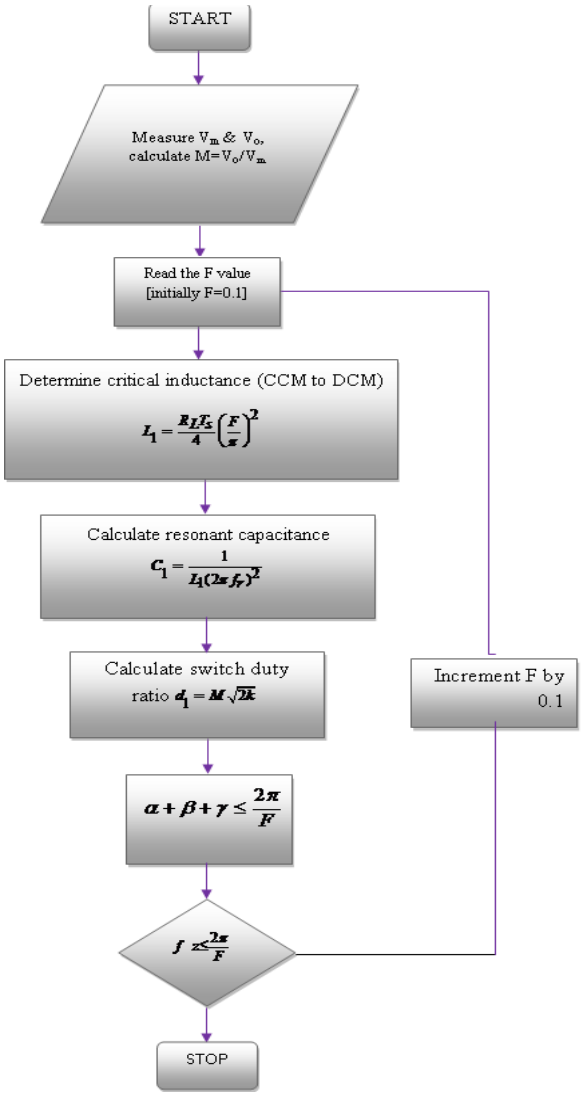


Fig. 7. Calculate the normalized Switching Frequency

Table 2
Designed strictures for different normalized switching frequency values

F	L_1 (μH)	C_2 μF	Duty ratio
0.1	2.56	4	0.06
0.2	10.1	1	0.04
0.3	22.77	0.4	0.19
0.4	40.5	0.2	0.25
0.5	63.3	0.16	0.31
0.6	91.1	0.11	0.38
0.7	0.50	0.08	0.42
0.8	162.5	0.062	0.45
0.9	253.5	0.049	0.49

5. Designing compensator using PSIM

Apart from the PFC in the front end regulation of output voltage also mandatory for most of the applications [31-[33]. Design of compensator using PSIM is detailed beneath. The first step after the plant selection is fixing the sensor, depending on the variable being controlled, SmartCtrl will display the appropriate sensor selection as described in Fig.8.

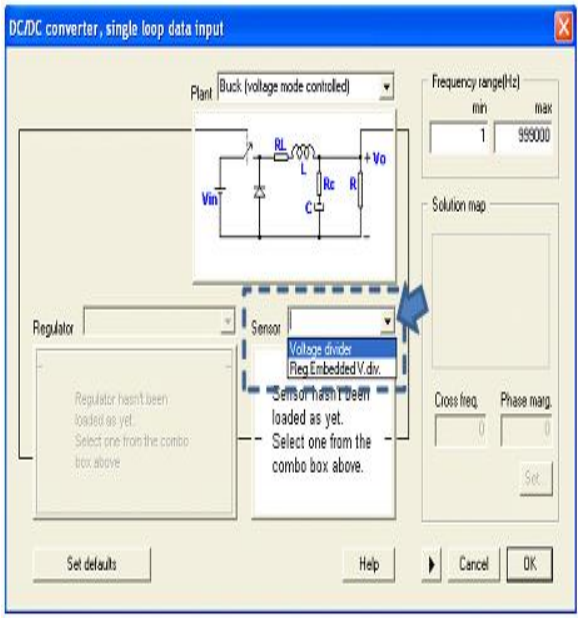


Fig. 8. Selection of sensor

In the case of a voltage divider, the reference voltage must be entered. The SmartCtrl will automatically calculate the sensor gain. In this example, the reference voltage is set at 2.5V. The figure below, Fig.9, shows the sensor input data window. Note that the design will be carried out using this gain, and the resistor values to implement the voltage divider will be listed by Smart Ctrl together with the regulator component values. Select the regulator type from the regulator drop down menu as shown Fig.10. The type of regulator depends on the plant controlled. In this example, since the plant is a second order system, the best choice is a Type 2 regulator in order to obtain the proper phase margin and enough bandwidth.

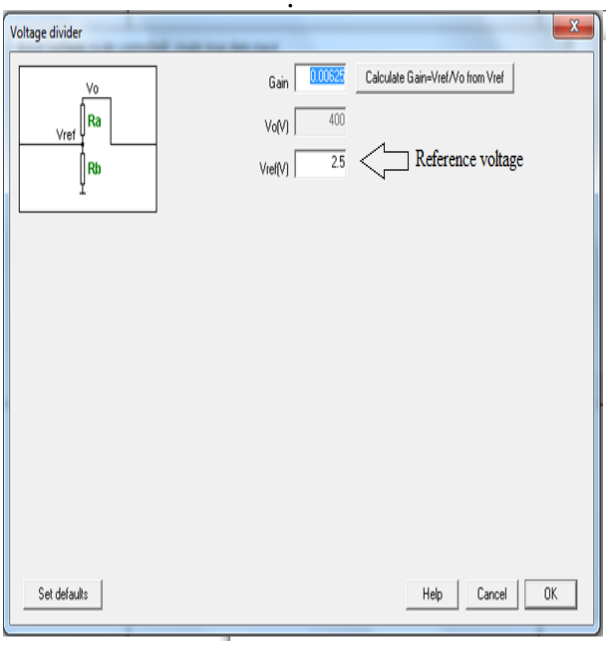


Fig. 9. Sensor input data window

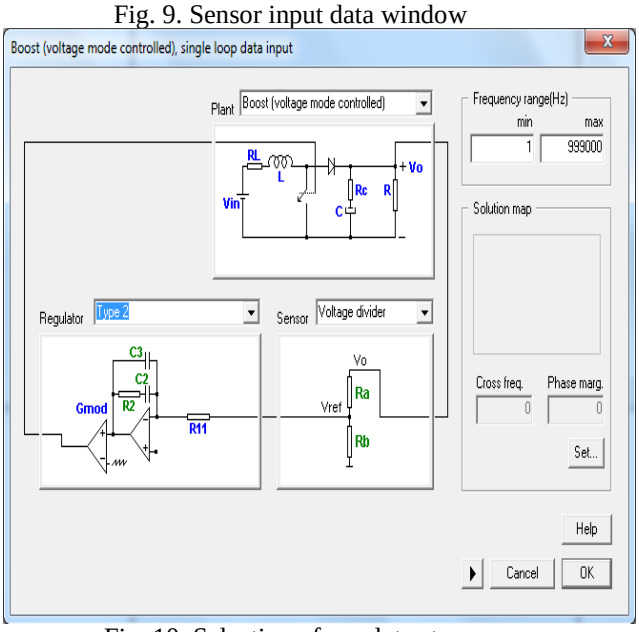


Fig. 10. Selection of regulator type

After selecting the Type 2 regulator, enter the parameters as shown in Fig.11, where Gmod is the modulator gain. Select the crossover frequency and the phase margin. SmartCtrl provides a guideline and an easy way of selecting the crossover frequency (sometimes also referred to as the bandwidth) and the phase margin through the Solution Map. Click on the Set button, and the Solution Map will be shown as below. The x-axis of the Solution Map is the

crossover frequency and the y-axis is the phase margin. Based on the converter parameters and the type of regulator selected, SmartCtrl will generate a safe design area as shown in the white area of the Solution Map (Fig.11). Any selection of the crossover frequency and the phase margin within this white shaded area will lead to a stable solution.

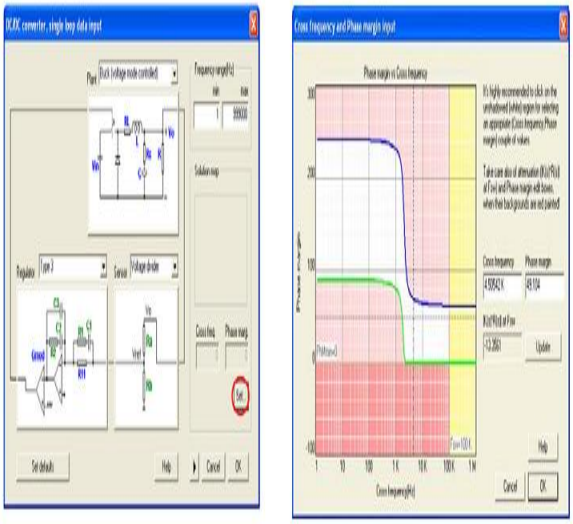


Fig. 11. Entering the parameters

One can select the desired crossover frequency and the phase margin by entering the values in the edit boxes, and click on the Update button, or left click directly on the Solution Map. The selected design appears as a red point in the Solution Map. For a particular design, the attenuation given by the sensor and the regulator at the switching frequency is calculated and displayed in the edit box $|K(s)*R(s)|$ at f_s. Note that if there is not enough attenuation at the switching frequency, the system will likely oscillate in the high frequency region. Also, if a design is not proper, the edit boxes will change to the red colour to warn the designer to review the design.

In general, a crossover frequency of 1/10 of the switching frequency and a phase margin of 45 to 60 degrees are the good initial guess. Click OK to continue. The solutions map will be shown on the right side of the input data window, as shown below in Fig.12. Now click OK to confirm the design, and the program will automatically show the performance of the system in terms of the Bode plots , polar plot, transient response etc. Now, the control loop analysis and optimization may be performed. Once the crossover frequency and the phase margin are selected, the regulator parameters will be calculated, and the control loop performance can be evaluated.

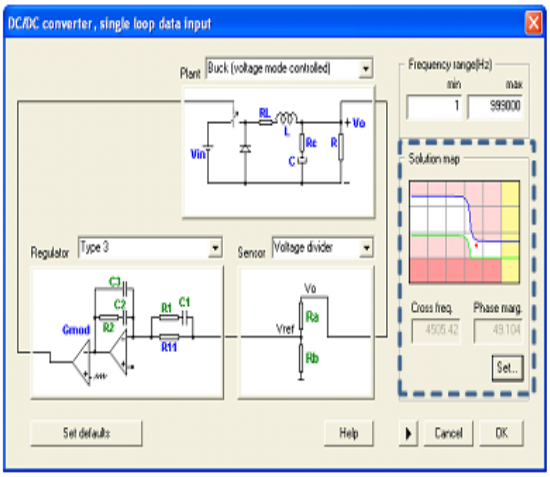


Fig. 12. Solution Map for typical design

Smart Ctrl provides a very intuitive and straightforward way of examining the control loop performance through Bode plots, the polar plot, and transient time-domain responses, as demonstrated in the Fig.13. From the View menu, or from the toolbar on the right, the display for the Bode plots of the plant, the regulator, the open-loop and closed-loop transfer functions, as well as the input/output step response and the reference step response etc can be selected. Depending on the regulator type, various methods are provided to calculate the regulator parameters.

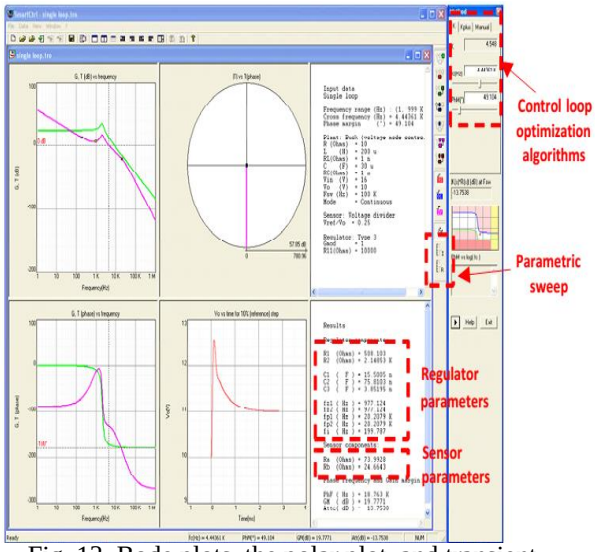


Fig. 13. Bode plots, the polar plot, and transient time-domain responses

The final step is validating the regulator design. SmartCtrl provides the component values for the sensor and the regulator. One can export the regulator circuit and parameters by selecting File > Export > Regulator > To PSIM (schematic) (or clicking on the icon Export to PSIM (schematic)), and perform a time domain

transient simulation in PSIM to validate the design.

6. Simulation Study

The simulation study of the developed converter is performed with specifications enlisted in Table 3.

Table 3
Specifications of the designed PORDBIBPFCR

Tank inductor	100µ H
Tank capacitor	65nF
Filter inductor	1mH
Filter capacitor	1µF
Output filter	470µF
Active switches	STY60NM60: 600V, 60A & R_{DS-ON} =50mΩ
Diodes D_1 and D_2	STTH2R06Q: 600V, 2A V_F=0.7V

The Fig.14 proves that input current is in phase with the supply voltage. Inductor current and capacitor voltage waveforms are revealed in Fig.15 while there enlarged view is depicted in Fig.16. Switch voltage and current are represented in Fig.17. The waveforms (voltage across and current through) associated with the diodes D_1 and D_2 are graphed in Fig.18 and Fig.19 respectively. The typical output voltage is shown in Fig.20.

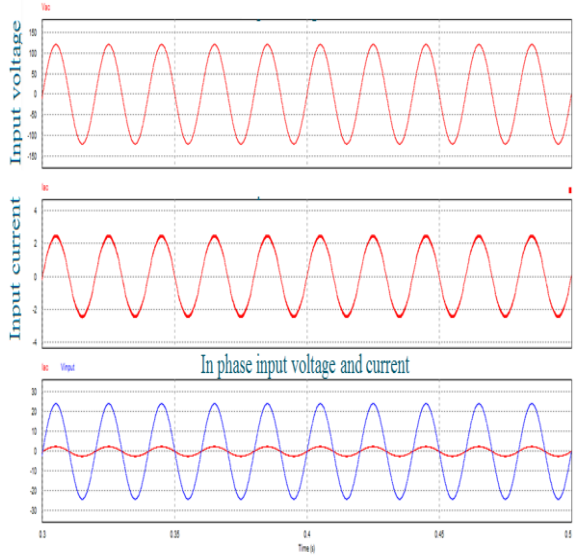


Fig. 14. Input voltage, input current and in-phase input current and voltage

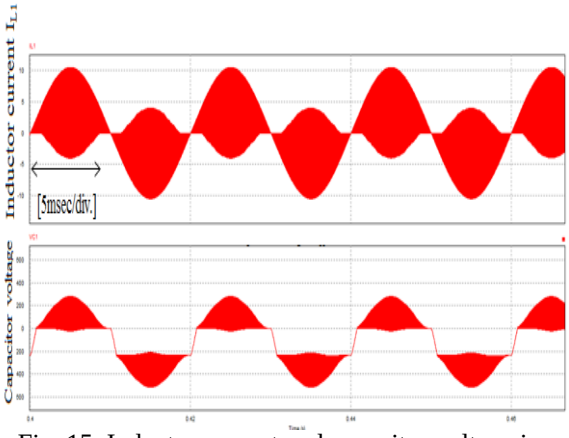


Fig. 15. Inductor current and capacitor voltage in [5msec/div.]

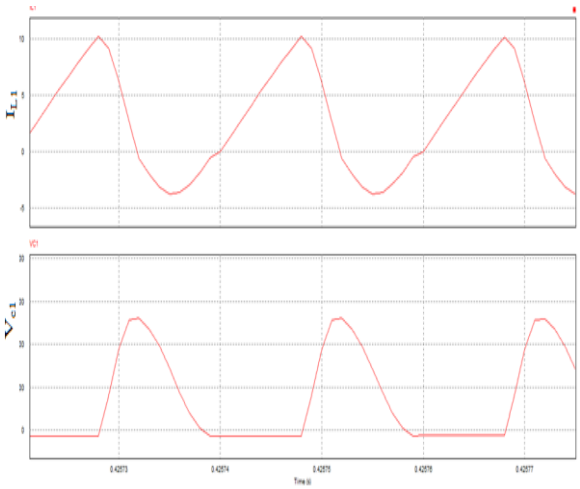


Fig. 16. Inductor current and capacitor voltage in [5µsec/div.]

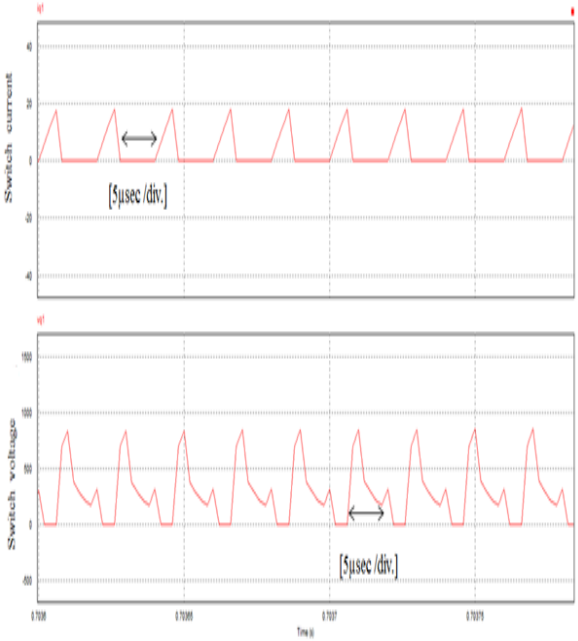


Fig. 17. Switch current and voltage

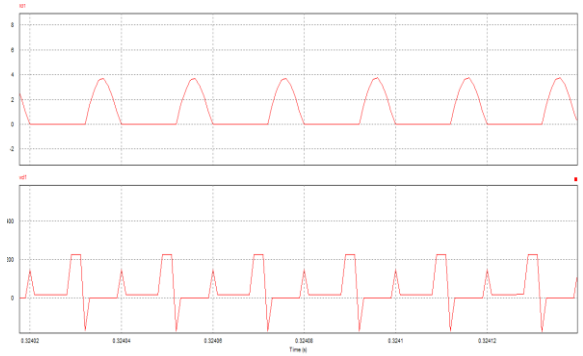


Fig. 18. Diode D_1 voltage and current

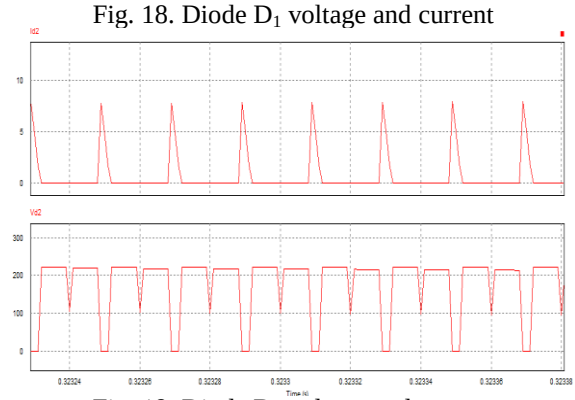


Fig. 19. Diode D_2 voltage and current

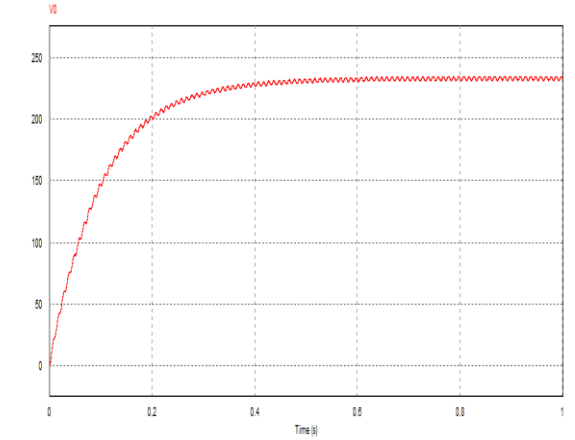


Fig. 20. Output voltage

The combating efforts of the designed Type-II compensator are studied for various perturbations. The response for the step change in the line voltage from 85V to 110V at 1second is captured in Fig.21. Similar study for the step changes in load from 500Ω to 600Ω at 1s is recorded in Fig.22. The step change in the reference is analysed in Fig.23. Table 4 provides the ccomparison between different boost PFC rectifiers with the hamstrung bench mark EN61000-3-2 Class D harmonic limit**s.** The boost rectifiers namely, conventional boost rectifier, SEPIC rectifier, and recent pseudo boost rectifier [30] are simulated in PSIM atmosphere and considered for comparison. The results reveal that the developed RDBIBPFCR produces lesser harmonics compared to its counterparts.

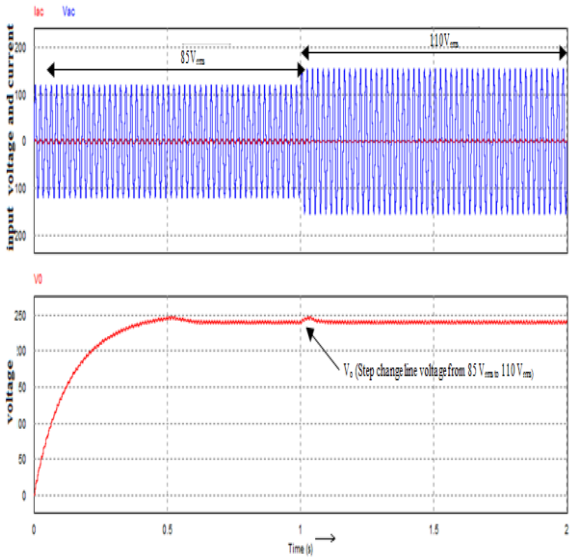


Fig. 21. Response of output voltage for step changes in line voltage- 85V to 110V at 1s

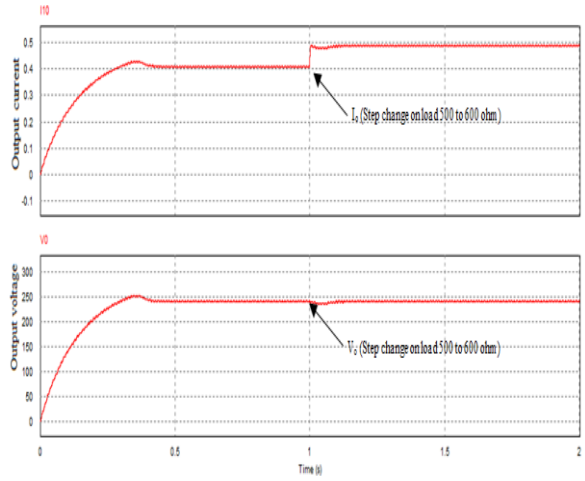


Fig. 22. Response of output voltage for step changes in load-500 to 600 ohm at 1s

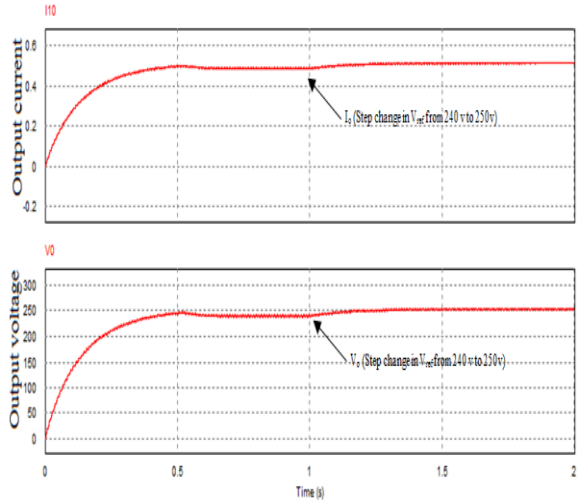


Fig. 23. Response of output voltage when reference value takes a step changes from 240 to 250 V at time 1sec

Table 4
Comparison of different PFC rectifiers at EN61000-3-2 Class D harmonic limits

n	Absolute limit (A)	Conventional boost rectifier	SEPIC rectifier	Recent pseudo boost rectifier [30]	RDBIBPFCR
3	2.30	1.8	1.6	0.15	0.15
5	1.14	0.9	0.8	0.09	0.09
7	0.77	0.6	0.55	0.07	0.07
9	0.40	0.3	0.26	0.05	0.05
11	0.33	0.2	0.15	0.01	0.01

7. Experimental Corroboration

The results obtained from the simulation study are substantiated by the experimental investigation. The prototype RDBIBPFCR is developed for the specifications listed in Table 3. Input voltage and current are provided in Fig.24 and Fig.25 shows the harmonic spectrum of input current. Fig.26 presents the inductor current and voltage and their enlarged view is given in Fig.27. Diode current and voltage waveforms are shown in Fig.28 (D_1) and Fig.29 (D_2). Output voltage responses to step changes in input voltage and the reference are depicted respectively in Fig.30 and Fig.31. The photograph of the fabricated hardware is given in Fig.32.

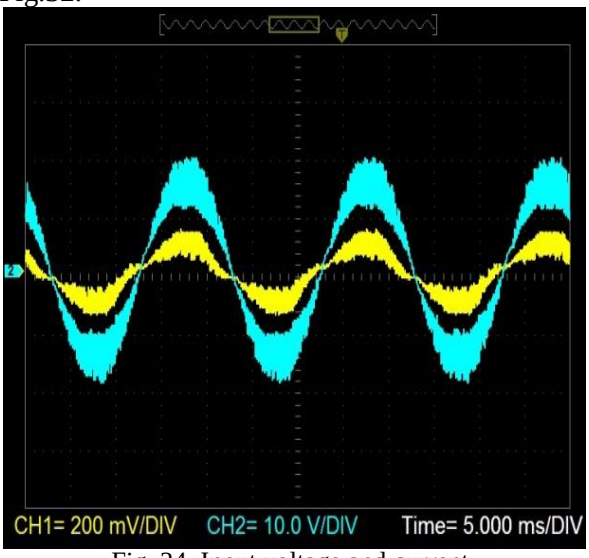


Fig. 24. Input voltage and current

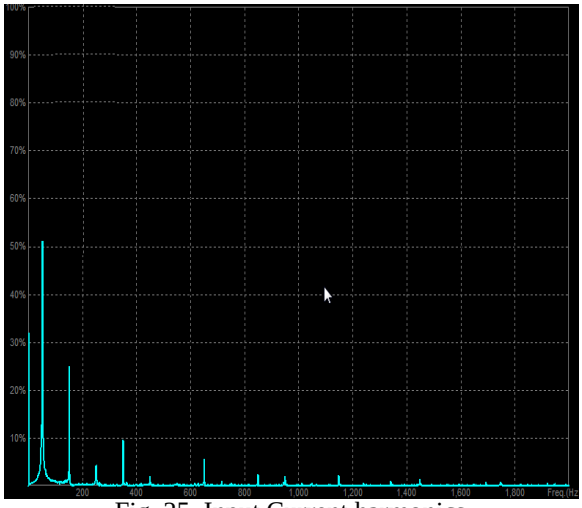


Fig. 25. Input Current harmonics

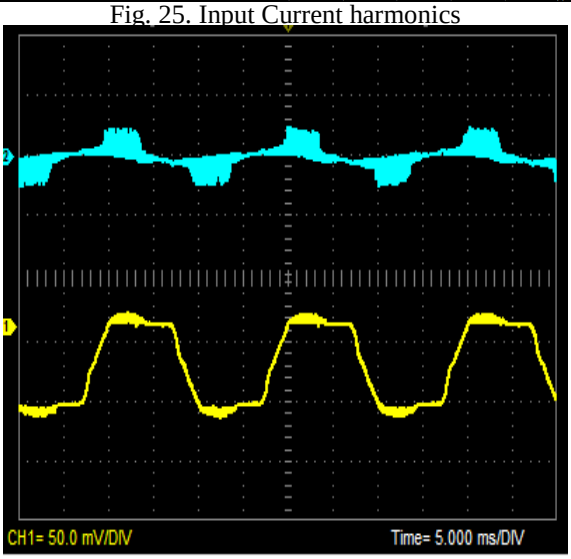


Fig. 26. Inductor current and voltage (5 ms/Div)

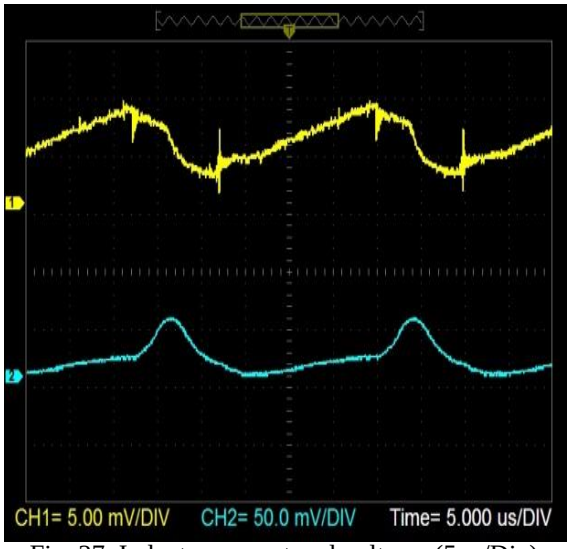


Fig. 27. Inductor current and voltage (5μs/Div)

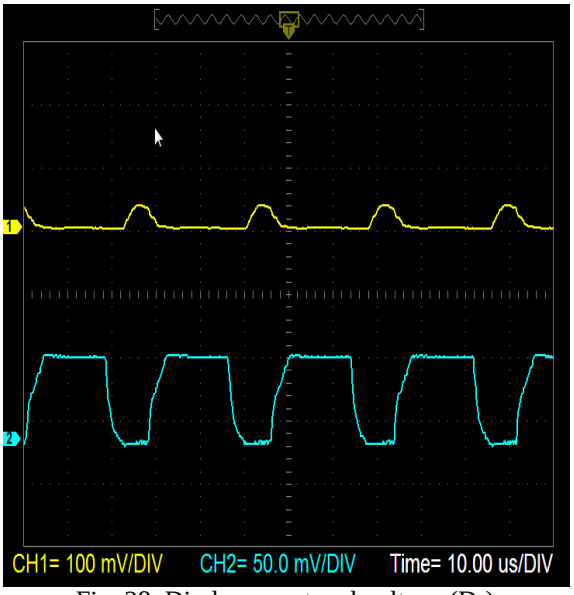


Fig. 28. Diode current and voltage (D_1)

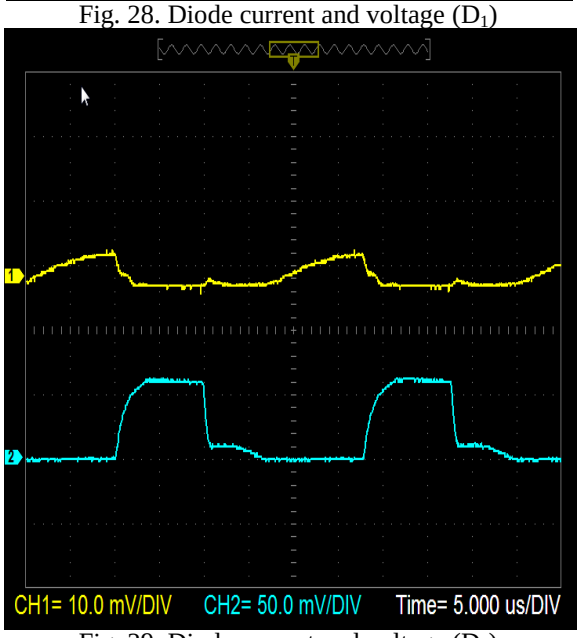


Fig. 29. Diode current and voltage (D_2)

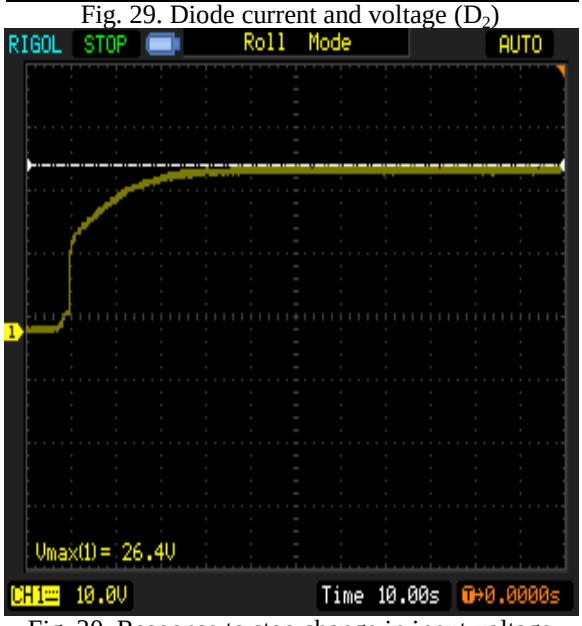


Fig. 30. Response to step change in input voltage

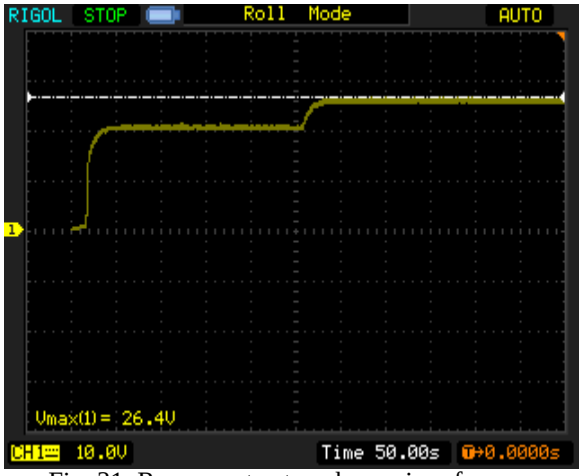


Fig. 31. Response to step change in reference

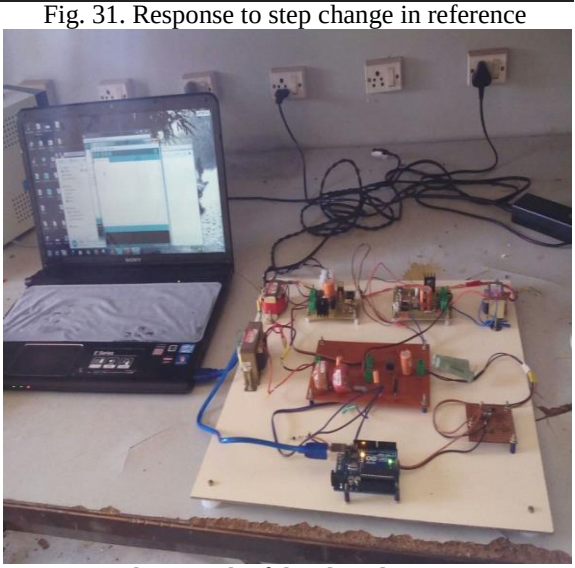


Fig. 32. Photograph of developed RDBIBPFCR

8. Conclusion

Due to the large harmonic content, typical single-phase bridge rectifiers used for interfacing power electronic equipment with utility system may exceed the limits on the individual current harmonics and THD specified by international standards. In this paper anew component waned single-phase boost ac-dc converter with a natural power factor correction has proposed. The presence of only one switch in the current path results in less switching loss and reduces the control complexity. The suggested single phase resonant boost converter, a resonant diode-bridge inserted boost PFC rectifier (RDBIBPFCR) with the designed type-II compensator combats against perturbations (line, load and circuit component variations). The topology enjoys the provision of offering negative output voltage by a minimal alteration. The performance comparison of the suggested topology with the existing topologies is compared for harmonic limits and other indices. The converters are simulated using PSIM software while the corroboration is done using the laboratory prototype based on Arduino board.

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