A HALF-BRIDGE DUAL OUTPUT CONVERTER WITH AN ASYMMETRIC PWM AND FM-LCC CONTROL

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Abstract—This paper discusses a half bridge converter with dual outputs.. Two independent regulated outputs are obtained with a single leg consisting of two switches. One of the two outputs is regulated through the switching frequency of an LCC resonant converter and the other output is controlled through duty cycle by asymmetrical pulse width modulation. The outputs are regulated over a wide range of input voltages and load variations. Cross regulation between the outputs is minimal due to independent control of each output. ZVS is also realized by the nature of the topology and higher switching frequencies are possible. The simulation and experimental results obtained for a converter with 48V input and 12V/20A and 5V/10A outputs are discussed.

Keywords — Asymmetric control, half-bridge, LCC resonant converter, Multiple outputs, PWM-FM , ZVS.

1. INTRODUCTION

Many industrial and military applications require the use of multiple supply voltages such that that the right voltage is supplied which would minimize energy consumption and would enhance speed of operation. Many instruments and appliances require various voltage/current levels for the different sub-modules. The multiple-output dc–dc converters are widely used for such applications. The key issue in the multiple output converters is the regulation of the various outputs against varying supply voltages and for different loads with minimum active and passive components. Cross regulation between the outputs is also an important consideration.

The simplest way to obtain multiple supply voltages would be to have one converter for each output. But this would require too many active and passive components. A reduction in hardware is possible if a transformer with multiple secondaries is used. The primary is common for all the outputs and each of the outputs is connected through a secondary winding. This reduces the hardware count since only one primary is used and the switch in the primary is also common for all the outputs. Generally the output with the maximum priority is regulated in a closed loop by controlling the switch in the primary. The other auxiliary outputs with lesser priority do not have any independent control and are said to be cross regulated. A variation in the primary load would vary the magnitude of other outputs as well due to the resistances and leakage inductances associated with the windings and also due to the varying drops in the rectifier diodes.

For low output current applications where the auxiliary outputs also need to be closely regulated, additional linear voltage regulators in the secondaries can be used. For medium and high output current applications, linear regulators would be very inefficient as they work in the active region where the effective resistance of the switch is high. Magnetic amplifier post regulators [2-3] have higher efficiency and the ability to handle high currents. However, they are more expensive and also bulky and this has limited their wide application. Synchronous-Switch Post Regulator (SSPR) [4-6] is another suitable way for high output current application, which utilizes a switching device as a post regulator. A switch in the secondary works as a buck regulator whose duty cycle is adjusted to regulate the voltage of the auxiliary outputs. For multiple output dc–dc converters by pulse width modulation-frequency modulation (PWM-FM) control [7-8], the main output is PWM controlled while the auxiliary output is regulated through the switching frequency. The frequency controlled converter could be of several types like series resonant, parallel resonant, LLC, LCC or LCLC converters.

Another way to obtain multiple-output dc–dc converters is the parallel regulation method. [9-10]. In this method, a controllable voltage source is added in the auxiliary output circuit. The auxiliary output is closely regulated by adjusting the magnitude of this controllable voltage source. This method is complementary to the earlier SSPR method in the sense that in the SSPR method the transformer secondary voltage input is fixed and the duty cycle of the switch in the secondary is varied whereas in the parallel regulation method the auxiliary voltage itself is varied suitably with an additional winding.

PWM-Pulse delay (PWM-PD) control method is another simple way to regulate multiple-output dc–dc converters [11-12]. In this method, three outputs are obtained from two switches. A third output is obtained by creating a phase delay between the other two outputs and the delay itself is varied to obtain a variation in the third output.

As an extension of this, for high voltage and high power applications, a full bride converter is proposed in [13] where each of the two legs is used as an asymmetrical half bridge converter. Two outputs are obtained by controlling the duty cycles of the two half bridge converters and the third one is controlled through the phase shift between the two legs. Three outputs are thus obtained with two legs consisting of four switches.

A combination of the asymmetrical duty cycle control and a frequency control is possible to get best results. [14-15]. Many non-isolated SIMO topologies have been proposed but this paper concerns only with isolated topologies. In this paper, an asymmetric half bridge PWM-FM converter is discussed. It has two switches connected in a half bridge configuration. One of the outputs is controlled by asymmetrical pulse width modulation and the other output is controlled through frequency in an LCC topology. An LCC topology combines the best advantages of series and parallel resonant converters with regulation over a wide range and a high efficiency. The input voltage of the converter is 48 V, and its outputs are 12V/20A and 5V/10A respectively. Zero voltage switching is also realized by operating the converter with a switching frequency above the resonant frequency.

This paper is organized as follows : Chapter 2 discusses the principle of operation of the presented converter, Chapter 3 discusses the design considerations, Chapter 4 presents the simulation results, Chapter 5 presents the details of hardware implementation and results and conclusions are presented in Chapter 6.

2. OPERATION OF THE CONVERTER

The proposed dual-output ZVS dc–dc converter is shown in Fig.1. Both the outputs are regulated through the switches in the primary side. The control signals are shown in Fig.2, where V_{AB} is the voltage input to the transformer T1 and T2. V_{AB} is applied through the LCC resonant elements LR1, CR1 and CP to the transformer T1 and through the blocking capacitor CB to transformer 2. The output V01 is regulated through the switching frequency of the asymmetrical half bridge converters composed of switches S1–S2. The half-bridge converter applies a square wave voltage of frequency (f_o) to the LCC resonant circuit. The resonant circuit has an effect of filtering the higher order harmonics so that a sine wave current is obtained over a wide range of loads which minimizes the device switching losses. The converter is thus suitable for operation at high switching frequencies . The output V02 is regulated through the duty cycle D1 of the asymmetrical half bridge converter and a continuous regulation is possible.

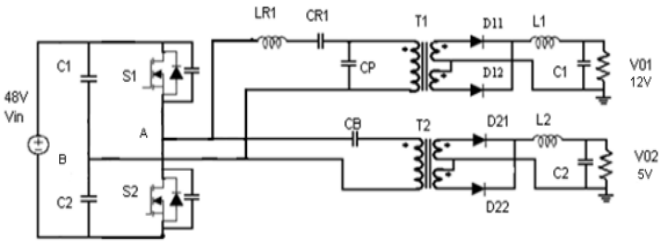

Fig .1 Proposed dual output DC-DC converter

According to the volt-second balance of the output inductors, output voltage V02 of the converter can be readily obtained as

$$V02 = \frac{2*Vin * D1 * (1-D1)}{n2} \qquad (1)$$

Where Vin is the input dc voltage, D1 is the duty cycle of the asymmetrical half bridge converter and n2 is the turns ratio of the transformer T2. From (1), the generalized voltage gain of the second output voltage to the input dc voltage can be derived as

$$G02 = \frac{V02}{Vin} = \frac{2*D1*(1-D1)}{n2} \qquad (2)$$

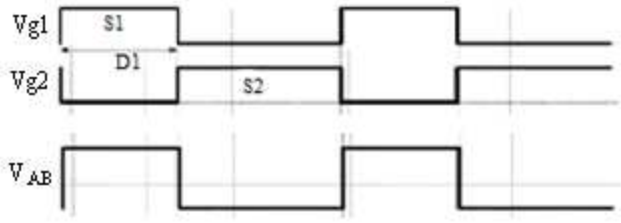

Fig. 2 Control signals of the dual output converter

The voltage gain curve in the form of a graph is shown in Fig. 3. It is a function of the duty cycle D1. The gain curve is a parabola, which reaches its peak when the duty cycle D1 is equal to 0.5. Corresponding to a given voltage gain, there are two different duty cycles, D1 and 1- D1 respectively. If the duty cycle D1 is chosen to be less than 0.5, from (1)

$$D1 = \left(\frac{1}{2}\right) - \sqrt{\left(\frac{1}{4}\right) - \left(\frac{n2*V02}{2Vin}\right)} \qquad (3)$$

and D1 < D1_max = 0.5, where D1_max is the maximum duty cycle of D1.

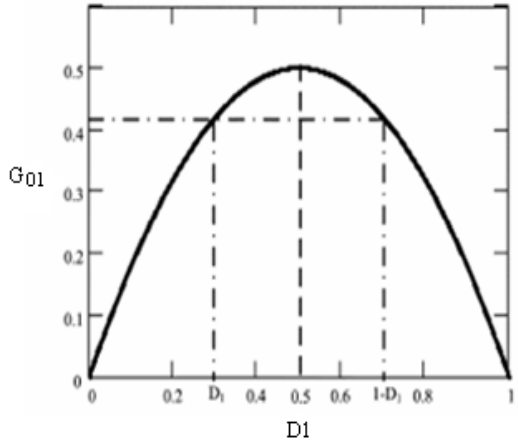

Fig.3. Gain-duty cycle curve for controlled outputs

For the other output, the equivalent circuit of LCC resonant converter is shown in fig. 4 and the analysis is done based on the fundamental approximation method. The input voltage V_{rms} to the resonant circuit is taken as the fundamental component of the square-wave voltage V_{AB}. Similarly the voltage V_{Rac} to the bridge rectifier is also assumed to be sinusoidal.

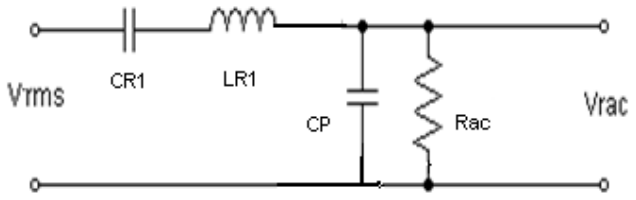

Fig.4. Equivalent circuit of LCC resonant converter

Because of the large value of filter inductor the output current is maintained constant and therefore, the rectifier input current is a square wave the polarity of which changes at the instant the polarity of voltage of capacitor CP changes. Voltage waveforms of LCC resonant converter is shown in Fig.5.

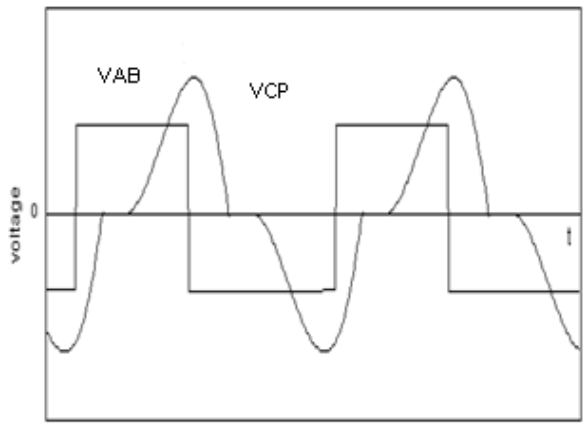

Fig.5.Voltages of LCC resonant converter

From the equivalent circuit, voltage transfer function is

$$\frac{V_{rac}}{V_{rms}} = \frac{1}{\left(1+\frac{X_{cs}}{X_{cp}}-\frac{X_L}{X_{cp}}\right)+j\left(\frac{X_L}{R_{ac}}-\frac{X_{cs}}{R_{ac}}\right)} \qquad (4)$$

Where,

$V_{rac} = \frac{\pi}{2\sqrt{2}} V_0$, for n=1, V_0 = DC output voltage,

$$V_{rms} = \frac{2\sqrt{2}}{\pi} V_{in}$$

V_{in} = DC input voltage, X_{cs} and X_{cp} are the series and parallel capacitive reactances.

If $Q_s(Quality\ factor) = \frac{\omega_s L}{R'_L}$; & $\omega_s(resonant\ frequency) = \frac{1}{\sqrt{LC_s}}$, then the generalized gain of the circuit can be expressed for n=1 as

$$\frac{V_0}{V_1} = \frac{1}{\frac{\pi^2}{8}\left[1+\frac{C_p}{C_s}-\omega^2 LC_p\right]+jQ_s\left[\frac{\omega}{\omega_s}-\frac{\omega_s}{\omega}\right]} \qquad (5)$$

Therefore, the first output V_{01} is given by

$$V_{01} = \frac{V_{in}}{\frac{\pi^2}{8}\left[1+\frac{C_{p1}}{C_{R1}}-\omega^2 L_{R1}C_{p1}\right]+jQ_s\left[\frac{\omega}{\omega_s}-\frac{\omega_s}{\omega}\right]} \qquad (6)$$

Gain–frequency characteristics of the resonant converter are shown in Fig. 6. The parameters are defined as follows: Voltage conversion ratio M, resonant frequency fr, and normalized switching frequency γ

$$M = \frac{V_o}{V_{in}} \qquad (7)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad (8) \quad ; \quad \gamma = \frac{f_s}{f_r} \qquad (9)$$

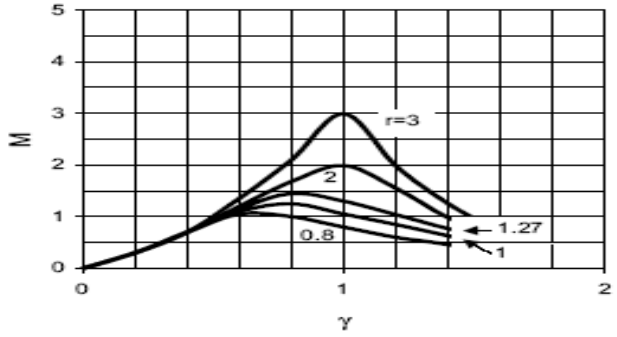

Fig.6. Gain –Frequency curves of LCC converter

3. DESIGN CONSIDERATIONS

From output equation (1), the turns ratio of transformer T2 can be calculated as

$$n_2 = \frac{2.V_{in*}.D_{1*}(1-D_1)}{V_{02}} \qquad (10)$$

where V_{in} is the input dc voltage, D_1 is the duty cycle and V_{02} is the second output voltage. Choosing a duty cycle of 0.4, n_2 becomes 16:3.5 (or 32:7).

A. DESIGN OF LCC TANK

The chosen specifications are as follows:

Input voltage – 48V, output voltage – 12V, switching frequency – 50 KHz and output power – 240W.

For a Cp/C_R of 1, from standard gain-frequency curves, for $\omega/\omega s = 1.1$, $Q_s = 4$.

Normalized output voltage at transformer primary is 0.8.

For half bridge, base voltage = 48/2 = 24V.

Output voltage at transformer primary = 0.8*24 = 19.2V

Transformer turn ratio n1 =19.2/12 = 1.6 (hence, a 16:10 transformer chosen)

Load current I_L = 240/12 = 20A

Load resistance R_L = 12/20 = 0.6 Ω

R'_L reflected in primary = Ω

For a Qs of 4, and ω =1.1 ωs

C_R = Cp = 0.59μf & L_R = 20.5μH

The blocking capacitor CB when large reduces the ripple but slows down the dynamic response. A 1μF value is chosen. [16].

4. SIMULATION RESULTS

The presented topology has been simulated using PSIM software and the circuit specifications are:

Input voltage	Switching frequency	Output voltage	Output power
48V	50KHz	12V	240W
		5V	50W

The detailed simulation is as shown below in Fig .

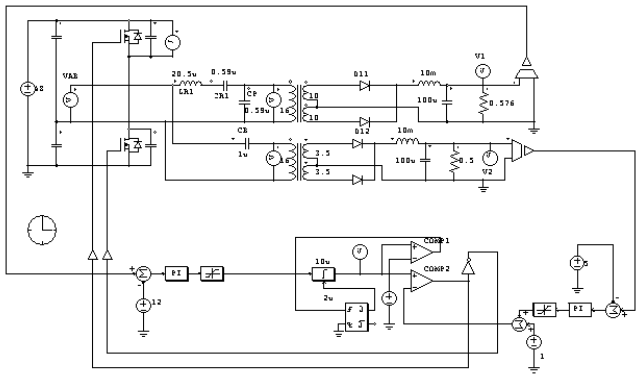

Fig 7 PSIM simulation of the dual output converter

The simulation results are as given below. The output voltage waveforms at full load on both the outputs are shown in Fig 8. The primary voltages of transformers are shown in Fig 9. The drain-source voltage of the switch S1 and its current are shown in Fig 10, indicating the ZVS action. To show the cross regulation performance, a 50% variation in the second load is simulated and the effect on the other output is shown in Fig 11. Similarly Fig 12 shows the effect of an increase in the supply voltage by 10% from 48 to 53V. In both cases, there is negligible effect on the output voltages and cross regulation effects are minimal.

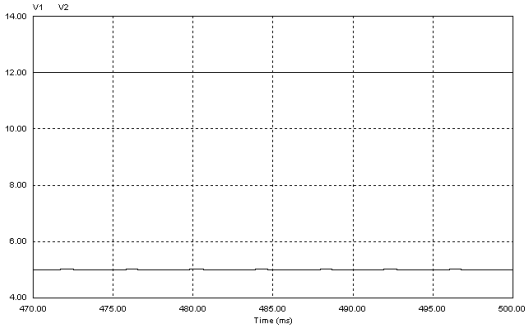

Fig 8 Output Voltages V1 and V2 at full load

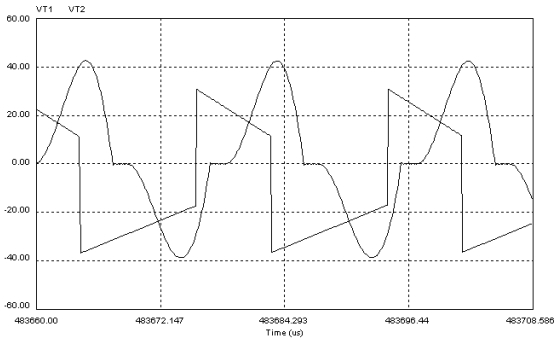

Fig. 9. Primary voltages of T1 (VCP) & T2

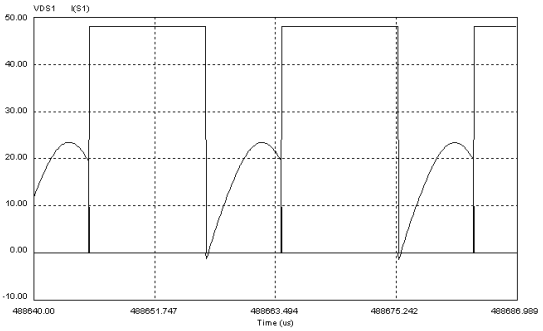

Fig. 10. Voltage and current of switch S1

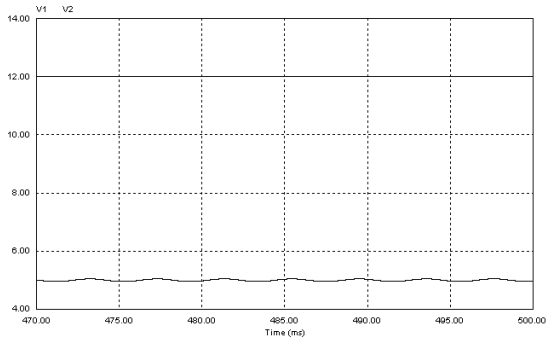

Fig.11. Output voltages when second load is halved

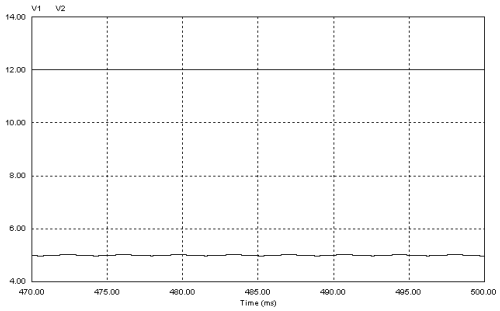

Fig.12. Output voltages when supply increased by 10%

5. HARDWARE DETAILS & RESULTS

The specifications chosen for the hardware are as follows :

Input voltage : 48V.
Switching frequency : 50 KHz.
Output Voltages : 12V / 2A / 24W and 5V / 2A / 10W.

IRFP150N HEXFET power MOSFET was chosen for the switch which was driven through IR 2110 drivers. MUR 460 Switch mode power rectifier was chosen for the diodes. The resonant inductor value used was 0.2mH and the resonant capacitors were 0.059 uF. Control was done using a micro controller AT89C2051 operated at 24MHz. The hardware layout is shown in Fig 13.

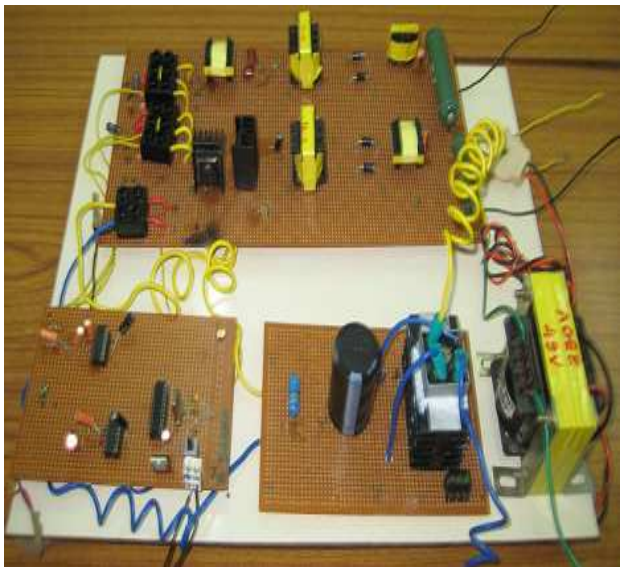

Fig 13 : Hardware layout

The input and PWM regulated output voltages are shown in Fig 14. The gate pulses and drain –source voltages of the two switches are shown in Fig 15 and 16 respectively.

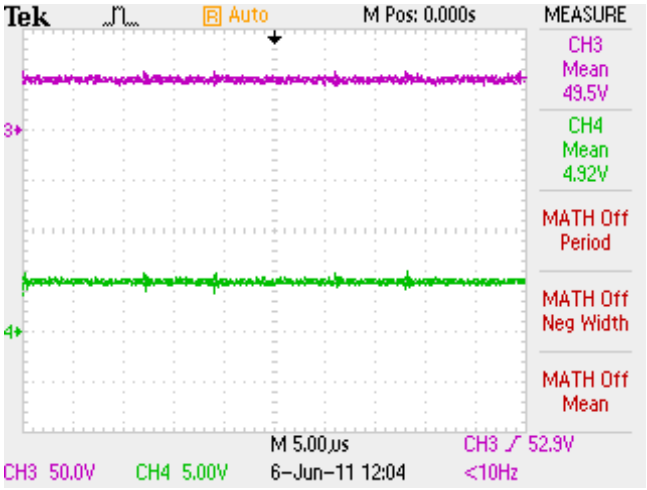

Fig 14 : Input and PWM regulated output voltages

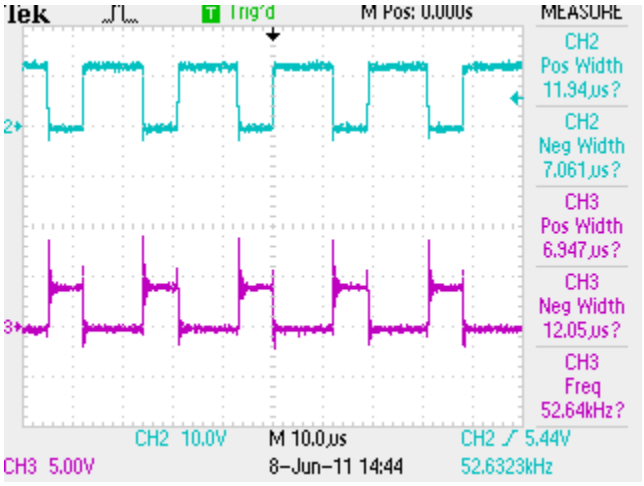

Fig 15 : V_{GS} & V_{DS} of switch S1

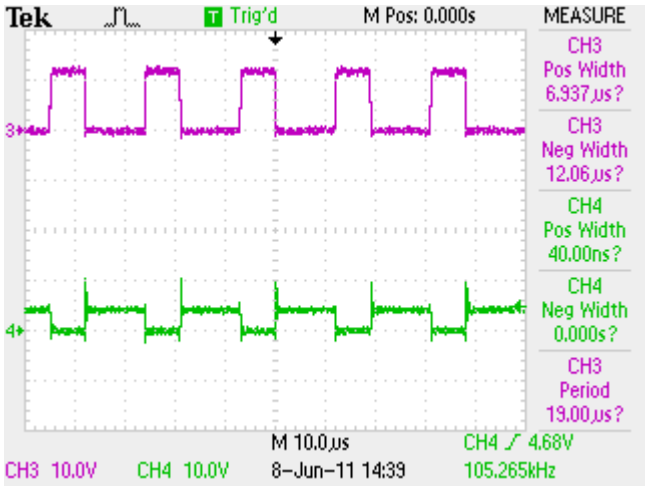

Fig 16 : V_{GS} & V_{DS} of switch S2

6. CONCLUSION

Asymmetric dual half-bridge PWM-FM converter was presented which was simulated using PSIM and tested in hardware. This configuration consists of two MOSFET switches to achieve dual outputs. The outputs are independently controlled through switching frequency(LCC topology) and duty cycle(asymmetric) and operate with effective regulation. ZVS is also realized. The outputs were found to be regulated for a wide input and load variation.

REFERENCES

1. Dhanalakshmi R, Sundararaman K, Gopalakrishnan M , (2011) "Asymmetric dual half-bridge PWM-FM converter with quad regulated outputs," Proceedings of the 3rd International conference on Electronics Computer Technology, ICECT 2011, Kanyakumari, 8-10 April 2011, Volume IV, p 412-416..
2. Lee J., Dan Y., Chen, & Jamerson C., (Magamp post regulator-practical design considerations to allow operation under extreme loading conditions),In: IEEE Trans. Power Electronics, (1990) Volume 5, No 1. January 1990, p 69-76
3. Wen C.-C., Chen C.-L., Chen W., & Jiang J., (Magamp post regulation for flyback converter),In: Proceedings of the IEEE 32nd Power Electronics Specialists Conference, PESC (2001), Vol 1, 2001, p 333-338.
4. Lin Y.-L., Kwang H., and Liu, (A new synchronous-switch post regulator for multi-output forward converter), In: Proceedings of the IEEE 5th Applied Power Electronics. Conference, APEC (1990), Volume 1, Mar. 11–16, 1990, p. 693–696.
5. Levin G., (A new secondary side post regulator (SSPR) PWM controller for multiple output power supplies)," In: Proceedings of the. 10th IEEE Applied. Power Electronics. Conference.APEC, (1995) Volume 2, Mar. 5–9, 1995, p. 736–742.
6. Xi Y. and Jain P. K., (A forward converter topology with independently and precisely regulated multiple outputs), In : IEEE Trans. Power Electron., (2003)Vol. 18, No. 2, March 2003, p 648–658..
7. Sebastian J., Uceda J., Rico M., Perez M. A., and Aldana F., (A complete study of the double forward-flyback converter), In: Proceedings of the. 19th IEEE Power Electronics Specialists Conference, PESC (1988) Volume 1, April. 11–14, 1988, p. 142–149.
8. Tacca H. E.,(Single-switch two output flyback-forward converter operation), In : IEEE Trans. Power Electron.,(1998), Vol. 13, No. 5, Sep 1998, p 903-911
9. Ferreres A., Carrasco J. A., Sanchis E., Espi M., and Maset E., (Application of a novel parallel regulation technique in a two output forward converter), In : Proceedings of the 30th Power Electronics. Specialist. Conference PESC (1999)., Jun. 27–Jul. 1, 1999, Volume 2, p. 914–919.
10. Ferreres A., Carrasco J. A., Sanchis E., Espi M., and Maset E., (Small-signal modeling of a controlled transformer parallel regulator as a multiple output converter high efficient post-regulator), In : IEEE Trans. Power Electron., Vol. 19, (2004) No. 1, Jan 2004, p. 183–191.
11. Barrado A., Olias E., Lazaro A., Pleite J., and Vazquez R., (PWM-PD multiple output dc–dc converters: Operation and control loop modeling), In : IEEE Trans. Power Electron., vol. 19,(2004) No. 1, Jan 2004, p. 140–149.
12. Barrado A., Olias E., Lazaro A., Pleite J., and Vazquez R., (Multiple output DC/DC converters based on PWM-pulse delay control (PWM-PD)), In: Proceedings of the IEEE 30th Power Electronics Specialist Conference, PESC, (1999) Jun. 27–Jul. 1, 1999, Volume 2, p. 1141–1145.
13. Yanjun Z. and Dehong X., (Design and Implementation of an Accurately Regulated Multiple Output ZVS DC-DC Converter), In : IEEE Transactions on Power Electronics, , Vol. 22, (2007) No 5 , Sep 2007, p. 1731-1742.
14. E. H. Kim, J. J. Lee, J. M. Kwon, W. Y. Choi and B. H. Kwon, (Asymmetrical PWM half-bridge convertor with independently regulated multiple outputs), In : IEE Proceedings Electric Power Applications, Vol 153,(2006), No 1, Jan 2006 p. 14-22.
15. Christopher M. Bingham, Yong Ann Ang, Martin P. Foster and David A. Stone, (Analysis and Control of Dual-Output LCLC Resonant Converters, and the Impact of Leakage Inductance,) In : IEEE Transactions on Power Electronics, Vol. 23, (2008) No. 4, July 2008, p 1724-1732.
16. Chen T M, Chen C L, (Analysis and design of asymmetrical half bridge flyback converter) In : IEE proceedings of Electric Power applications, Vol 149 (2002), No 6, Nov 2002, p 433-440.
17. Rashid, : (Power electronics handbook), Academic Press, 2001.
18. P.C.Sen, (Modern Power Electronics), S.Chand & Co, 2004.