Design and Fabrication of a Non dissipative Charge Equalization Converter for Battery Stack used in Hybrid Electric Vehicle

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Abstract: **With increasing interest to decrease vehicle pollution and consumption of fossil fuels Hybrid Electric vehicle has taken on an accelerated pace. Energy storage systems (ESS) composed of battery stack play an important role in Electric Vehicle (EV) and Hybrid Electric Vehicle (HEV). In battery stack, small differences between charges under operating conditions tend to be magnified in each charge or discharge cycle. This paper proposes a Non Dissipative Novel Charge Equalization Converter (NDNCEC), in which the intra-module and inter-module equalizer are implemented to equalize the battery charging levels. The equalizer balances the whole stack by sequentially compensating the battery with low charge. The effectiveness of the proposed converter is confirmed by simulating it in MATLAB/SIMULINK software. The robustness of the proposed converter to parametric variations is observed through simulation and experimental studies. The simulation results prove that the proposed voltage equalization circuit is characterized with rapid equalization and simple control. Experimental results of proposed converter validate the equalization scheme which promised low voltage stress, small size and short equalization time.**

Index Terms**—** Hybrid Electric Vehicle, Non dissipative Charge Equalization Converter, Battery Stack.

1. INTRODUCTION

With increasing interest to decrease vehicle pollution and consumption of fossil fuels Hybrid Electric vehicle **(**HEV**)** has taken on an accelerated pace. The dream of having commercially viable Electric vehicles and Hybrid electric vehicles is becoming a reality. The technology used depends on the goals set for the vehicle, which includes fuel efficiency, power and driving range or reduced greenhouse gas emissions [1]-[3]. Most HEVs on the streets today use nickel metal hybrid (Ni-MH) batteries. A hybrid vehicle is an automobile that has two or more major sources of propulsion power. Most hybrid vehicles currently marketed to consumers have both conventional gasoline and electric motors, with the ability to power the vehicle by either one independently or in tandem. Consumer oriented hybrid vehicles, which have been on the market for about ten years, are usually tuned for reduced emissions and driving range. Corporate and government fleets that have been in service for twenty years or more are usually tuned for fuel efficiency, often at the cost of driving range, power, and hydrocarbon emissions Recent developments in the Lithium ion battery have higher power and energy density, a lower self-discharge rate and higher single cell voltage than the Ni-MH battery. Continual charge and discharge of series connected batteries can cause charge imbalance [4]-[5]. The problem arises when batteries are left in use without any control such as cell equalization converter. For example, in regenerative braking mode, highly charged batteries cannot capture an optimal amount of renewable energy and can cause charge imbalance. Deeply discharged batteries in Battery Electric Vehicles (BEV) cannot provide sufficient stored energy and causes charge imbalance. Therefore, charge equalization for the series connected battery stack is essential to prevent these undesirable situations and accomplish the maximum utilization of the battery and strengthen its lifetime. So a novel voltage equalization circuit is proposed in this paper. The capacitor stack (in place of Battery stack to show rapid charge and rapid discharge) contains three capacitors (C_1, C_2, and C_3). The voltage equalizer consists of a full-bridge converter and input to the converter is from the capacitor stack. The full bridge converter feeds to a linear transformer. The inductor L is introduced here to limit the current. All of the transformer's secondary's have the same turns to ensure that each battery output has the same voltage level. When the equalizer works, the secondary of the linear transformer are clamped to a lower voltage, and the other bridge rectifiers remains **OFF**. Hence, the equalization current only flows into the weakest capacitor cell(s), and no equalization current flows into the other capacitor cell(s). As a result, the voltage of the weakest capacitor rises. Until the voltage of the weakest capacitor reaches the voltage of the second weakest capacitor, both of the full bridge rectifiers of these two capacitor cells turn **ON**. Hence, the equalization current flow into both of these capacitor cells at the same time there by the voltages of these two capacitor cells rises. At the same time that the weakest cell(s) is (are) being charged, the other capacitor's voltage decreases, because the energy to the weakest cell(s) is from the whole stack. On this analogy, the whole capacitor stack finally reaches the same voltage.

2. PROPOSED BLOCK DIAGRAM

The operational modes of the proposed equalization circuit is as shown in Figure.1 can be separated into four parts. Figure 2 shows the key wave forms of the proposed converter. The different modes of operation of the proposed circuit are shown figure.3 to figure.6 respectively. The three capacitor stacks is taken in the equalizing circuit and charging current is I_{in} and turns ratio of Linear Transformer is 1:1. The converter operates with a 50% duty cycle .

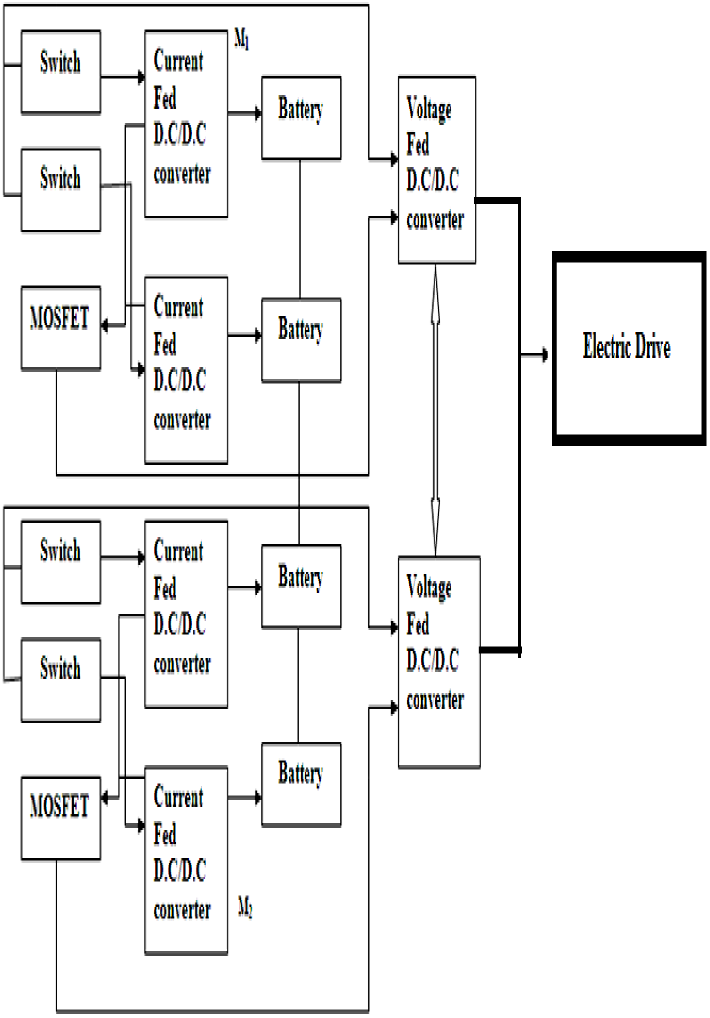

Figure.1 Proposed Block diagram of Charge Equalization converter

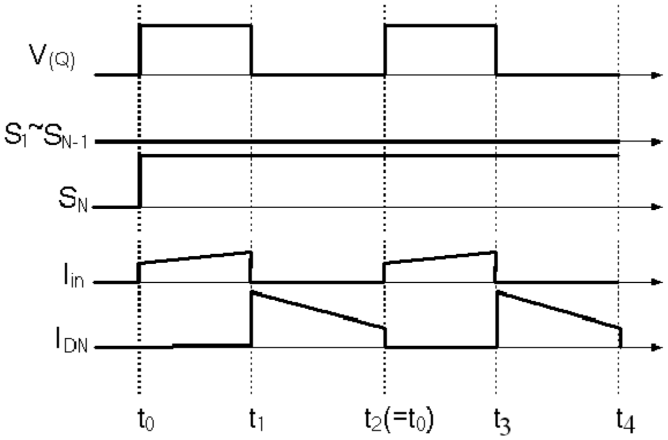

Figure.2 Key wave form of proposed charge Equalization converter

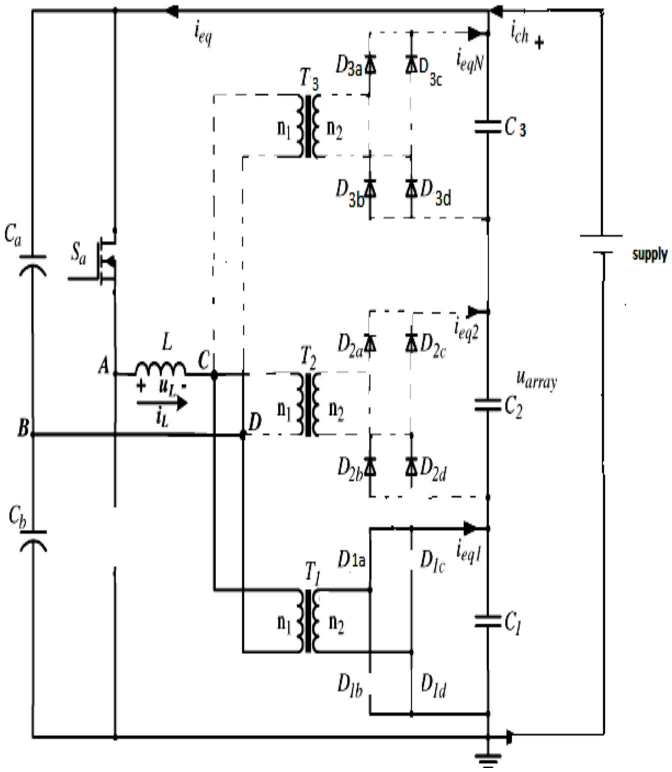

Figure.3 Mode 1 operation of proposed converter

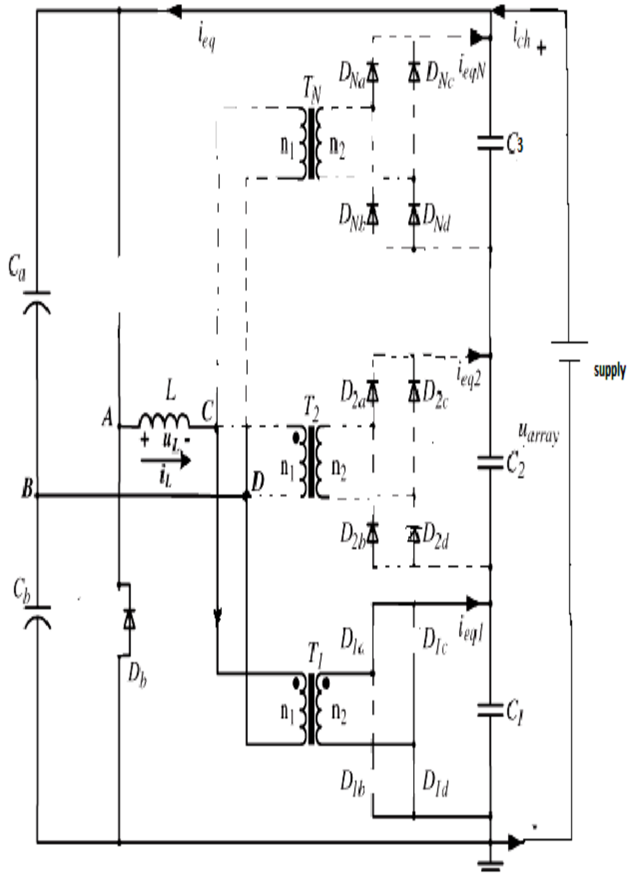

Figure.4 Mode 2 operation of proposed converter

In **Mode 1 (**t_0-t_1**)** shown in Figure.3, switch S_a conducts their by diodes D_{1a}, D_{1d} are entered into conduction state. So equalization current flows through S_a, D_{1a}, D_{1d}.In **Mode 1(**t_0-t_1**),** shown in figure.3, **s**witch S_a conducts and diodes D_{1a}, D_{1d} are forward biased. In **Mode 2(**t_1-t_2**),** shown in Figure.4, **s**witch S_a is turned **OFF** and D_{1a}, D_{1d} continue to conduct, inductor current I_{in} commutates into D_{1b} to freewheel and rapidly drops there by energy is continuously transferred to weakest capacitor cell C_1. At the end of this interval, the inductor current drops to zero and diodes D_{1a},D_{1d} and D_{1b} are **OFF**. In **Mode 3**(t_2-t_3) shown in Figure.5 **s**witch S_b conducts and D_{3b}, D_{3c} are forward biased there by C_1 is charged. The inductor current reversibly increases at same rate as in interval1 **(**t_0-t_1**)**. In **Mode 4**(t_3-t_4), shown in Figure.6, switch S_b is turned OFF and diodes D_{3b}, D_{3c} are still forward biased. The energy is still transferred to the weakest battery C_1.This is the intra-module equalization process [6-10]. In addition, there are additional equalizing currents, which are the magnetizing currents from the inter-module equalizer. In other words, the magnetizing currents are reset through the first cell voltage.

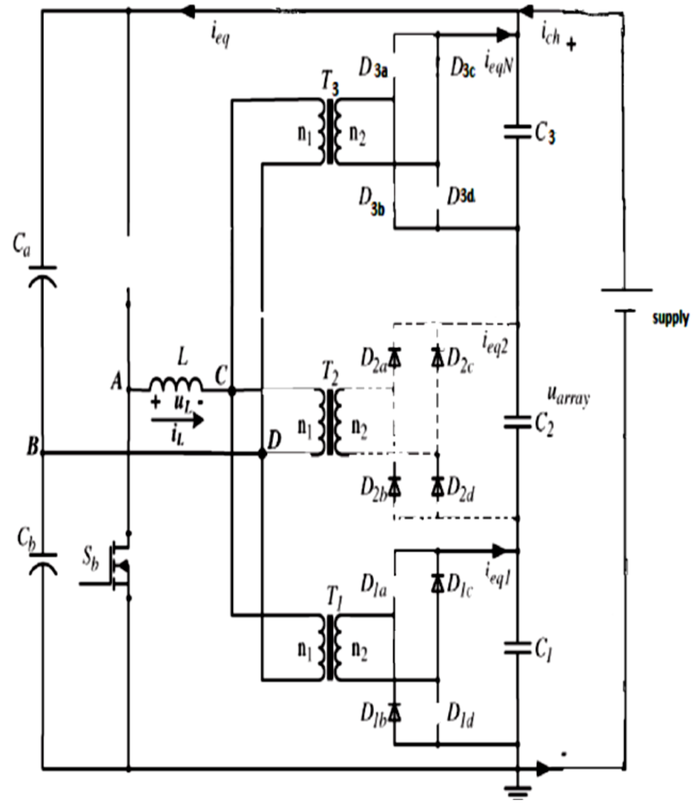

Figure.5 Mode-3 operation of converter

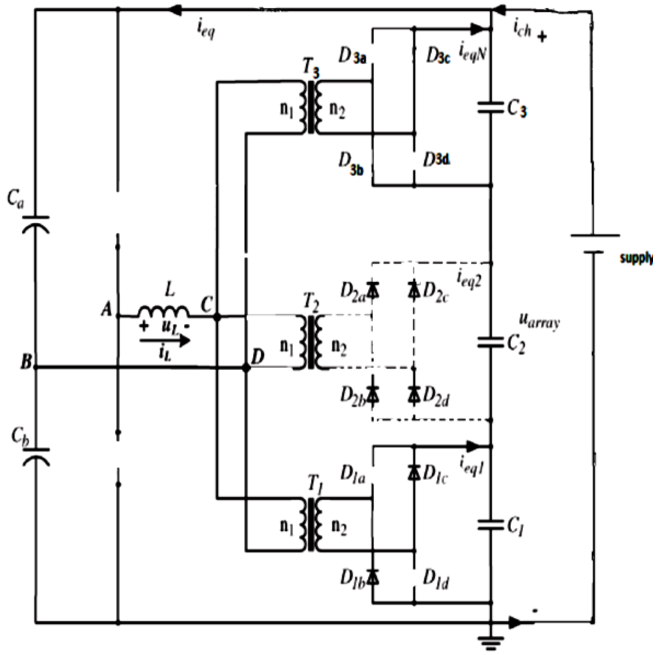

Figure.6 Mode-4 operation of converter

3. DESIGN ASPECTS OF CONVERTER

To obtain high power density of the proposed circuit, the optimal power rating design rule will be applied. The optimal power rating selection guide can provide the minimal size of the cell balancing circuit while achieving equalization within the cell balancing time. In this paper, this power rating design rule will be applied only to the intra-module equalizer, not the inter module equalizer since the inter-module equalization can be achieved automatically by using the voltage-fed DC/DC converter. [11-14]. Here proposed charge equalization circuit is designed for 3 capacitor cells which are grouped into 1 module.

The following equations are used to get the optimal power rating of the intra module equalizer with in time of equalization,

$$Q_1(t) = \frac{1}{3}\sum_{n=2}^{n=3} Qn(t) \tag{1}$$

$$P_{out,avg} = \eta\ P_{in,av} \tag{2}$$

$$Q_1(t) = Q_1(0) + I_1\ .t = Q_1(0) + (I_{out} - I_{in}).t \tag{3}$$

$$P_{out\ ,avg} = \left(V_1(0) + \frac{1}{2C}(I_{out} - I_{in}).t \right).I_{out} \tag{4}$$

Where

$Q_n(t)$ is charge quantity of the n^th^ cell at time t

$V_n(t)$ is Voltage of the n^th^ cell at any time t

I_n is input current of the n^th^ cell

I_{in} is input of the intra module equalizer

I_{out} is output current of the intra module equalizer

$P_{in}(t)$ is input power of the intra module equalizer at time t

$P_{out}(t)$ is output power of the intra module equalizer at time t

$P_{in,avg}$, is average input of the intra-module equalizer

$P_{out,avg}$ is average output power of the intra-module equalizer

η is overall efficiency of the intra-module equalizer

4. SOFT WARE AND HARD WARE IMPLEMENTATION OF PROPOSED TECHNIQUE

The proposed model is simulated as shown in figure .7 through Multisim soft ware. In the converter shown in figure.7, MOSFETS are used in place of selection switches and for convenience the batteries are replaced by the capacitors**.** Here the initial voltages are different for different capacitors. After execution voltage waveform across each capacitor(s) as shown in figure.8 is observed. To verify the operational principles of the proposed cell balancing circuit and also the usefulness of the optimal power rating design rule, a prototype is implemented. The magnetizing current of the intra-module equalizer flows into the first cell through the rectifier diode, D_1, M_1, during the turn-off period of a MOSFET switch. In addition, the magnetizing current of the inter-module equalizer is reset through the voltage of the first cell. The equalizing current flows from the second module into the first during the turn-on period of the MOSFET switches The maximum voltage stress of the proposed equalization circuit resides at the MOSFET switches and its value does not exceed 8V including the voltage spikes. From these results, one can see that the proposed balancing circuit has advantageous features such as low voltage stress due to modularization and efficient equalization during the entire equalization time. The output voltage of the weakest cell battery and inductor current are shown in figure.8 and figure.9 respectively. From this result, the proposed charge equalization circuit, implemented by using the optimal power rating design rule, shows outstanding charge balancing performance within a high power density.The Charge Equalization for series-Connected battery circuit consists of batteries which are to be equalized, converter circuits, selection switches and a pair of MOSFETs.

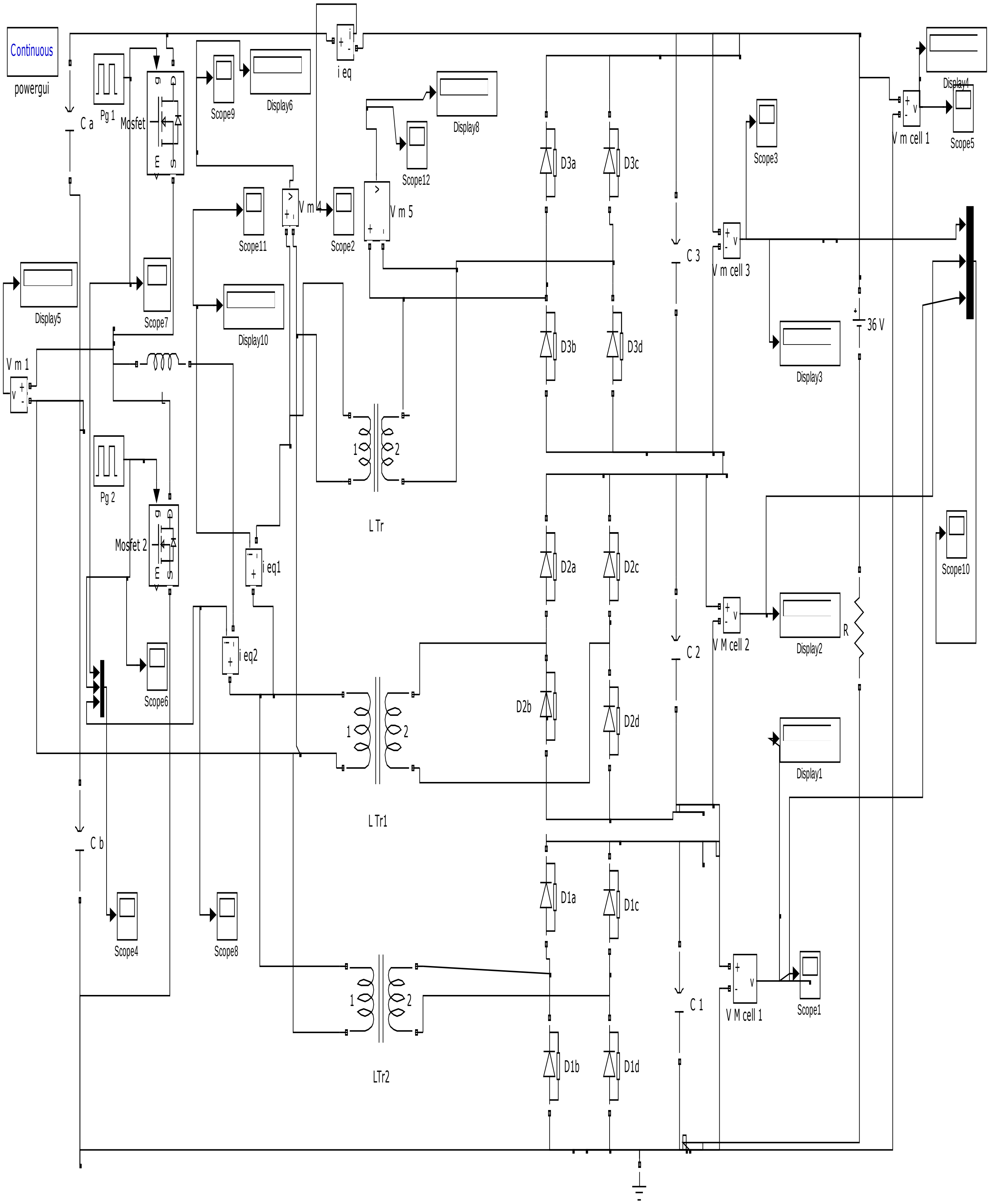

Figure.7 Simulink model of proposed circuit

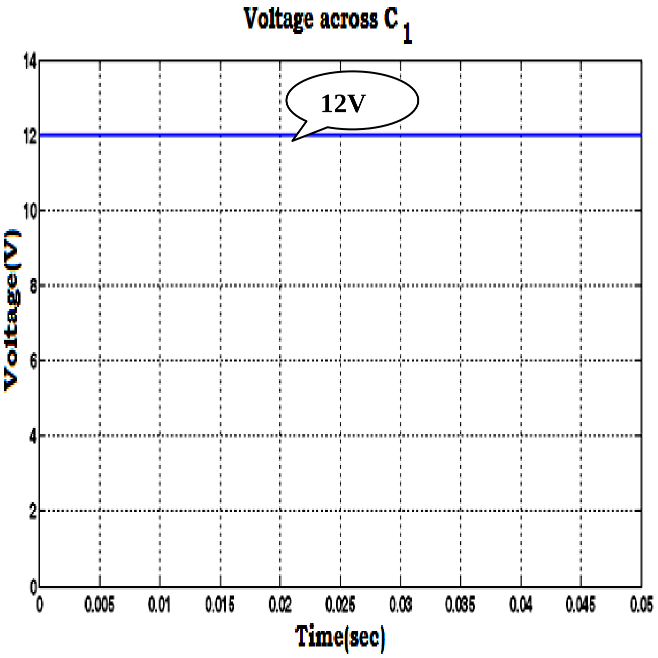

Figure.8: Simulation result for charging the capacitor C_1 when Input voltage is 36V

Hard ware and simulated results are given inTable.1 and shown graphically in figure.12. A hardware model shown in figure.10 is designed with the batteries of rating 12V, 4.5Ah and fabricated. Voltage across each and every cell is shown from figure.11(a) to figure.11(c) respectively

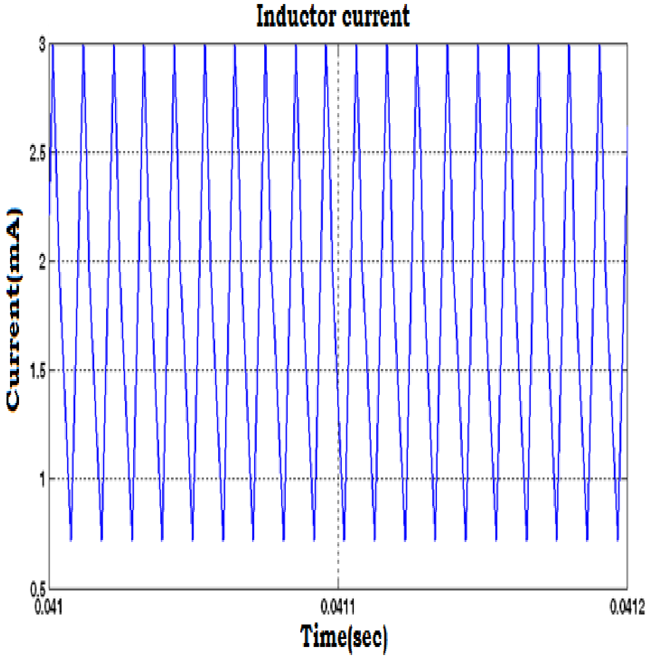

Figure.9 Inductor current variation

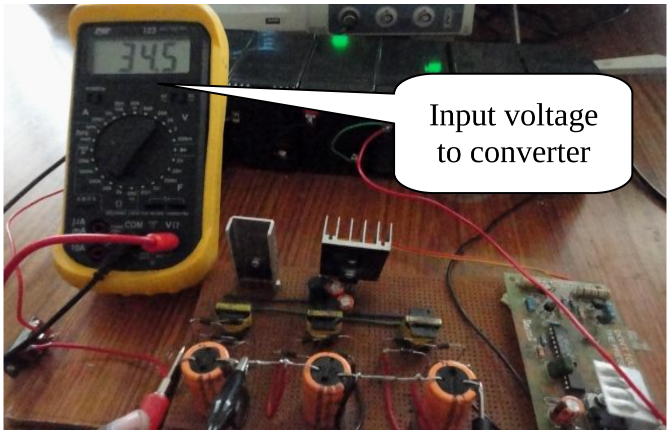

Figure.10 Hardware Model of Circuit under Operation when input is 34.5 volts

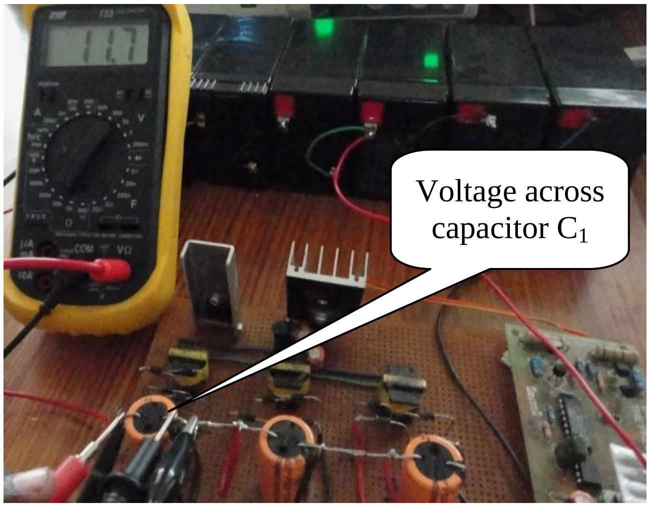

Figure.11(a) Output voltage across capacitor C_1

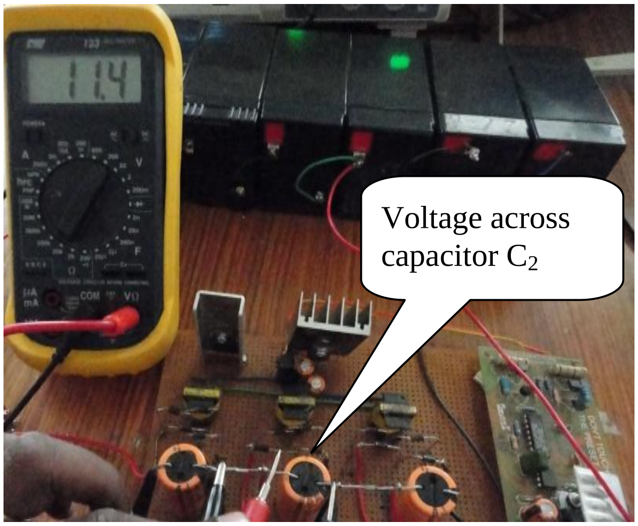

Figure.11(b) Output voltage across capacitor C_2

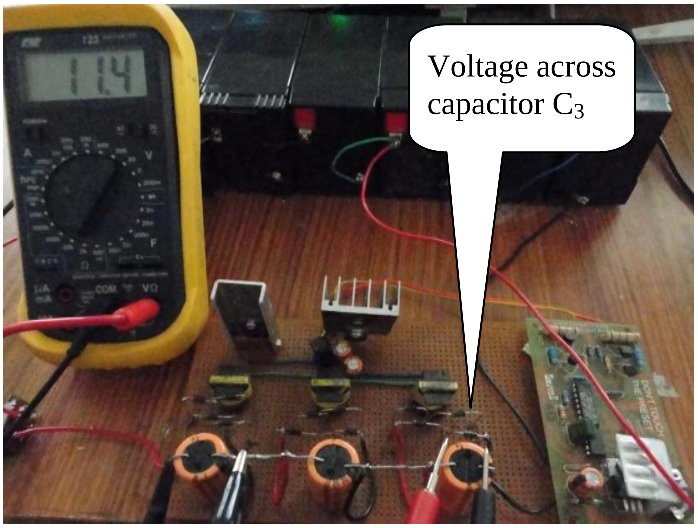

Figure.11(c): Output voltage across capacitor C_3

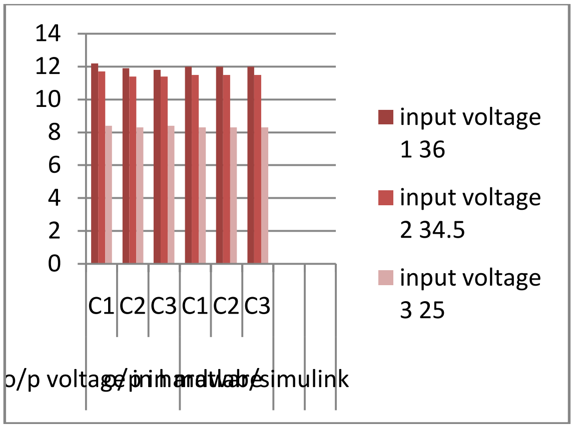

Figure.12 Graphical comparison of software and hardware results of proposed converter

Table.1: Comparison of battery voltages measured in simulated and fabricated converter

Voltage (V)		**Output voltage measured in fabricated converter circuit**			**Output voltage measured in Simulated converter circuit**		
		C_1	C_2	C_3	C_1	C_2	C_3
Input voltage 1	36	12.2	11.9	11.8	12	12	12
Input voltage 2	34.5	11.7	11.4	11.4	11.5	11.5	11.5
Input voltage 3	25	8.4	8.3	8.4	8.3	8.3	8.3

5. CONCLUSIONS

A non dissipative voltage equalization converter for Electric and Hybrid Electric Vehicle is simulated and tested.Compared with the dissipative converter, proposed converter does not need the voltage-detection and comparative circuits. Simulation and experimental setup of a 36V battery stack is carried out to verify its feasibility for Electric and Hybrid Electric vehicles. Simulation and experimental results are compared to validate the equalization effect. The results proved that the proposed voltage equalization circuit is able to produce equalization for battery stack and validate the proposed equalization scheme.

6. REFERENCES

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