A CASCADED MULTILEVEL PHOTOVOLTAIC INVERTER TOPOLOGY WITH HYBRID PHASE DISPOSITION MODULATION FOR GRID CONNECTED PV SYSTEM

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Abstract: *This paper presents a generalized cascaded multilevel photovoltaic inverter topology for grid connected PV systems with hybrid phase disposition PWM control scheme. Hybrid PWM strategy is based on the combination of fundamental frequency PWM and high frequency phase disposition PWM which reduces the power losses and improves energy efficiency. A digital proportional–integral current control algorithm is also implemented in TMS320F2407 digital signal processor to keep the current injected in to the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions. Xilinx Complex Programmable Logic Device (CPLD) is used to realize the hybrid PWM algorithm and it is integrated with digital signal processor for hybrid phase disposition PWM generation. This inverter offers much less weighted total harmonic distortion, high conversion efficiency and can operate with low thermal stress. The proposed system is verified through simulation and it is implemented in a low power prototype, and the experimental results are compared with conventional grid connected PV systems.*

Keywords: *complex programmable logic device, digital signal processor, hybrid phase disposition modulation, multilevel photovoltaic inverter, weighted total harmonic distortion*

1. Introduction

The demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. Photovoltaic (PV) sources are used today in many applications as they have the advantages of being maintenance and pollution free. Solar-electric-energy demand has grown consistently by 20%–25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices. This decline has been driven by the following factors: 1) an increasing efficiency of solar cells; 2) manufacturing technology improvements; and 3) economies of scale [1].

Photovoltaic inverter, which is the heart of a PV system, is used to convert dc power obtained from PV modules into ac power to be fed into the grid [2]. Multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveforms. In recent years, multilevel inverters have become more attractive, because it has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Forth, lower acoustic noise and electromagnetic interference (EMI) is obtained [3].

Multilevel inverter topologies are classified in to three categories: diode clamped inverters, flying capacitor multilevel inverters and cascaded inverters. The topologies have an equal number of main switches [4]. The diode clamped inverter uses a single dc bus that is subdivided in to number of voltage levels by a series string of capacitors. A matrix of semiconductor switches and diodes allows each phase leg output to be switched to any of these voltage levels. Flying capacitor inverter requires the most number of capacitors. Furthermore, for low switching frequency, the clamping capacitors become large in size thus decreasing the power density of the inverter. Comparing these topologies, the cascaded multilevel inverter offers a simple modular structure and the use of low power converter modules.

In this topology, no clamping capacitors or diodes are necessary. The switches of the each phase leg of diode clamped, flying capacitor multilevel inverter is not equally loaded and it presents difficulties with practical implementation. This complexity has generally restricted cascaded inverters to the higher power range where several switched output voltage levels are needed and diode clamped structure is unsuitable because of the difficulty of balancing the series dc capacitor voltages [5]. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular.

Modulation control of any type of multilevel inverter is quite challenging, and much of the reported research is based on somewhat heuristic investigations. Switching losses in high power converters represent an issue and any switching transitions that can be eliminated without compromising the harmonic content of the final waveform is considered advantageous [6]. Now, this paper proposes a new modulation technique that is focused on minimizing the power losses of the cascaded inverter. Furthermore the inverter is used in a PV system, a proportional–integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity.

2. Cascaded Photovoltaic Inverter and Control System Algorithm

Cascaded multilevel inverter is a series cascade of single phase full bridges to make up each phase leg of the main inverter. The proposed single-phase five-level inverter topology is shown in fig. 1. The inverter adopts a cascade connection of two full-bridge configuration with dc-dc boost converter. Photovoltaic arrays (PV arrays) are used as input voltage sources for this inverter. PV arrays are connected to the inverter via a dc–dc boost converter. PV voltage source is boosted by a dc–dc boost converter to exceed grid voltage to ensure power flow from the PV arrays into the grid. The proposed inverter is used in a grid-connected PV system; utility grid is used instead of load. A filtering inductance L_f is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion.

The feedback controller used in this application utilizes the digital PI control algorithm. As shown in block diagram fig.2, the current injected into the grid, also known as grid current i_g is sensed and fed back to a comparator which compares it with the reference current (i_{ref}) . It is obtained by sensing the grid voltage and converting it to reference current and multiplying it with constant Q. This is to ensure that grid current i_g is in phase with grid voltage v_g and always at near-unity power factor. One of the problems in the PV generation systems is the amount of the electric power generated by solar arrays always changing with weather conditions, i.e., the intensity of the solar radiation. A maximum power point tracking (MPPT) method or algorithm, which has quick-response characteristics and is able to make good use of the electric power generated in any weather, is needed to solve the aforementioned problem. Constant Q is derived from the MPPT algorithm incorporated in the closed loop operation. The perturb-and-observe algorithm is used to extract maximum power from PV arrays and deliver it to the inverter. The instantaneous current error is fed to a PI controller. The integral term in the PI controller improves the tracking by reducing the instantaneous error between the reference and the actual current. The resulting control signal u which forms reference signals that is compared with a triangular carrier signal, and intersections are sought to produce high frequency phase disposition signals.

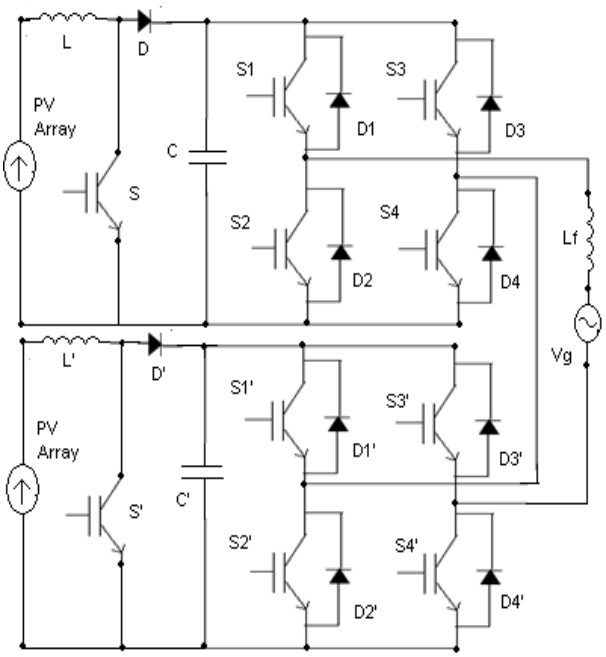


Fig.1. Schematic diagram of the cascaded multilevel photovoltaic inverter topology used to verify the proposed hybrid phase disposition modulation

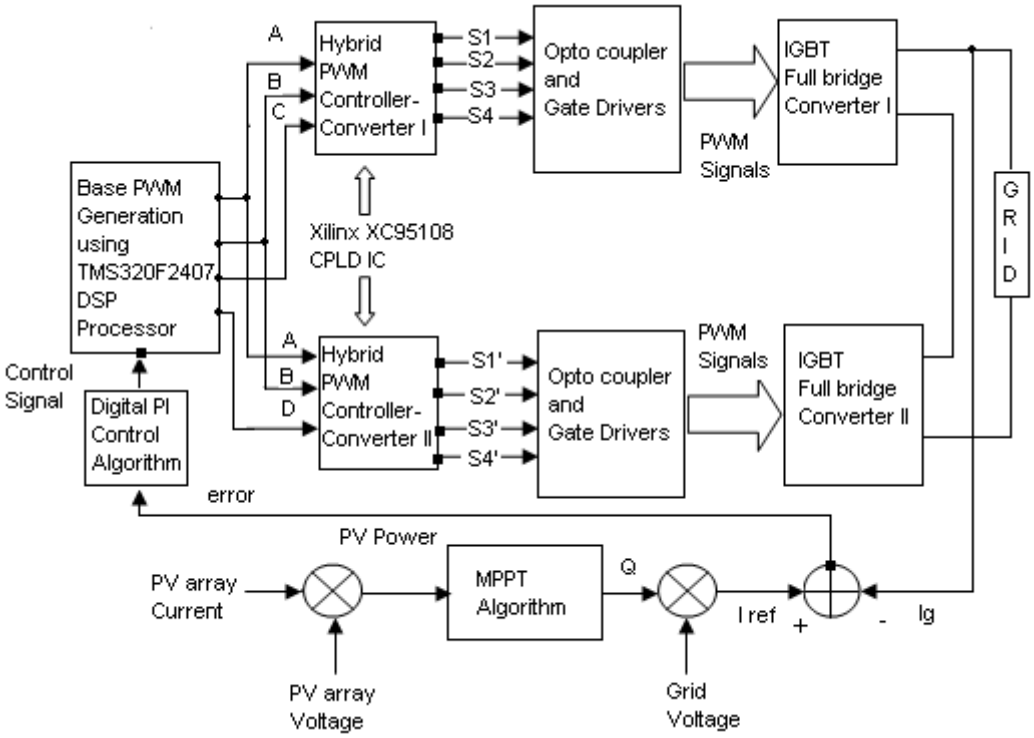


Fig.2.Block diagram of the proposed cascaded photovoltaic inverter with closed loop control algorithm

The PI algorithm can be expressed in the continuous time domain as

$$u(t) = K_p\, e(t) + K_i \int_{\tau=0}^{t} e(\tau)\, d\tau$$

where

u(t) control signal; e(t) error signal;
t continuous-time-domain time variable;
τ calculus variable of integration;
K_p proportional-mode control gain;
K_i integral-mode control gain.

Implementing this algorithm using a DSP requires one to transform it into the discrete-time domain [7]. Trapezoidal sum approximation is used to transform the integral term into the discrete-time domain because it is the most straightforward technique. The mathematical expressions for discrete PI control law is represented as

$$u(k) = K_p\, e(k) + K_i \left(\frac{h}{2}\right) \mathrm{sum}(k)$$

$$\mathrm{sum}(k) = \mathrm{sum}(k-1) + [e(k) + e(k-1)]$$

where h is sampling period and k is discrete-time index. These two equations, which represent the discrete-time PI control law, are implemented in TMS320F2407 DSP processor to control the overall operation of the inverter. Control signal saturation and integral mode antiwindup limiting is also implemented in software.

3. Proposed Hybrid Phase Disposition PWM technique

The idea here is to mix fundamental frequency PWM and conventional phase disposition PWM (PD-PWM) for each inverter module operation, and therefore the output contains the features of fundamental frequency PWM and PD-PWM. In this hybrid modulation, the four switches of each inverter module are operated at two different frequencies, two being commutated at fundamental frequency, while the other two switches are pulse width modulated at phase disposition switching pattern. Unfortunately, this arrangement causes the problem of different switching losses and therefore differential heating among the switches. In order to overcome this problem, a sequential switching scheme is embedded in hybrid modulation. Fig.3 shows the general structure of the proposed hybrid phase disposition PWM method. It consists of base PWM generator and hybrid PWM controller to generate new modulation pulses.

3.1 Base PWM generator

In this modulation strategy, three base PWM signals are required for each inverter module in a cascaded multilevel inverter. A sequential signal (A) is a square signal with 50% duty ratio and it has half of the fundamental frequency.

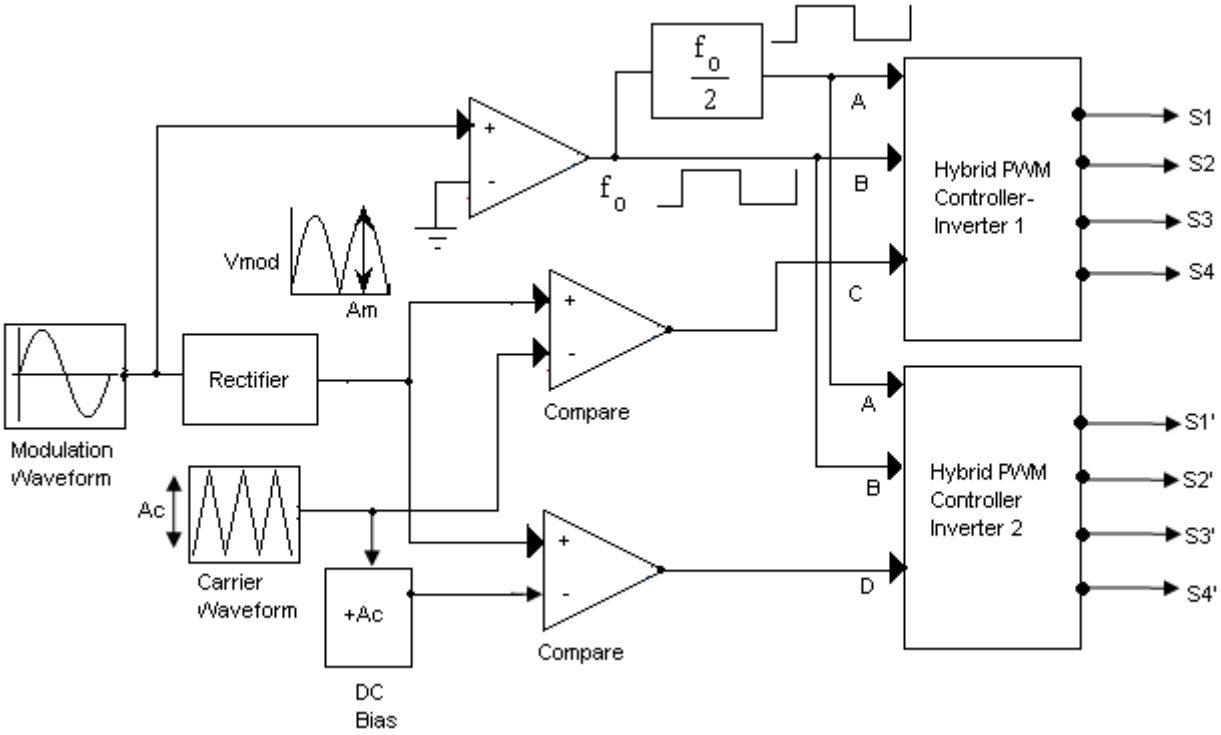


Fig.3.Scheme of the Hybrid Phase Disposition PWM technique

This signal makes every power switch operating at PD-PWM and fundamental frequency PWM sequentially to equalize the power losses among the switches. Fundamental frequency PWM (B) is a square wave signal synchronized with the modulation waveform, and is defined as B=1 for during positive half cycle of the modulation signal; B=0 for during negative half cycle of the modulation signal. A PD-PWM signal is obtained by the comparison of rectified modulation waveform with carrier waveform for each inverter module.

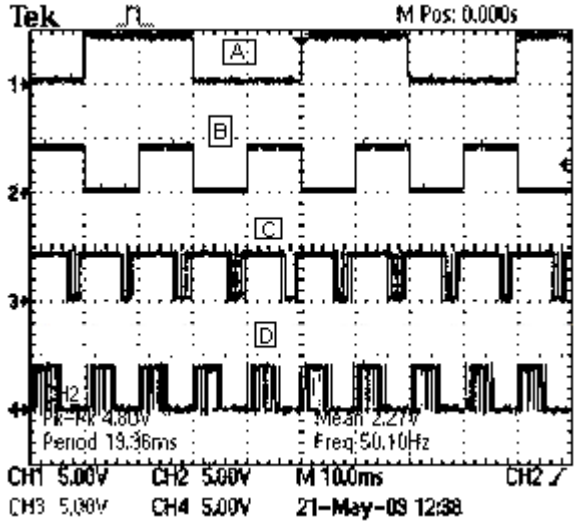


Fig.4. Base PWM signals for five-level Cascaded Multilevel Inverter

For N level PD-PWM operation, it consists of (N-1)/2 number of carrier signals with dc bias of A_c, where A_c is amplitude of the carrier. A PD-PWM pulse for inverter-I (C) is generated from the comparison between rectified modulation waveform and carrier, while PD-PWM pulse for inverter-II (D) is generated from the comparison between rectified modulation waveform and carrier with dc bias of $+A_c$. The base PWM signals (A, B, C and D) for five-level hybrid PWM controller are shown in fig.4.

3.2 Hybrid PWM Controller

Hybrid PWM controller is implemented using a simple combinational logic, and hence, it can be processed very quickly. The functions of the combinational logic for a five level hybrid PWM are expressed as

$$S1 = A\,B\,C + \overline{A}\,B \qquad S1' = A\,B\,D + \overline{A}\,B$$
$$S2 = \overline{A}\,B\,C + \overline{A}\,\overline{B} \qquad S2' = \overline{A}\,B\,D + \overline{A}\,\overline{B}$$
$$S3 = \overline{A}\,\overline{B}\,C + A\,\overline{B} \qquad S3' = \overline{A}\,\overline{B}\,D + A\,\overline{B}$$
$$S4 = \overline{A}\,B\,C + A\,B \qquad S4' = \overline{A}\,B\,D + A\,B$$

and

where A is a sequential signal, B is a fundamental frequency PWM, C is a PD-PWM for inverter-I, and D is PD-PWM for inverter-II. In fig.5, it is shown that each gate signal is composed of both low frequency PWM and PD-PWM signals.

If sequential switching signal A=1, S1 and S2 in converter-I and S1' and S2' in converter-II are operated with PD-PWM while S3 and S4 in converter-I and S3', S4'in converter-II are operated at fundamental frequency. If sequential switching signal A=0, S1 and S2 in converter-I and S1' and S2' in converter-II are operated at fundamental frequency while S3 and S4 in converter-I and S3', S4'in converter-II are operated with PD-PWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress for four power switches in each inverter bridge is inherently equalized with this modulation.

4. Performance Analysis

4.1 Harmonics

The principle of Fourier decomposition is that any regular time varying waveform can be described by an infinite series of sinusoidal harmonic components [8]. For the hybrid phase disposition PWM applied to cascaded inverter, the harmonic solution of the inverter phase voltage is given by

$$V_{ph\_HPD} = K\,M\,V\cos(\omega_o t) +$$

$$\frac{8V}{\pi^2}\sum_{m=0}^{\infty}\{\frac{A_{m0}}{2m+1}\cos((2m+1)\omega_0 t\} +$$

$$\frac{4V}{\pi^2}\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\{\frac{A_{mn}}{2m+1}\cos((2m+1)\omega_c t + 2n\omega_o t\} +$$

$$\frac{V}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\{\frac{1}{m}J_{2n-1}(2\,k\,m\,\pi\,M)\cos((n-1)\pi)$$

$$\cos(2\,m\,\omega_c t + (2\,n-1)\omega_o t)\}$$

Where K is number of inverter modules, M is the modulation index, and V is supply voltage. For a justifiable comparison, a performance index namely weighted total harmonic distortion (WTHD) was chosen to evaluate the proposed technique. Weighted total harmonic distortion (WTHD) is superior to total harmonic distortion (THD) as a figure of merit for a non sinusoidal inverter waveform in which lower portion of the frequency spectrum is weighted heavily, accurately portraying the expected harmonic current of an inductive load [9].

The WTHD uses spectral weighting factor and it is defined by

$$WTHD = \frac{\sqrt{\sum_{n=2}^{100}(\frac{V_n}{n})^2}}{V_1}$$

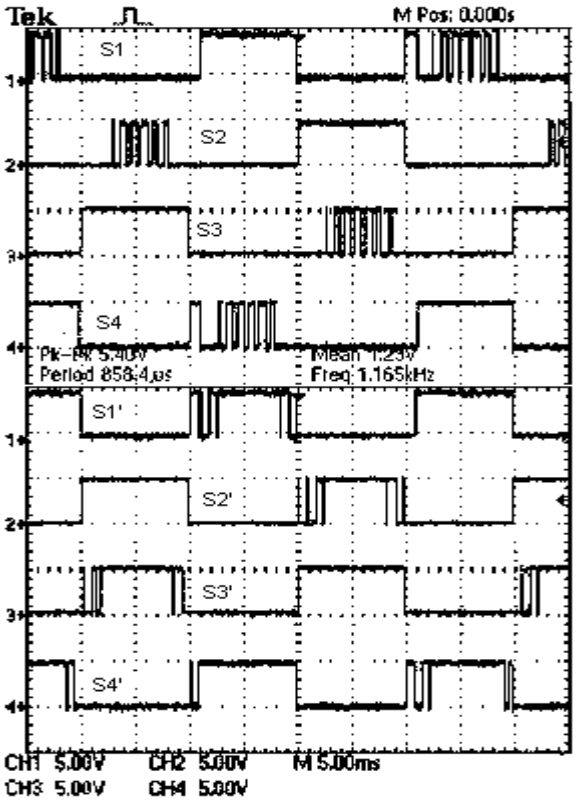


Fig.5. Hybrid Phase Disposition PWM signals for five-level Cascaded PV Inverter

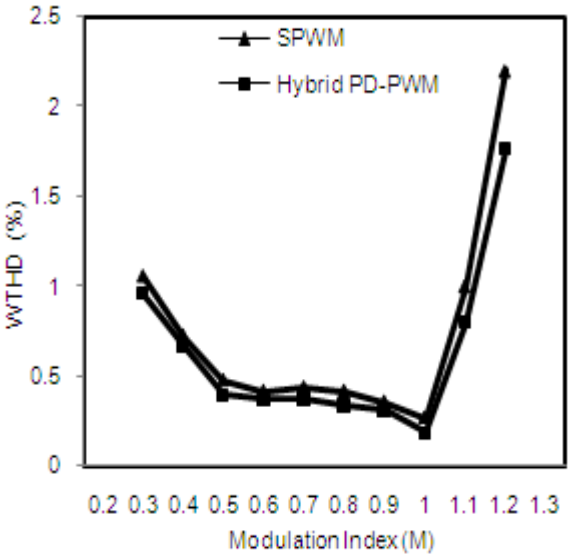


Fig.6.WTHD vs.Modulation index for five level cascaded photovoltaic inverter at carrier frequency fc=1050 hz

As shown in fig.6, WTHD measurement for the proposed hybrid phase disposition PWM technique is much lower when compared with that for the conventional SPWM operation. This proves that proposed inverter can reduce the WTHD which is an essential criterion for grid-connected PV systems.

4.2. Power Loss Comparison

Losses in power electronic converters can be classified in to four types, as 1) Conduction losses; 2) Switching losses; 3) Snubber losses; 4) OFF-state losses [12]. The last category is usually omitted, as these losses are insignificant. Snubbers are not usually required in converters made by insulated-gate bipolar transistors (IGBTs) [10].Thus, only conduction and switching losses are considered in this paper. MATLAB-SIMULINK model of a five level inverter has been developed to study the power loss. The carrier frequency f_c is 2 kHz and each converter cell is connected to 200 v dc supply. The IGBTs selected are FF150R12KT3G, in which their maximum ratings are a forward current of 150 A and a direct voltage of 600 V.

Switching losses are generated during the turn-on and turnoff switching processes of the power devices. In such processes, the voltages and currents can take significant values simultaneously. Therefore, their instantaneous power can reach high values. Fortunately, these processes only last for short periods, although they are repeated several times within a second. For this reason, they are directly related to the switching frequency. The average switching losses are calculated based on the information from the data sheet, turn on energy losses per pulse (Eon), turn off energy losses per pulse (Eoff) including reverse recovery loss and switching frequency $f_c = 1/T_c$.

$$P_{sw} = \frac{1}{2\pi T_c} \sum (Eon + Eoff)$$

The conduction power losses are those that occur while the semiconductor device is conducting current. The conduction losses of the transistors are obtained from the linearization of the static characteristics of the power switches. The model of the switches in the ON-state is represented by a voltage source and a series resistor. Consequently, the mean value of the conduction losses in a power device can be approximated by the following:

$$P_{cl} = \frac{1}{2\pi} \int_0^{2\pi} (V_{Fo} + i_F R_{on})\, i_F \, dt$$

in which V_{Fo} is the threshold voltage, R_{on} is the dynamic resistance of the model and i_F is the forward current in the device. The values were obtained by drawing a straight line tangent to the characteristic curves of the device, taking into account the current magnitude in this application. Fig.7 shows, for the full range of modulation index and the relative angle of the output currents, the ratio of total power losses (switching and conduction losses) for a five level inverter with the modulation strategy proposed in this paper versus the conventional PWM technique. Note that the surface is always below one, which means that the power losses are significantly smaller for the proposed modulation. The mean value of the surface is found 0.7326 approximately; which means the power loss reduction is about 26%. The best case is produced for a unity power factor and modulation index is one.

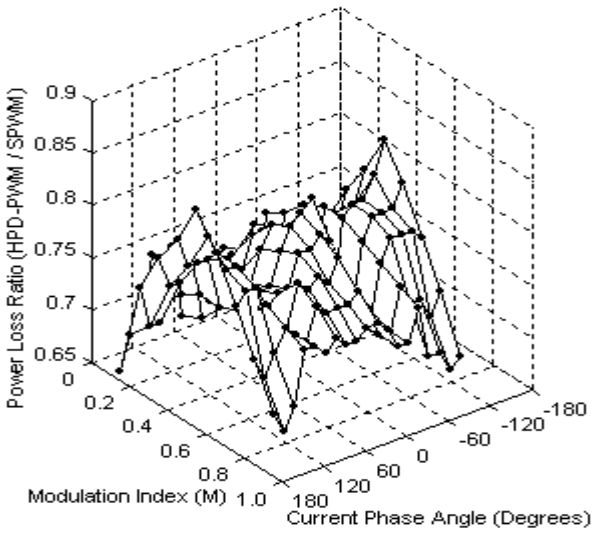


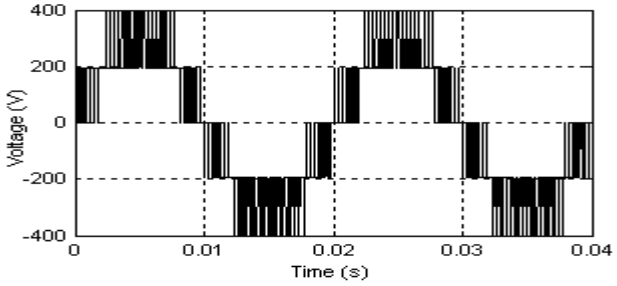
Fig.7 Ratio of the power losses of hybrid phase disposition PWM and conventional SPWM fed fivel level cascaded photvoltaic inverters.

5. Results and Discussion

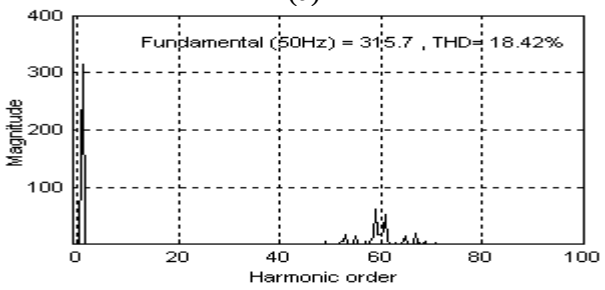
5.1. Simulation Results

In order to verify that the proposed inverter can be practically implemented in a photo voltaic system, simulations were performed by using MATLAB/SIMULINK. It also helps to confirm the PWM switching strategy which then can be implemented in a DSP. The dc-bus voltage is set at 200 V in order to inject current into the grid. The inverter should not operate with modulation index being less 0.5 because the current flow from the grid into the inverter, rather than the PV system injecting the current into the grid. Over modulation condition in the inverter operation makes a flat top at the peak of the positive and negative cycles because both the reference signals exceed the maximum amplitude of the carrier signal. This will cause grid current to have a flat portion at the peak of the sine waveform.

To optimize the power transferred from photo voltaic arrays in to grid, it is recommended to operate this inverter at the modulation index range of 0.5 to 1. The inverter output voltage and grid current for optimal operating conditions are shown in fig. 8 and 9, respectively. Fig 8(b) shows the harmonic spectrum inverter of output phase voltage waveform for a five level inverter in a linear modulation index and it injects very less harmonic to the grid. The grid current is almost pure sine wave and offers lesser THD as shown in fig.9.

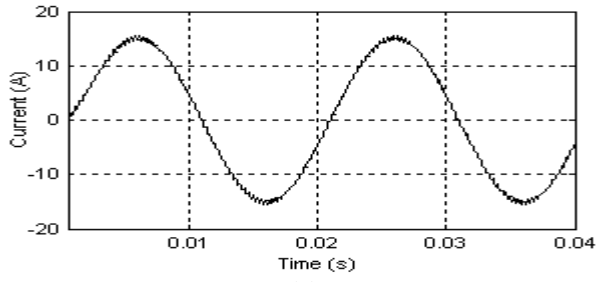


(a)



(b)

Fig.8 (a).Inverter output phase voltage waveform at M=0.8 and fc=3000 hz. (b).Harmonic Spectrurm of the output phase voltage.



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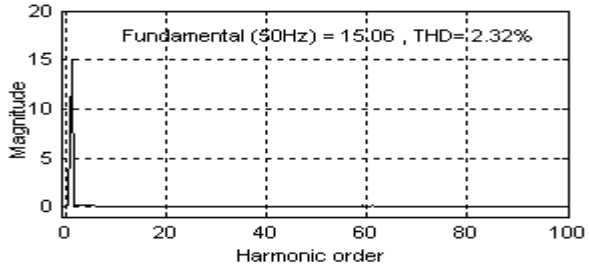


(b)

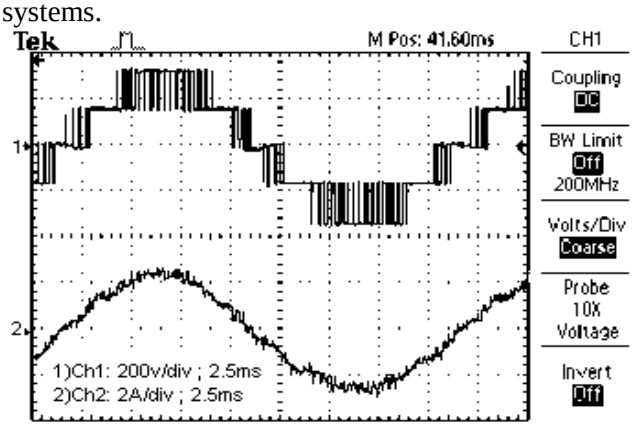
Fig.9 (a) Grid current waveform and (b) its Harmonic Spectrurm

5.2 Experimental Results

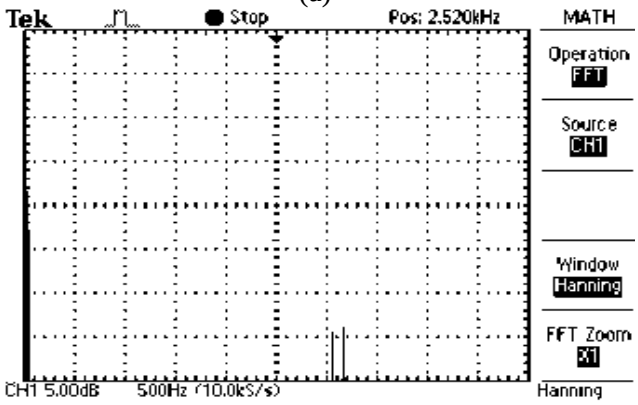
The simulations are verified experimentally by using low power prototype of a five level photovoltaic inverter. The fundamental frequency PWM and high frequency phase disposition PWM signals are generated using low cost high speed Texas instruments TMS320F2407 digital signal processor board with an accuracy of $20\,\mu s$. A sequential signal is also used a base PWM to operate each IGBT with low frequency and PD-PWM sequentially to equalize power losses, and heating among the devices. Xilinx CPLD XC95108 is used to develop the hybrid PWM control algorithm which suited for this application that has the features of better response for high frequency input signals, narrow pulse width pulses and no jitter of the delay in the circuit. The optically coupled isolators MCT2E are used to provide an electrical isolation between the Xilinx CPLD controller board and the power circuit. High voltage high speed insulated gate bipolar transistor drivers (IR2112) were used to provide proper and conditioned gate signals to the power switches. Digital real time oscilloscope (Tektronix TPS2024) was used to display and capture the output waveforms.

Fig. 10 shows the experimental results for inverter output voltage and grid current waveforms. It can be seen that inverter output voltage consists of five levels, and the grid current has been filtered to resemble a pure sine wave. The modulation index M is 0.8. For Modulation index M is less than 0.5, inverter output is less than grid voltage. Therefore, current will be injected from the grid into the PV system. This condition should be avoided to protect the PV system from damage. The modulation index is varied accordingly for the inverter to operate at minimum and maximum power conditions. Below the minimum power condition (during heavy clouds or nighttime) or above the maximum power condition (over rating of PV arrays which exceeds the rating of the inverter), the inverter should not operate to ensure the safety of the PV system and the environment. Efficiency measurement has been carried out to compare the efficiency of the proposed PWM inverter with that of a SPWM for PV application. The measured efficiency of a five level inverter with phase disposition modulation is approximately 96.8%, whereas that of the five-level SPWM inverter is only 82.1%. The results were taken at almost the same environmental conditions to ensure that grid current is similar to the measurement made for the five-level inverter.

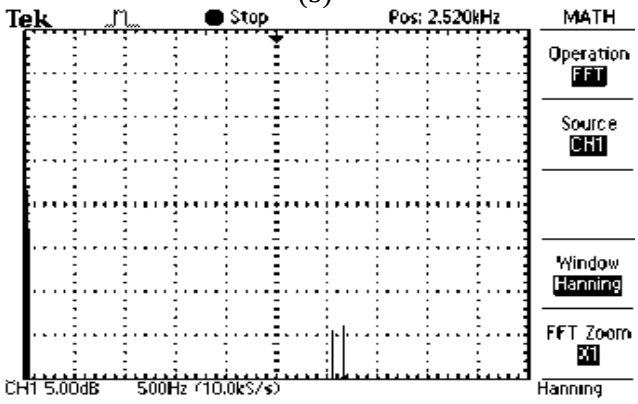
Simulation and experimental results show that the harmonic performance and efficiency improvement of the proposed inverter is better when compared to that of the conventional SPWM inverter, which is an important element for grid-connected PV systems.



(a)



(b)



(c)

Fig.10. Experimental results of Inverter operation for M=0.8, f_o =50 Hz, f_c =3000 Hz; (a) Inverter output voltage and grid current, (b) Spectrum of the output voltage, and (c) Spectrum of the grid current.

7. Conclusion

This paper has presented hybrid phase disposition PWM fed cascaded multilevel inverter for photovoltaic applications. Hybrid PWM control algorithm was developed with Xilinx CPLD controller and it is integrated with TMS320F2407 DSP processor for on-line hybrid PWM generation. A digital PI current control algorithm is also implemented in DSP processor to optimize the performance of the inverter. Experimental results indicate that harmonic performance of the proposed PV inverter is better than that of the conventional system. Furthermore, power loss reduction is about 26% by just modification of the modulation technique has been proven, which improves the efficiency of PV system. As a conclusion, the proposed topology with hybrid phase disposition modulation represents a valuable power conversion stage for grid connected PV systems.

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