Simulation Analysis of Direct Torque Controlled Three-Phase Induction Motor using a Three-Level Inverter

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Abstract: *Most researches focus on DTC using two-level inverters. This paper investigates the direct torque control (DTC) of a three-phase induction motor (IM) using a three-level (3L) neutral-point clamped (NPC) inverter. An analytical study is made to construct the switching table for the DTC with a three-level NPC inverter. A simulation model is implemented to compare the performance of the proposed DTC based on three-level inverter and the conventional DTC which uses the two-level (2L) inverter. The comparison includes speed performance, torque and flux ripples, voltage and current harmonics…etc. Also a simple balancing scheme is introduced to solve the inherent problem of neutral-point (NP) voltage deviation in the three-level NPC inverter. Simulation results are provided to confirm the advantages of using the three-level NPC inverter.*

Key words: *Direct torque control, three-level inverter, induction motor (IM)***,** *neutral point.*

1. Introduction

Direct torque control (DTC) has become strongly competitive to field-oriented control (FOC) in variable speed drives (VSDs). This is because DTC offers a lot of advantages such as: a fast torque response, simple control schemes, robustness against parameter variation, no need of current regulators [1-3].

Several kinds of DTC techniques have been devised so far and the most important of which are the classic switching-table DTC (ST-DTC), space vector modulation DTC (SVM-DTC) and discrete-SVM DTC (DSVM-DTC) [2]. ST-DTC represents the simplest type of DTC techniques since it requires no PWM modulator. On the other hand ST-DTC presents some drawbacks such as torque ripple and variable switching frequency.

Multilevel voltage source inverters (VSIs) have emerged for medium voltage and high power applications. They overcome the voltage and power limitations of two-level inverters and have attractive features over them [5-6].

The three-level neutral-point clamped (NPC) inverter has become increasingly used for medium voltage drives as well as being competitive to two-level inverters in low voltage drives. Most papers are related to DTC using two-level inverters (2L-DTC). A few has dealt with DTC using three-level inverters (3L-DTC). In this paper, the DTC system based on the three-level NPC inverter is modeled and simulated.

Section 2 gives an overview of the multilevel VSIs. In section 3 the space voltage vectors (SVVs) and switching states generated in 3L NPC inverter are shown, and the NP voltage problem is illustrated. Section 4 illustrates previous contributions of other authors to our work, the construction of the proposed DTC switching table, the devised method for solving the NP voltage problem and the overall block diagram of the proposed DTC system. Simulation results are given in section 5. Section 6 contains conclusions and the recommended future work.

2. Multilevel Inverter Topologies

Controlled ac drives in the megawatt range are usually connected to the medium voltage networks. It's hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a considerable interest in multilevel power electronic converters (PECs) was taken in the 1980s-1990s, in particular multilevel VSIs.

Fig. 1 shows a schematic diagram of one phase leg of inverter switch with different number of levels, for which the operation of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two levels as shown in Fig. 1 (a), while three-level inverter generates three levels and so on.

Three main topologies have been proposed for multilevel VSIs are: NPC, capacitor-clamped (flying capacitor), and cascaded H-bridge with separate dc sources. Several modulation and control strategies have been developed for multilevel inverters [5-7].

3. The Three-Level NPC Inverter

3.1 The Three-Level NPC Inverter Modeling

The three-level NPC inverter is the most widely used and investigated topology compared to other topologies, so it will be used in this paper. A three-level diode-clamped inverter is shown in Fig. 2.

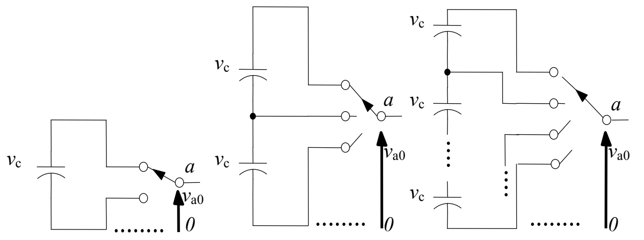

Fig. 1 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point n of the two capacitors can be defined as the neutral point. The output voltage v_{a0} for example has three states: V_{dc}, $V_{dc}/2$, and 0 neglecting R_a. A simple and sufficient model will be devised with the help of [8-9].

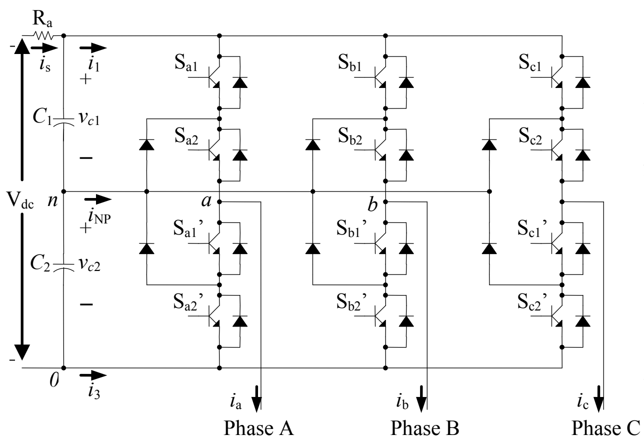

Fig. 2 The detailed three-level NPC inverter circuit

3.2 The Space Voltage Vectors (SVVs) of the Three-Level NPC Inverter

In contrast to the two-level inverter which has only 7 SVVs, 19 SVVs can be generated in the three-level NPC inverter as shown in Fig. 3. They can be classified into four categories:

1) One Zero-vector : V19 with magnitude of zero
2) Six Small-Vectors: V2, V5, V8, V11, V14 and V17 with magnitude of $V_{dc}/3$
3) Six Medium-Vectors: V3, V6, V9, V12, V15 and V18 with magnitude of $\sqrt{3}$Vdc/3
4) Six Large-Vectors: V1, V4, V7, V10, V13 and V16 with magnitude of 2Vdc/3

3.3 The Neutral Point (NP) Voltage Problem

The effect of the above SVVs on the NP voltage deviation is as follows:

1) Large and zero vectors have no effect on the NP voltage deviation due to the fact that there is no connection between the NP and inverter output phases. ($i_{NP} = 0$).

2) Small SVVs affect the NP. Fig. 4 shows that the same SVV V5 can be generated with two possible switching patterns (221) and (110). We have two cases:

- $i_c < 0$: In this case the (221) state causes C_1 to be discharged and C_2 to be charged [Fig. 4(a)]. The opposite effect occurs in Fig. 4(b) due to the state (110).

- $i_c \geq 0$: The effect of the witching states (221) and (110) is reversed. This means that each small SVV has two redundant states with opposite effects on the NP.

3) Medium SVVs affect the NP. Fig. 4(c) shows that V18 SVV is generated by the switching state (201). The effect of V18 on the NP depends on i_c direction.

From the above discussion, it's noted that the small SVVs can be used to solve the NP voltage deviation problem since a small SVV can be generated by two switching states with opposite effects on the NP voltage deviation.

4. DTC with the Three-level NPC Inverter

4.1 Previous Work

A few researchers were interested in DTC with the three-level NPC inverter. In developing the switching table for DTC in three-level inverters, the effect of each SVV on the torque and stator flux should be known so as to construct an accurate switching table. This was not shown in most researches [10], [15-17] and [21]. In our work a precise analytical study will be made to construct the switching table.

In [10], the authors used only 12 SVVs of the available 19 SVVs (zero and medium SVVs were not used). This neglects the benefit of the additional six medium SVVs generated by the three-level inverter.

In [13], an analytical study of the effect of SVVs on torque and flux was shown. The analysis shows that there are always more than one suitable SVV satisfying the torque and flux demands. This analysis neglects the effect of the stator resistance on flux. At low speed and heavy loads, the stator resistance causes a flux distortion and consequently an increase stator current harmonics [18].

The authors [13] have used the mentioned analysis in developing a DTC system with some degrees of freedom in the selection of the switching states which minimize the switching frequency [14]. Results for the torque, flux, voltage or current performance were not shown.

Most papers use multilevel hysteresis controller for torque control [10-12], [16], [21] which makes the controller and switching table more complex. In our work we will use a simple three-level torque controller.

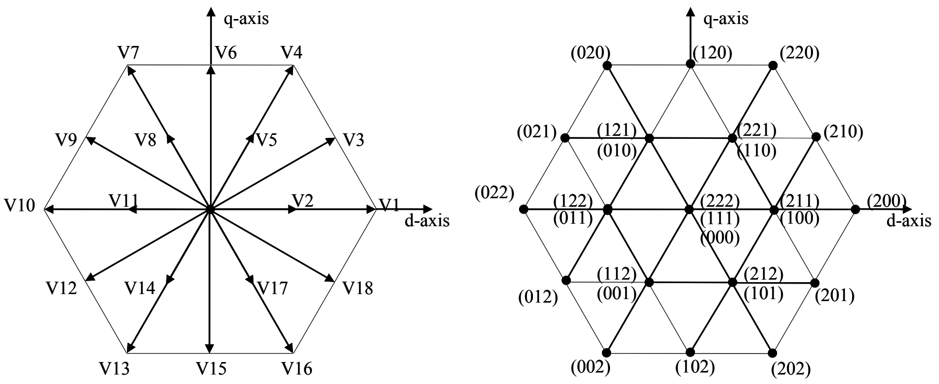

Fig. 3 (a) Voltage vectors, and (b) The switching pattern of a three-level inverter

Most researches [11-12], [14], [17], [21] do not show a comparison of 3L-DTC to the conventional 2L-DTC to verify their results.

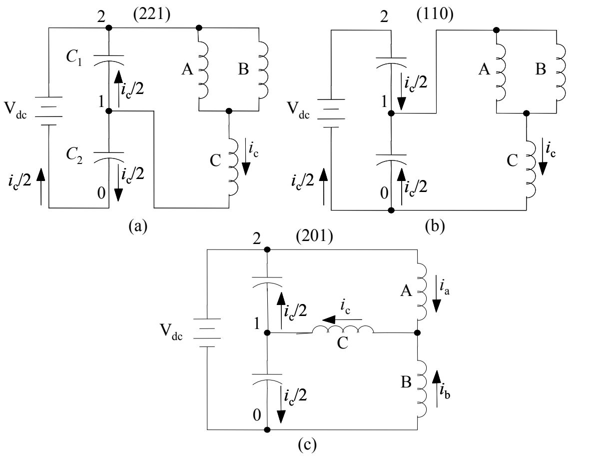

Fig. 4 Voltage unbalancing of the inverter capacitors

4.2 The proposed Method

This paper proposes a more precise analytical study with the help of analyses shown in [19-20]. It will be seen that the effect of SVVs on torque depends on the operating speed.

Fig. 5 shows the effect of the SVVs on stator flux and torque variation at $T_L = .9T_b$ and 1120 rpm ($0.4N_{rb}$) where T_b and N_{rb} are rated torque and speed of the motor with parameters shown in section 5. Based on this analysis, a switching table for SVVs can be deduced and it's shown in Table I. Note that the first sector for the conventional 2L-DTC is now divided into two sub-sectors: ($-30^o \sim 0^o$) and ($0^o \sim 30^o$).

Table I shows that according to the change of the effect of SVVs on the torque variation with speed, we can divide the DTC operation into three regions based on the reference speed Nref:

1) Region a ($H_T = 3$) : $N_{rb} \geq N_{ref} > 0.4N_{rb}$
2) Region b ($H_T = 2$) : $0.4N_{rb} \geq N_{ref} > 0.12N_{rb}$
3) Region c ($H_T = 1$) : $0.12N_{rb} \geq N_{ref} > 0$

The SVVs of H_T = -1 are used as torque reverse-affecting vectors. This will reduce the torque ripples as the results will show. In regions b and c, V18 is used instead of V17 in Table I. (B) since V17 causes flux drooping as shown in Fig. 5. The use of V18 will lead to lower harmonics in the stator currents.

TABLE I THE SWITCHING TABLE

(A) LOWER SUB-SECTOR

H_{phi}	H_v	H_T						
		3	2	1	0	-1	-2	-3
1	1	V4	V5$^+$	V3	V19	V17$^+$	V16	V15
	-1	V4	V5$^-$	V3	V19	V17$^-$	V16	V15
-1	1	V6	V7	V8$^+$	V19	V14$^+$	V12	V13
	-1	V6	V7	V8$^-$	V19	V14$^-$	V12	V13

(B) UPPER SUB-SECTOR

H_{phi}	H_v	H_T						
		3	2	1	0	-1	-2	-3
1	1	V6	V4	V5	V19	V17$^+$	V18	V16
	-1	V6	V4	V5	V19	V17$^-$	V18	V16
-1	1	V7	V8$^+$	V8$^+$	V19	V14$^+$	V13	V15
	-1	V7	V8$^-$	V8$^-$	V19	V14$^-$	V13	V15

4.3 The proposed NP balancing scheme

The NP voltage balancing scheme used in this paper is quite simple. It depends on the use of the small SVVs as mentioned before in section 3.3. To illustrate the scheme, suppose that the SVV V5 is currently selected by Table I to meet the torque and flux demands. A two-level hysteresis controller with output H_v (See Fig. 7) determines if the capacitor C_2 is overcharged or undercharged (Fig. 6). The final selection between (221) and (100) states of V5 will

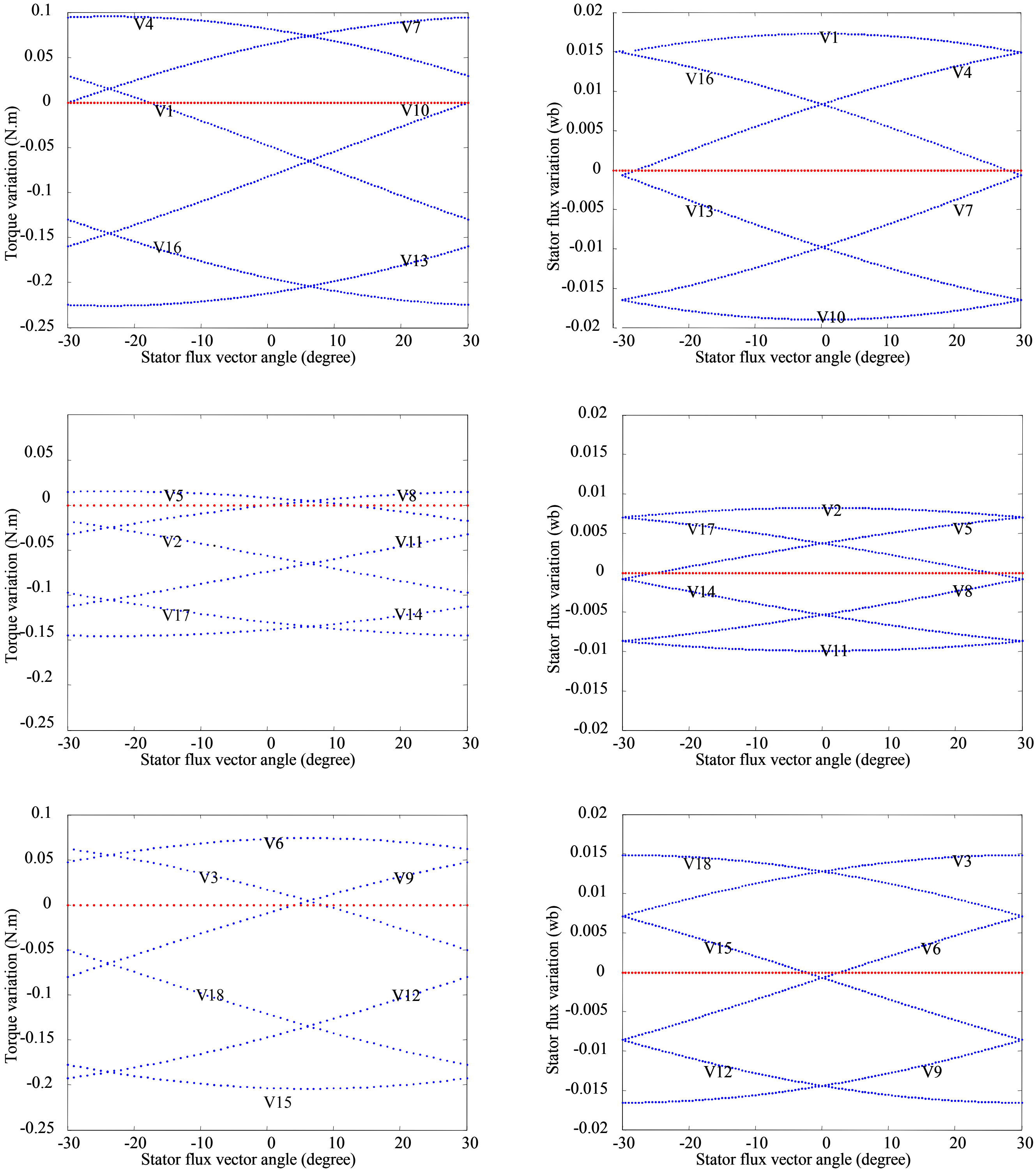

Fig. 5 The SVVs effect on the torque and stator flux variations in the first and second sub-sectors at T_L=.9T_b and 1120 rpm

depend on the sign of the phase current i_c to charge or discharge C_2 and keep v_{c2} within predetermined limits. The same action applies when any other small SVV is selected.

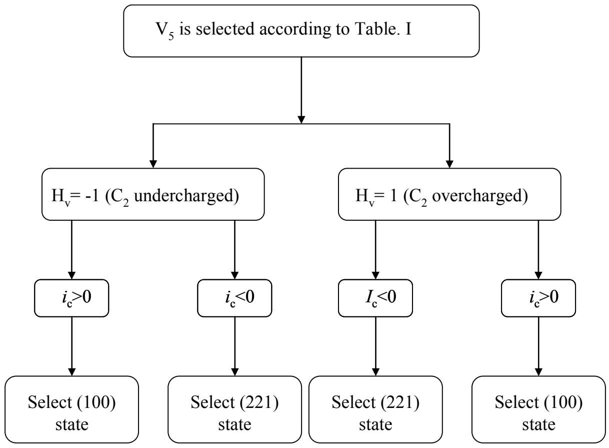

Fig. 6 Illustration of the proposed NP voltage balancing scheme assuming that V5 is currently

Fig. 7 shows the block diagram of the proposed DTC system. It can be noticed that it's identical to the conventional DTC for a two-level inverter with the exception of the additional two-level hysteresis controller required for the NP voltage balancing.

The inputs of the torque and flux estimator block are the capacitor C_2 voltage and two phase currents. The inputs of the switching-table block are the three hystersis controller outputs, the stator flux vector sector number and the sign of the stator currents. This block outputs the required SVV to the three-level NPC inverter.

5. Simulation and Results

The proposed DTC algorithm has been simulated in MATLAB-Simulink environment.

The DTC drive has been modeled (three-level inverter, three-phase IM, control algorithm, voltage balancing algorithm). The IM is Y-connected. Table II shows the parameters of the IM. Results are shown in Figs. 8, 9 and 10 and Table III.

5.1 Results at T_L = 3.3764(0.9T_b) and $N_{ref} = N_{rb}$ = 2800 rpm with Speed Reversal (H_T =3)

Speed reversal is performed at t = 1 s. Results show that: The speed response is nearly the same. A lower torque and flux ripple for the three-level DTC. During speed reversal, the stator current reaches 10 A in three-level DTC while it reaches 20 A in two-level DTC. In three-level DTC, THD for line and phase voltages is lower while THD for the stator current is higher. The NP voltage balancing technique is efficient.

5.2 Results at T_L = 3.3764 (0.9T_b) and N_{ref} = .35N_{rb} = 980 rpm (H_T =2)

The speed response is nearly the same. A lower torque and flux ripple for the three-level DTC. In three-level DTC, THD for line and phase voltages and the stator current is lower than two-level. The NP voltage balancing technique is also efficient.

TABLE II MOTOR PARAMETERS

Rated power Prated [kW]	1.1
Rated phase voltage [V]	220
Rated frequency [Hz]	50
Pole-pairs	1
Stator resistance R_s [Ω]	6.667
Stator inductance L_s [H]	0.4307
Rotor resistance R_r [Ω]	6.782
Rotor inductance L_r [H]	0.4307
Magnetizing inductance L_m [H]	0.4101
Moment of inertia J [Kg·m2]	0.005

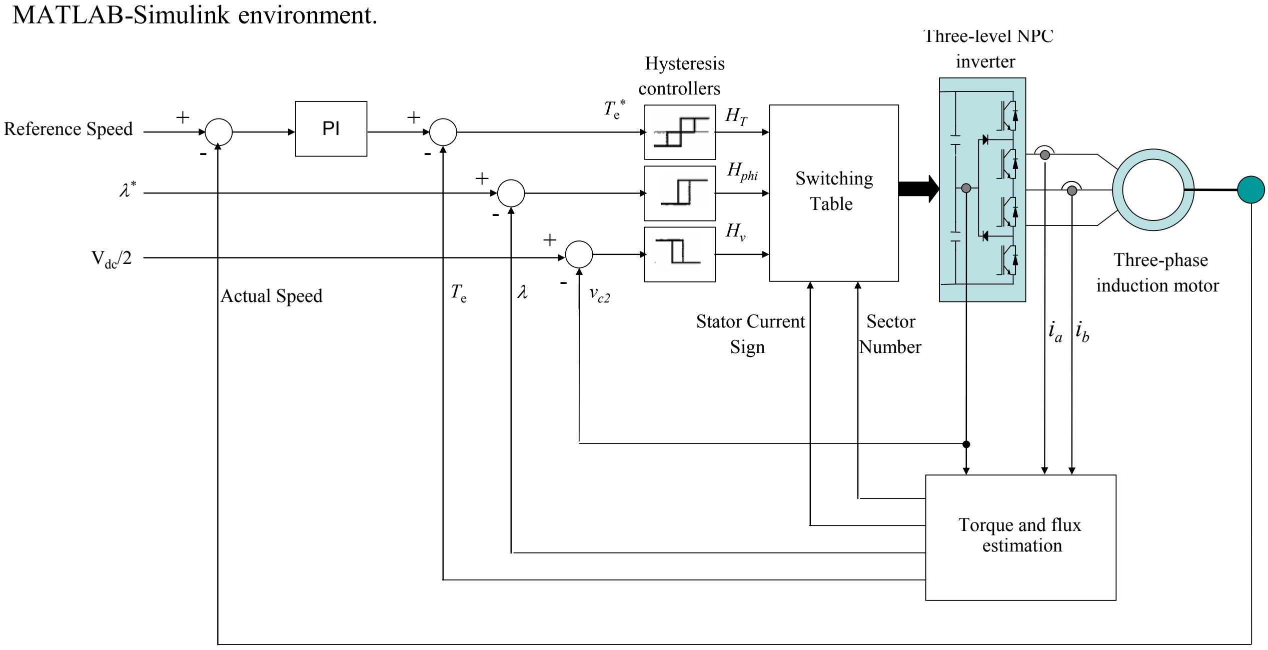

Fig. 7 Block diagram of the proposed three-level DTC

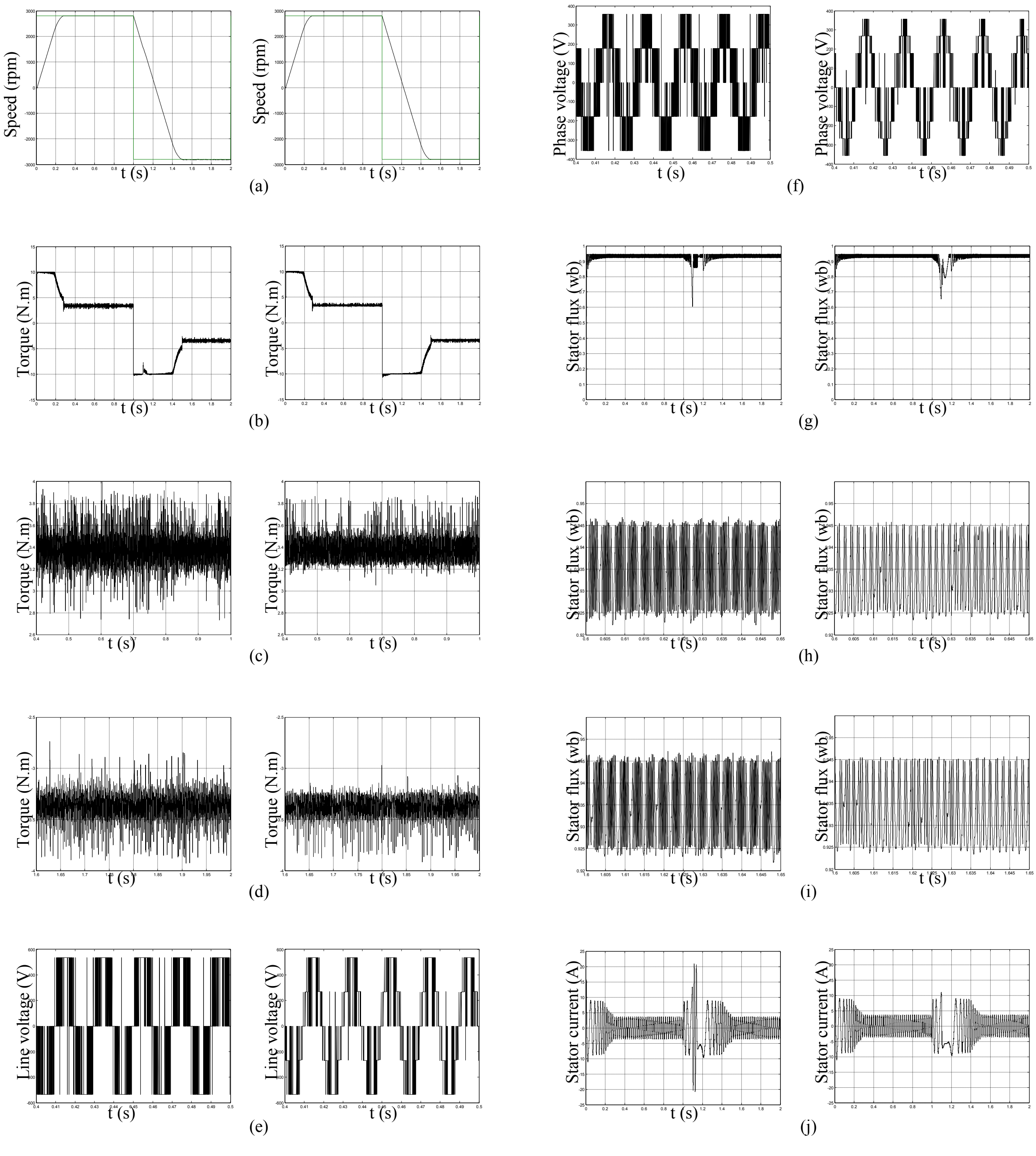

Fig. 8 Case A. results for (a) Speed response, (b) torque response, (c) a zoom on torque (forward direction), (d) a zoom on torque (backward direction), (e) line voltage, (f) phase voltage, (g) stator flux, (h) a zoom on stator flux (forward direction), (i) a zoom on stator flux (backward direction) and (j) stator current. Left: two-level and Right: three-level

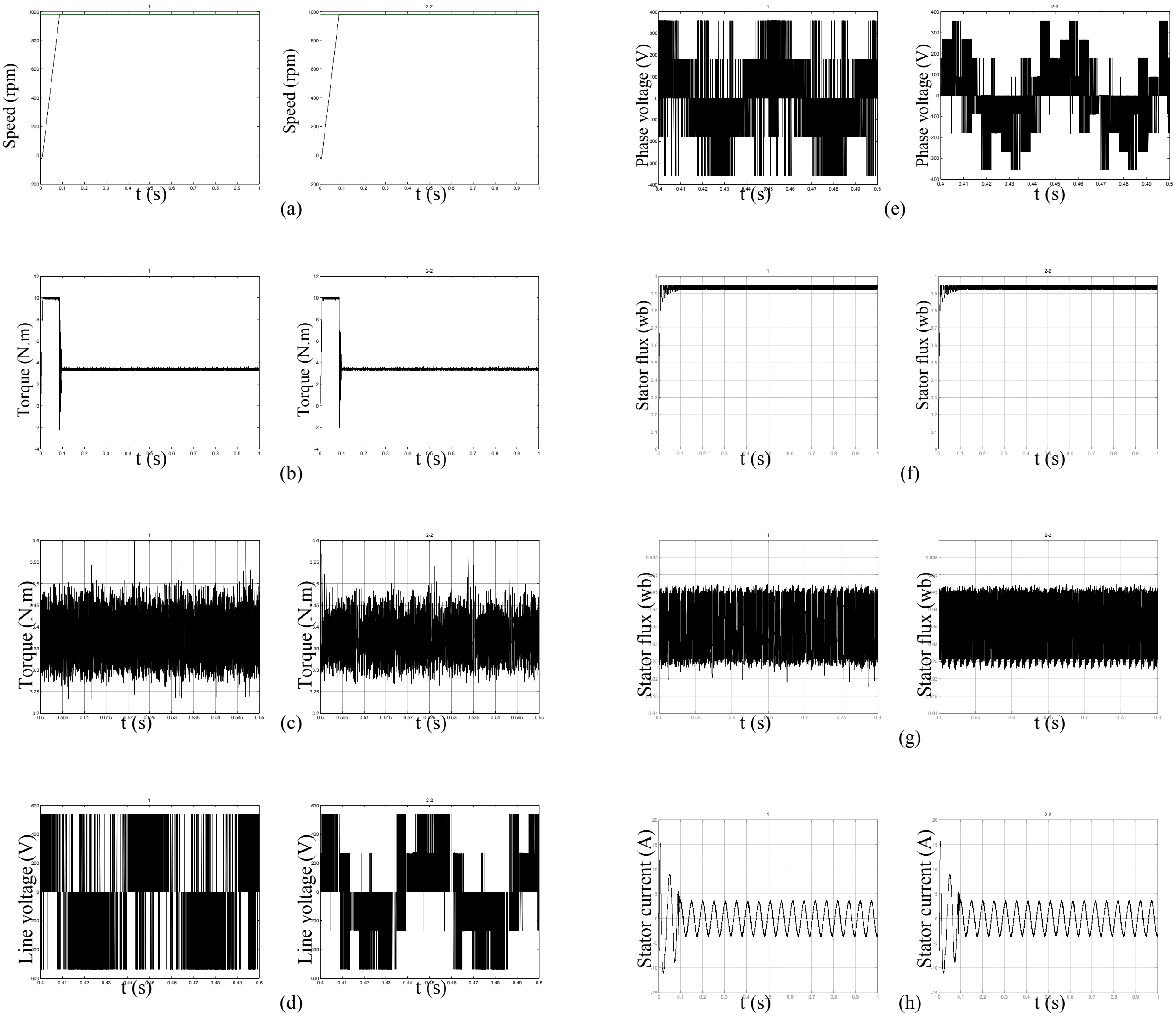

Fig. 9 Case B. results for (a) Speed response, (b) torque response, (c) a zoom on torque, (d) line voltage, (e) phase voltage, (f) stator flux, (g) a zoom on stator flux and (h) stator current. Left: two-level and Right: three-level

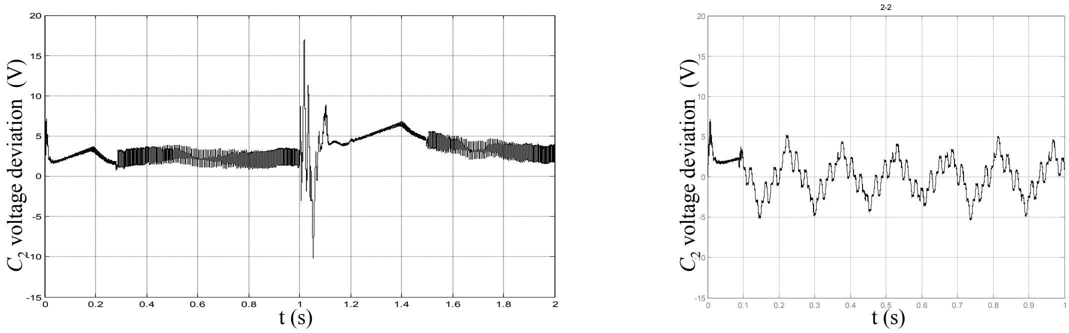

Fig. 10 C_2 voltage deviation of three- level DTC for (a) Case A, (b) Case B

TABLE III THD% for Line and Phase Voltage, and Stator Current; (A) Case A and (B) Case B

(A)

	i_a	v_{AB}	v_{AN}
2-Level	2.27	17.67	17.50
3-Level	2.54	10.06	10

(B)

	i_a	v_{AB}	v_{AN}
2-Level	1.72	49.81	49.69
3-Level	1.49	42.99	41.24

6 Conclusions

In this paper a new 3L-DTC NPC inverter was presented. The effect of SVVs on torque and flux variations was analyzed to select the appropriate SVV. The proposed system is similar to the conventional 2L ST-DTC. The difference is the additional two-level hysteresis controller for the NP voltage balancing.

The proposed method constructs a novel switching table with three regions based on the operating speed of the motor. Simulations verify that torque and flux ripples, voltage THD, and stator-current limitation during speed reversal are improved in the proposed DTC compared to the 2L DTC. The stator current THD is noticed to be higher in the proposed system in case A., but it becomes lower in case B.

The real-time implementation of the proposed work is now done to verify the simulation results. As a future work, it is recommended to apply the analytical analysis on higher-level inverters such as the four- and the five-level inverters.

References

[1] Takahashi I., Noguchi T.: *A new quick-response and high efficiency control strategy of an induction machine*. In: IEEE Trans. Ind. Applicat., (1986), Vol. IA-22, Sept./Oct. 1986, p. 820-827 .

[2] Baader U., Depenbrock M., Gierse G.: *Direct self control (DSC) of inverter-fed-induction machine—A basis for speed control without speed measurement*. In: IEEE Trans. Ind. Applicat., (1992), Vol. 28, May/June 1992, p. 581-588.

[3] Buja G. S., Kazmierkowski M. P.: *Direct torque control of PWM inverter-fed AC motors-a survey*. In: IEEE Trans. Ind. Electron, (2004), Vol. 51, August 2004, p. 744-757,

[4] Buja G., Casadei D., Serra G.: *DTC-based strategies for induction motor drives*. In: Proceedings of the IECON, New Orleans, Nov. 9-14, 1997, Vol. 4, p. 1506-1516.

[5] Lai J. S., Peng F. Z.: *Multilevel converters–a new breed of power converters*. In: IEEE Trans. Ind. Applicat., (1996), Vol. 32, May/June 1996, p. 509–517.

[6] Rodriguez J., Lai J. S., Peng F. Z.: *Multilevel inverters: a survey of topologies, controls, and applications*. In: IEEE Trans. Ind. Electron., (2002), Vol. 49, August 2002, p. 724-738.

[7] Muhammad H. R.: *Power Electronics Handbook*, Academic Press, 2006.

[8] Kanchan R. S., Tekwani P. N., Gopakumar K.: *Three-level inverter scheme with common mode voltage elimination and DC link capacitor voltage balancing for an open-end winding induction motor drive*. In: IEEE Trans. Power Electronics, (2006), Vol. 21, Nov. 2006, p. 1676-1683.

[9] Sinha G., Lipo T. A.: *A four-level inverter based drive with a passive front end*. In: IEEE Trans. Power Electronics, (2000), Vol.15, Mars 2000, p. 285-294.

[10] Cirrincione M., Pucci M., Vitale G.: *A novel direct torque control of an induction motor drive with a three-level inverter*. In: Proceedings of the Power Tech Conference, Bologna, June 23-26, 2003, Vol. 3.

[11] Cirrincione M., Pucci M., Scordato G., Vitale, G. : *A low-cost three-level converter for low-power electrical drives with induction motor applied to direct torque control*. In: Proceedings of the Power Electronics Specialists Conference, Aachen, June 20-25, 2004, Vol. 6, p. 4571-4577.

[12] Cirrincione M. , Pucci M., Vitale G.: *Direct torque control for three-level fed induction motor drives with capacitor voltage ripple minimization*. In: Proceedings of the IECON, Orlando, No. 10-13, 2008, p. 3238-3245.

[13] Gharakhani A., Radan A.: *Analytical study of affecting characteristic of voltage vectors of a three-level NPC inverter on torque and flux of DTC controlled drives*. In: Proceedings of the International Electric Machines & Drives Conference, Antalya, May 3-5, 2007, Vol. 1, p. 754-759.

[14] Gharakhani A., Radan A.: *A novel strategy for minimizing the variation of neutral point voltage and switching frequency in DTC controlled, NPC driven induction motors*. In: Proceedings of the International Electric Machines & Drives Conference, Antalya, May 3-5, 2007, Vol. 1, p. 748-753.

[15] Zhang Y. , Zhao Z., Zhu J., Xu W., Dorrell D. G.*: Speed sensorless direct torque control of 3-level inverter-fed induction motor drive based on optimized switching table*. In: Proceedings of the IECON, Porto, Nov. 3-5, 2009, p. 1316-1321.

[16] Sadeghi Larijani A., Shahparasti M., Fatemi A., Amiri A., Mohammadian M.: *DTC drive of induction motor using three-level inverters with optimized switching table and minimizing the deviation of neutral point voltage*. In: Proceedings of the PEDSTC, Tehran, Iran , Feb. 17-18, 2010, p. 255-260.

[17] Tan Z., Li Y., Li M. : *A direct torque control of induction motor based on three-level NPC inverter*. In: Proceedings of the PESC, Vancouver, BC, June 17-21, 2001, Vol. 3, p. 1435-1439.

[18] Mei C.G. , Panda S.K., Xu J.X., Lim K.W.: *Direct torque control of induction motor - variable switching sectors*. In: Proceedings of the PEDS Conference, Hong Kong, July 27-29, 1999, Vol. 1, p. 80-85.

[19] Buja G., Casadei D., Serra G.: *Direct stator flux and torque control of an induction motor: theoretical analysis, and experimental results*. In: Proceedings of the IECON Conference, Aachen, Aug. 31-Sep. 4, 1998, Vol. 1, p. T50 - T64.

[20] Bertoluzzo M., Buja G., Menis R.: *Analytical formulation of the direct control of induction motor drives*. In: Proceedings of the ISIE Symposium, Bled, July 12-16, 1999, Vol. 1, p. PS14-PS20.

[21] Alloui H., Berkani A., Rezine H.: *A three level NPC inverter with neutral point voltage balancing for induction motors direct torque control*. In: Proceedings of the ISIE Symposium, Rome, Sept. 6-8, 2010, p. 1-6.