CMOS Eight-Transistor Memory Cell for Low-Power High-speed Embedded SRAM

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Abstract- With Migration towards low supply voltages in low-noise embedded SRAM designs, low-power, high-speed, and small physical cell area become more essential in VLSI devices. This necessitates sharing of power supplies and substrates with sensitive digital and analogue circuitry, which have large impacts on timing and power specifications of SRAM's performance. A CMOS eight-transistor (8T) memory cell circuit for single and multi-port SRAM is proposed. The cell is based on the traditional cross-coupled invertors, but with an addition of two NMOS transistors for read buffer circuit. The read buffer structure is based on pre-charging the read bit-line during the low value of read clock and evaluating the read bit-line during the high value of read clock. This eliminates the use of sense amplifier with all its synchronization schemes (i.e. self-timing), which exploits a cost-effective of overhead circuitry, and more important reduces the power consumption. Consequently, the 8T cell memory of sizes less than 5k-bit storage capacity has smaller total silicon area than six-transistor (6T) cell

memory with the same storage capacity by a rate of 6%, while it is larger by a rate of 13% otherwise.

Furthermore, the cell contributes to the operation both at high speed and at low power supply voltage with a comparable silicon size of 14% larger than 6T SRAM cell. The simulation results show that, the embedded SRAM of size 128-bit X 128-bit is operating at a maximum frequency of 200 MHz for Write/Read clock cycle at 1.62 V power supply, and measures a total average power dissipation of 0.180 mW. All simulation results were conducted on 0.18 µm TSMC single poly and three layers of metals measuring a cell area of 3.2*3.75 μm^2.

Index Terms- Embedded SRAM, Local SRAM, 8T cell, 6T cell, 0.18 µm, low voltage power supply, self-timing.

I. INTRODUCTION

Embedded memory components have become widely attractive of the embedded processor market which are integrated with million of gates into CMOS ASIC's applications in order to deliver most of the performance at a lower fraction of price. In addition to the cost, low-power consumption and high-density CMOS static RAM with high speed have been widely used and demanded for high-performance graphics and small systems. Hence, with a rapid advancement in deep submicron technologies, memory devices are considered bound to processor performance which has been referred

to as memory wall [15], [22], [5] due to the increased in high speed operation to the field of CPU application. Furthermore, a significant large density memory with an integration of large number of gates is considered power consumption limit on a VLSI chip due to its high capacitance busses, frequently accessed, and I/O interfaced buffer with standby sensing amp current.

Consequently, several design techniques have been proposed for low supply and low power embedded SRAM [6], [9], [11], [12], [13], [14], [17], [23] where many cells have been developed to reduce the power consumption by operating at low voltages and have fast access time. However, most of these attempts suffer with very large cell size compare to basic 6T SRAM [4], [10], [20], or they required a high cost of overhead circuitry in the I/O buffer. To realize fast access time, low power supply voltage, and small silicon area of memory cell with relatively no cost of overhead I/O, a CMOS 8T cell has been proposed.

In this brief, the new 8T cell structure is described which is combined a conventional 6T cell for write access only and two NMOS transistors for read buffer output. The read buffer output uses one NMOS transistor for discharging or keeping the charge at the output read bit-line depending on the stored bit value, while the other NMOS transistor is used for selecting the row read address line. On the other hand, the cell can be extended for multi-port output by adding more read buffers to the core cell.

In this paper, the details of the proposed memory cell are introduced and their advantages are discussed. Then, a complete memory structure based on 8T cell is presented with all supporting circuitry in next section. Experimental results of storage size128-bit X 128-bit embedded SRAM, which is implemented as a local memory in

SAVAGEXP [25] product, are illustrated in farther section. Conclusion is given in the last section.

II. CMOS 8T CELL

A. Cell Structure

The author patent given in Fig. 1 [19] is a representation of 8T cell which are optimized at the standard supply voltage in order to realize both at high speed and at low supply voltage with least silicon area. A conventional CMOS 6T cross coupled invertors is employed for write operation due to its stability, compact, and more reliable than any other regenerative circuit [3], [7], [18]. In addition to 6T cell, two NMOS transistors are used for read operations. Such that, N1 is used to discharge the read bit-line (RBL) which was selected by Read Word-line (RWL) through N2 for stored logic "0" at the cell. For stored logic "1" at the cell, N1 is kept off and the RBL is kept pre-charge to maximum power supply voltage, even though, it was selected by RWL since the discharge path through N1 is off. A minor constraint requires that, the RBL loading capacitances is higher than intermediate capacitance between N1 and N2 in order to avoid voltage drop during the evaluated logic "1" of the selected cell. This constraint is already existed in nature of the design since the RBL loading capacitances is much larger than the cell capacitance between the diffusion of N1 and N2. Thus, the voltage drop is much less than the order of mV.

Consequently, the read bit-line level swings full rail between the supply voltage level and ground level which meet the requirement for low power consumption through low supply voltage level operation. This eliminates the use of sensing amps, standby sensing current, and differential bit line adjusting circuit. Hence, the proposed cell

minimizes the overall memory component overhead, in contrast to other cell structures [1], [2], [8], [16], [7]. Furthermore, the cell can be extended for multi-port output as predicted in Fig. 1(b), where each output has its won read buffer transistors.

B. Cell Layout

The layout of the presented 8T memory cell is drawn in Fig. 2 with actual drawn transistor sizes. The cell is designed based on a 0.18 µm single poly and three layer of metals CMOS n-well technology [24]. The total of approximate size of the cell is 3.2 X 3.75 μm^2, in contrast to the size of 6T cell on the same technology 3.2 X 3.2 μm^2. Since there are no PMOS transistor in read buffer portion, the total cell area leads to a better layout arrangement and smaller layout area, which about 14% larger than the 6T cell. In addition, the two NMOS read transistors provide enough and fast conducting capability in a frequency range of 200 MHz for the memory size of 64k-bit embedded local SRAM.

Notice that the sizes of transistors in the write portion of the cell are only optimized for the write operation since the read operation uses different portion of the cell. This makes the 6T write portion of the 8T cell is smaller than the conventional 6T SRAM cell [5], [13], [15], [22] of about 6%, which implies that the presented cell area is only larger than the 6T cell of about 14%. Moreover, the separation between write and read circuitry of the 8T cell provides higher noise margin, eliminates soft error coupling effects [4], [5], [9], [11], [13], [14], [15], [22], [23] and insensitive to simultaneous read and writes coupling mechanisms. These advantages are very attractive in local embedded SRAM design since the layout of the chip allows routing above memory components for certain busses.

III. 8T CELL IN EMBEDDED MEMORY ARCHITECTURE

A. Write/Read Pre-decoder/Decoder Circuit

Write address bus is streamlined by a simple combinatorial logic of pre-decoder and decoder circuit [1], [2], [8] which meets a timing specification between write clock, address, and data (i.e. setup, hold, and accesses) as clearly shown in Fig. 3(a). On the other hand read address bus is formed by low power latches [21] with an addition of standard pre-decoder and decoder circuit as shown in Fig. 3(b)-(c). During the low-level (pre-charge phase) of read clock, the read address is stored through a read latch. While during the high-level of read clock (evaluate phase), the read address is evaluated and the RWL value is decoded. The Write/Read Pre-decoder and Decoder circuits of 8T cell are about the same in geometry for the 6T cell; there is no silicon area advantage in this portion of the memory.

B. I/O Buffer Circuit

In order to realize a pre-charge mechanism on read bit-line, the I/O buffer circuit shown in Fig. 4 is implemented for every column which is analogous to sensing amps circuit in 6T cell. The PMOS (P1) transistor is used to pre-charge the RBL with the falling edge of read clock, while the output latch hold the previous outcome. During the rising edge of the clock, the P1 transistor is disabled and the output latch update the current outcome at the RBL. A few concerns on timing criteria between P1, output latch, and RWL need to have a careful synchronization (as explained next) in order to optimize the power dissipation reduction and provide high speed read access with reliable outcome. This timing synchronization is simply accomplished through the use of *INV1*, *INV2*, and *INV3*. An external buffer (*BUFFER*) is added at RCLK line for every I/O

buffer in order to provide an external adjustment on the timing and reduced the load capacitance on the distributed RCLK line.

C. Timing Chain for Read Operation

Separation of write circuitry from read circuitry implies higher noise margin operation with simple timing chain, where write and read signals in the memory cell can access independently. Since write operation is analogues to 6T cell traditional approach [6], [9], [11], [12], [13], [14], [23] we focus our explanation on a read mechanism as illustrated in Fig. 5. The decoded row cells selected by RWL are disabled before RCLK enable the pre-charge on RBL by some duration time (T_p). Following the same arguments, disabling pre-charge is conceived before enabling the row cells by T_p. This timing sequence is recommended in order to prevent any direct path between power supply conducted by P1 through RBL and ground through the read buffer cell. Hence, any static power dissipation is reduced if not eliminated.

Moreover, the latch output circuit is disabled before pre-charge is conducted on RBL, and the output latch is enabled after the pre-charge is disabled on RBL by duration of T_h. This holding time mechanism is to ensure that the output latch does not allow any pre-charge value to sneak in during pre-charge phase. Furthermore, avoid any small contention between output latch and cell read buffer during evaluate phase in order to optimize the speed of read access.

Last, it is worthwhile to mention that all timing adjustment involve in the read operation are simply inherited in a pre-decoder/decoder and I/O latch circuitry with a careful selecting sizes of transistors. Hence, the read operation is self-timing adjustment without the use of controller or special sequential circuit.

IV. SIMULATION and RESULT

S3.incoroprated released the commercial product SAVAGEXP [25] in year 2000 based on a 0.18 µm TSMC single-poly and six layer of metal CMOS technology [24] which operated at clock cycle of 200 MHz. All different geometries of embedded memories within the product are laid out based on single-poly and three layers of metals in order to provide enough silicon area for top-level routing. In addition, all embedded memories including first and second level caches are implemented based on our proposed 8T cell architecture supported by a general design patent [19].

In this brief, we choose to present the post-layout simulation of 128-bit X 128-bit embedded SRAM including all parasitic modeling layout values. The simulation is conducted by HSPICE simulator based on the RC-extracted net-list given in Fig. 6 for worst case cells under-test, when the supply voltage is 1.62-1.8 V, temperature is 0-125 °C, and operating frequency is set to 200 MHz. Fig. 7 shows the complete memory waveform; such that, the read clock signal (RCLK) is given in Fig. 6, cell stored value (CELL_VALUE) is given in Fig. 1(a), row cells read word line (RWL_CELL) is given in Fig. 1, Pre-charge read bit line (RBL_IOBUFF) is given in Fig. 4, Pre-charge read clock control line (RCL_IOBUFF) is given in Fig. 4, and final output buffer result (READOUT) is given in Fig. 4. As we observe that the input data written into the memory cell is read out correctly and the memory is functioning correctly for all process corners. Moreover, we observe that the final output buffer (READOUT) has a constant glitches (i.e. high to low spike) at the rising edge of RCLK. This is due to the pre-charge voltage at the RBL_IOBUFF during the evaluate phase in which the voltage sneaks

partially to output buffer, and then, the buffer corrects itself based on the cell stored value.

The worst case output delay using HSPICE RC-extracted net-list is measured to be 2.11ns as shown in Fig. 7 which implied that the memory component can further operates at 250 MHz. In addition, the worst case power consumption was reported to be 0.180 mW at a fast process corner (i.e. power supply 1.98V and Temperature 0 C), where Fig. 8 shows a comparisons of maximum power consumption at different operating frequencies between 6T and 8T memory cells structures. This topology shows that using 8T cell structure in embedded system reduces the power consumption by an average rate of 30% over 6T cell memory topology of the same size.

On the other hand, the silicon cost of 8T cell memory structure is less at sizes below 5k-bit than the 6T cell embedded memory by a rate of 6%, while it is larger otherwise as predicted in Fig. 9 by a rate of 13%. This is due to the larger layout size of the 8T cell over 6T cell from one side vs. the extra silicon area of the synchronization circuitry of the 6T cell memory over the 8T cell memory on the other side.

V. CONCLUSION

A CMOS 8T memory cell for substantial low-power consumption, low supply voltage operation, and comparable high dense embedded SRAM with fast operating frequency is proposed. The cell has a total geometry silicon area of 3.2 X 3.75 μm^2, where it provides an increase of 14% over 6T cell based on 0.18µm single-poly CMOS technology. However, the 8T cell topology in embedded SRAM eliminates the synchronization circuitry and timing controller required for 6T cell memory structure. This provides an overall area advantage of about 6% rate for 8T cell memory less than 5k-bit in storage size.

The separation of write and read circuitry of the cell precludes the soft error coupling mismatch between read and write operation, and provides higher noise margin which make it suitable for low power supply voltage. In addition, it allows flexibility of floor plan routing through using multi-layers of metals, where some metal busses allow passing over embedded memory.

Finally, the main clear advantage of the proposed 8T cell is the reduction of power consumption in embedded systems, where they are very limited with total consumption power. The power consumption shows a rate change advantage of about 30% than counterpart 6T memory of sizes ranges between 1k-bit to 500k-bit at operating frequencies ranges between 50 MHz to 250MHz. This reduction of power is mainly due to the elimination of using sensing amplifier at the I/O stage with all its synchronization circuits used in 6T cell memory structure. The I/O buffer in the proposed 8T cell is basically a simple latch with pre-charge PMOS for Read Bit line with no standby current requirements.

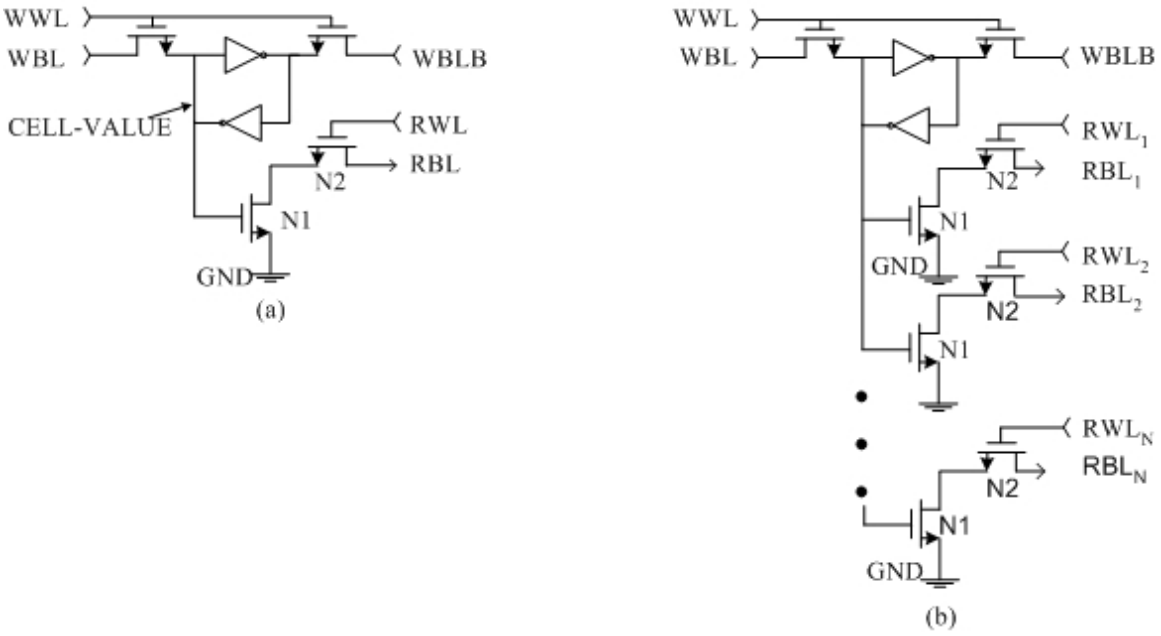

Fig. 1. 8T CMOS cell [1] (a) Single-read port (b) Multi-Read Port.

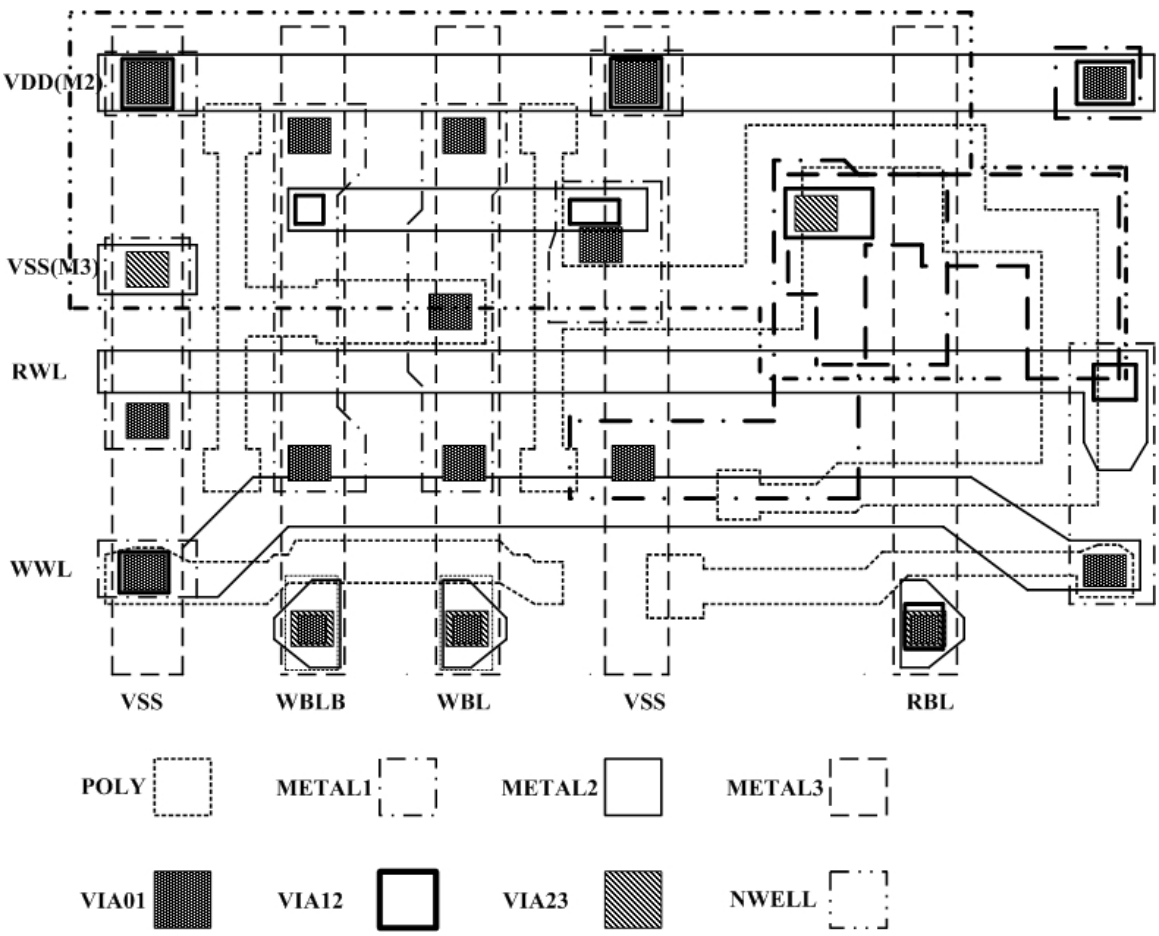

Fig. 2. 8T cell CMOS layout.

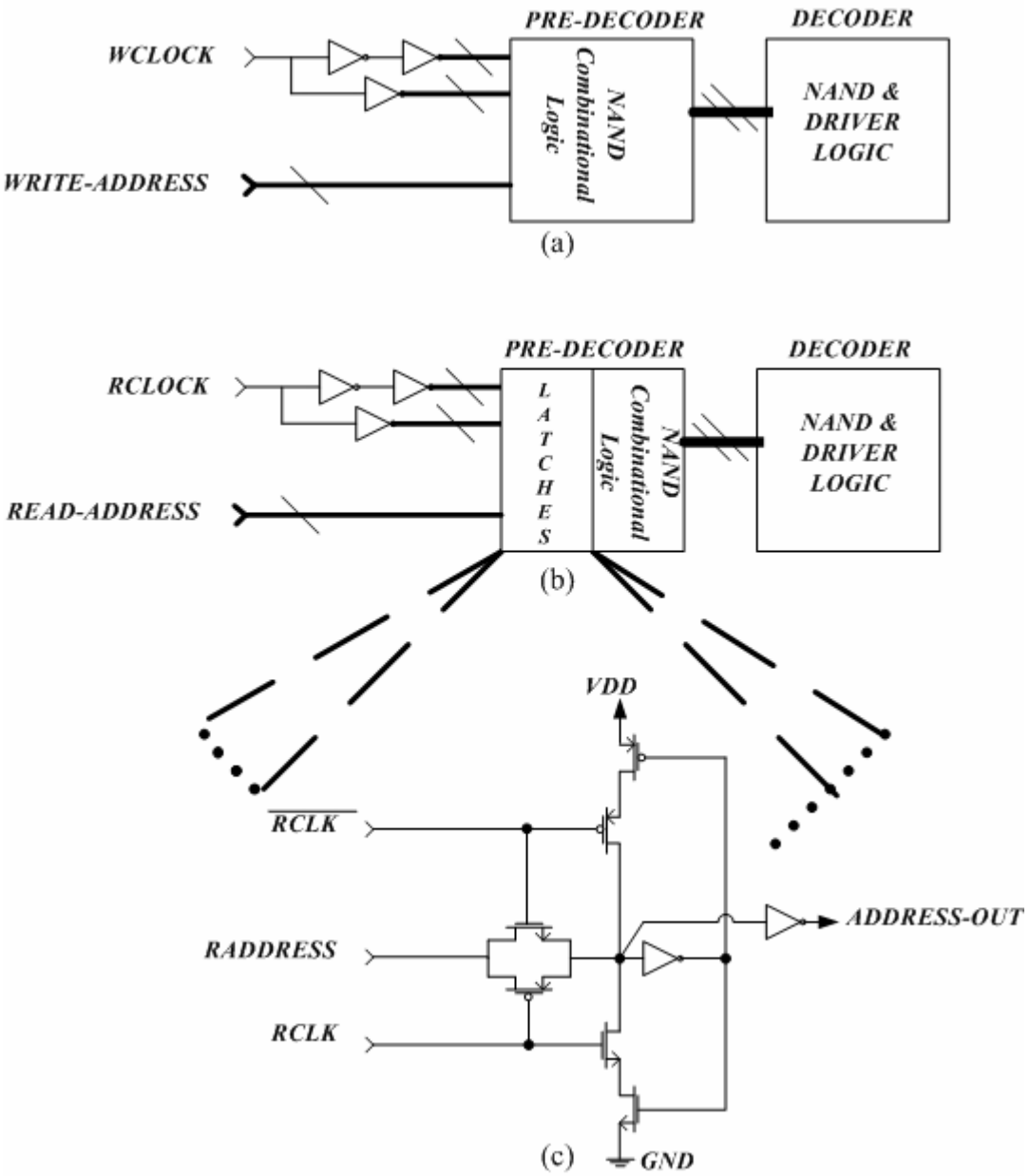

Fig. 3. (a) Write organization, (b) Read organization, (c) Read address latch.

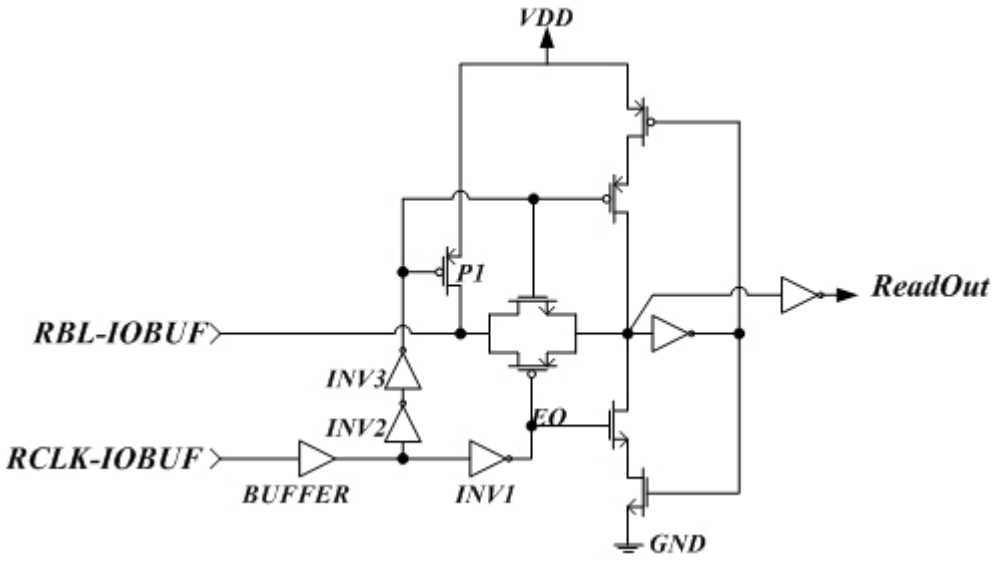

Fig. 4. Sense latch for pre-charge RBL and output driver buffer.

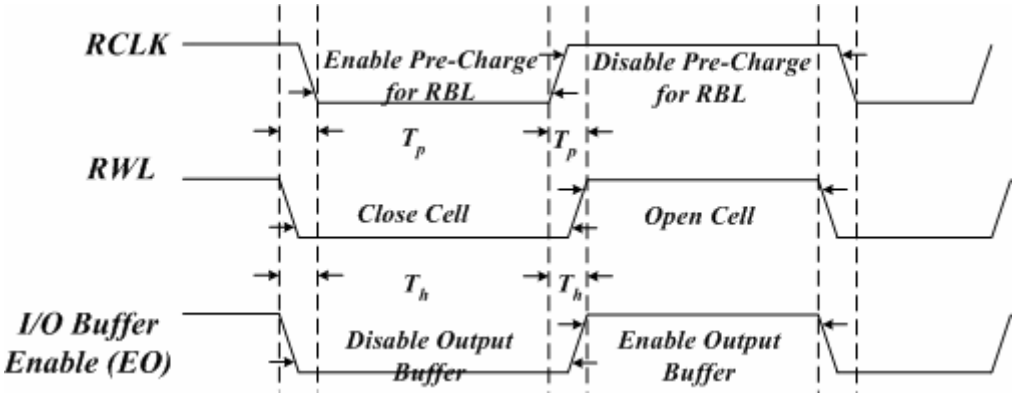

Fig. 5. Internal memory timing for read cycle.

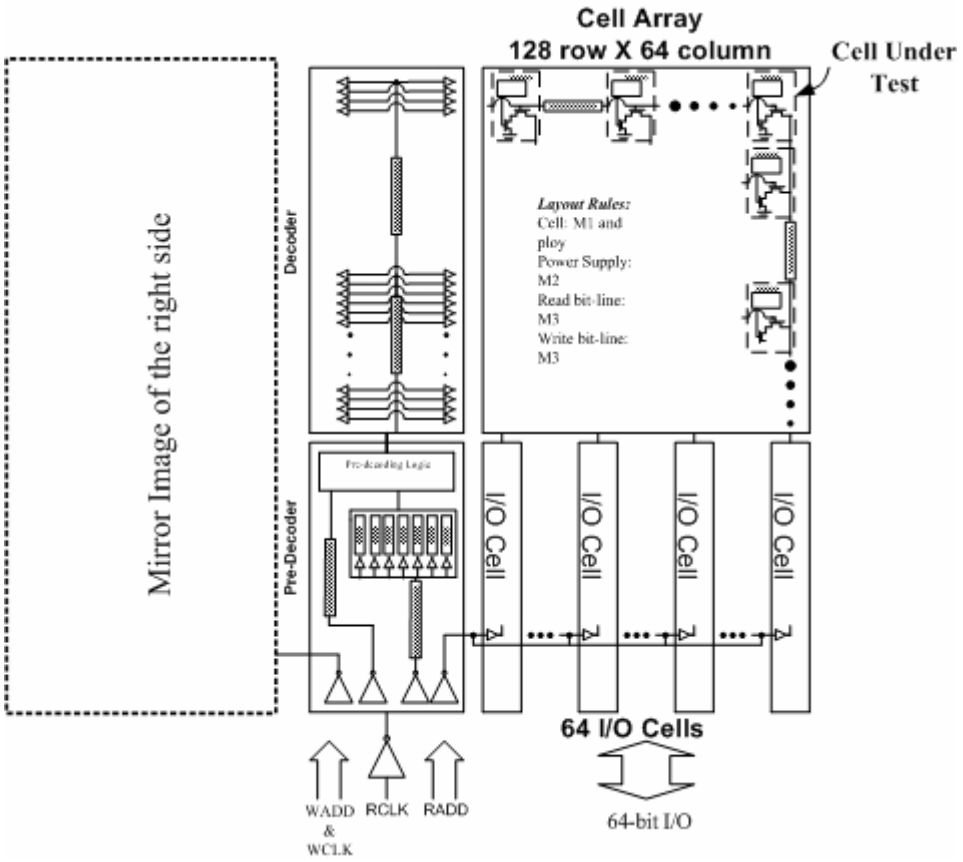

Fig. 6. Memory model for RC extract net-list of size 128-bit X 128-bit.

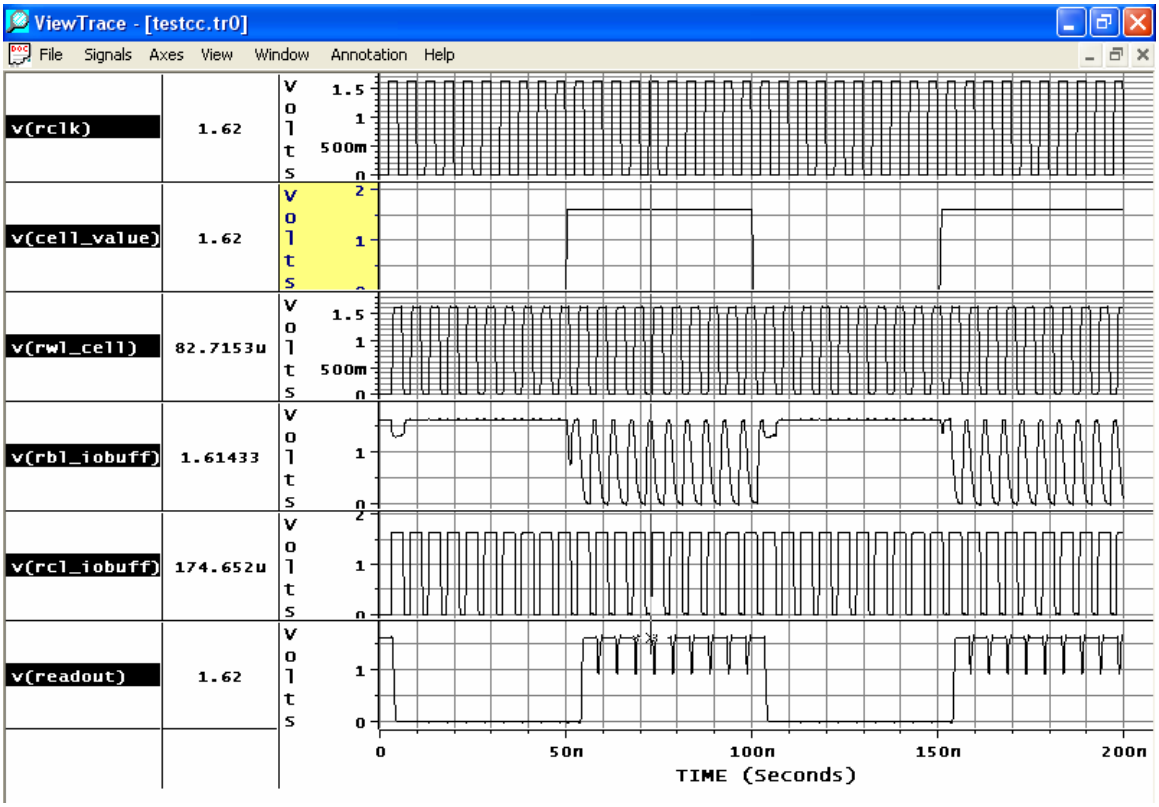

Fig. 7. HSPICE RC extracted net-list simulations for all internal read timing signals.

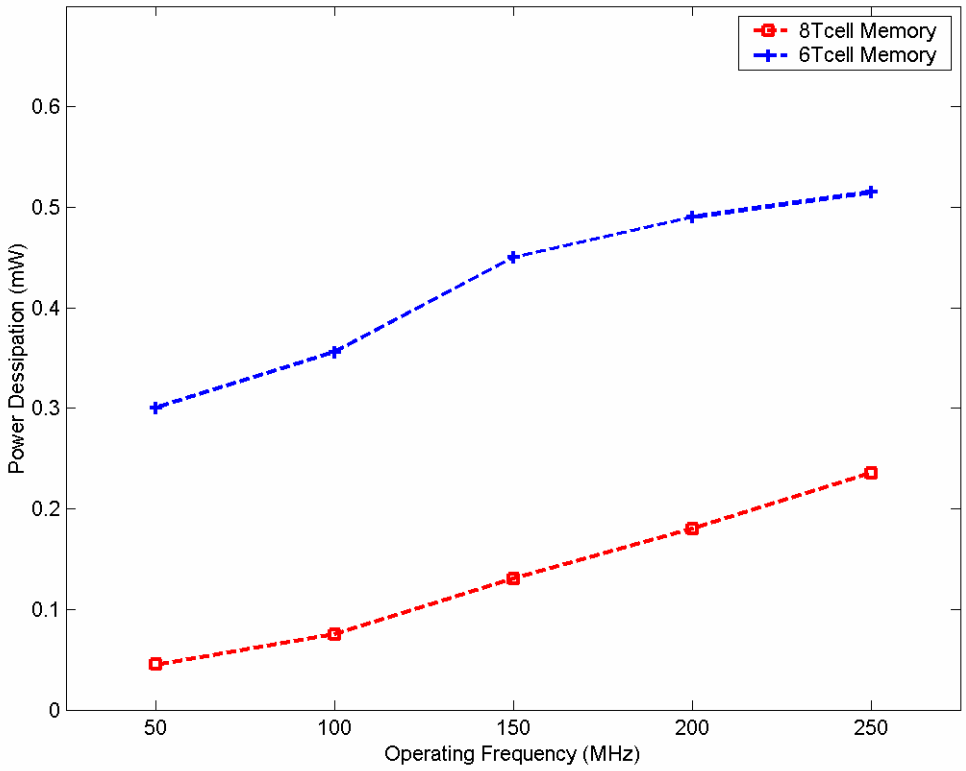

Fig. 8. Maximum power dissipation versus operating frequencies.

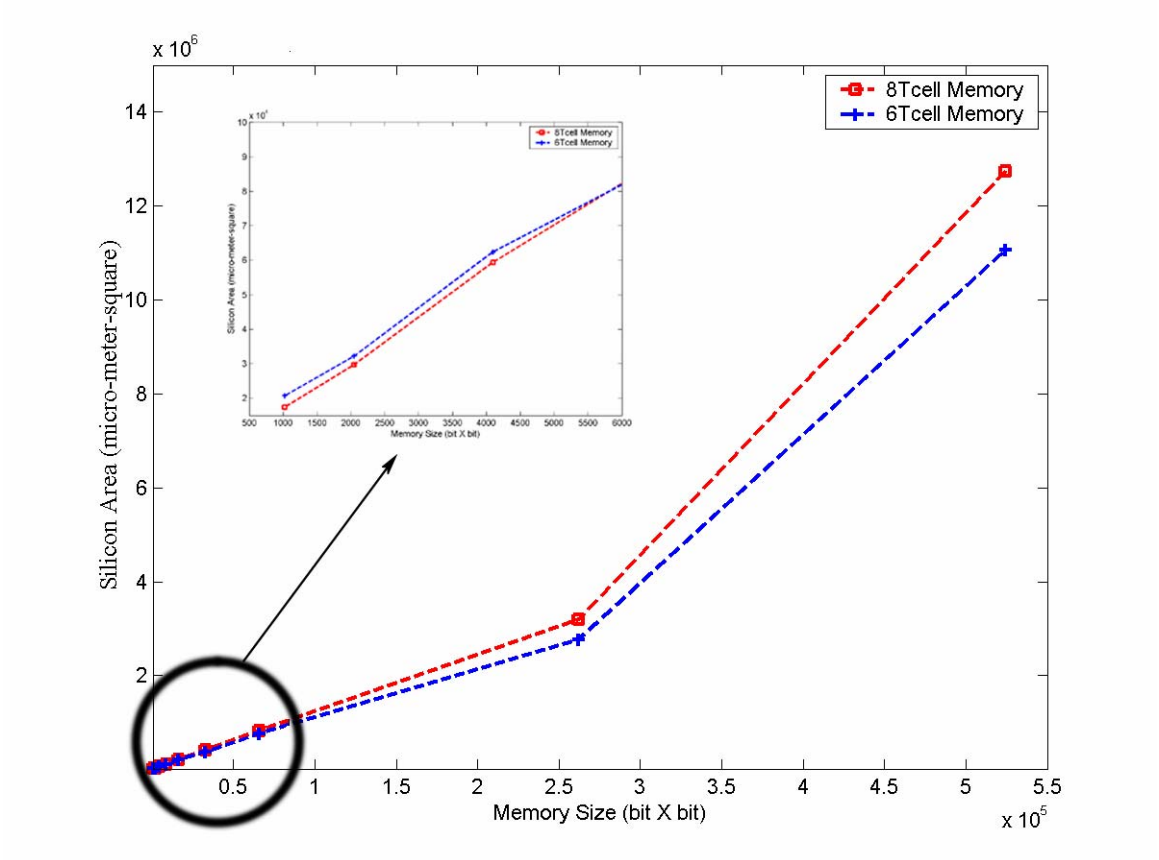

Fig. 9. Total layout area in μm^2 versus memory sizes in bit storage values.

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