A PULSE WIDTH MODULATION FOR PV CONNECTED DIODE ASSISTED Z SOURCE NPC-MLI TO OBTAIN HIGH VOLTAGE GAIN

***C. SANTHAKUMAR** ***R. SHIVA KUMAR**
* Assistant Professor, Department of Electrical and Electronics Engineering's. K.S.R I.E.T, India.
**Professor, Department of Electrical and Electronics Engineering, Sona College of Technology, India.
***C. BHARATRAJA**
***Department of Electrical and Electronics Engineering, SRM University, Chennai, India

Abstract: *The Z source inverter/ multilevel inverter (MLI) is an unavoidable converter technology in the power electronics family for renewable energy application since it having a nature of single stage operation. Particularly, in PV application these inverters are boosting the voltage in the single stage while converting DC to AC. Normally, the diode assisted Z Source Neutral Point Diode Clamed (NPC-MLI) with the photovoltaic system produces a supreme voltage gain that is relatively better than other double stage boost conversion practices. This paper mainly explores vector selection approach based pulse width modulation (PWM) for diode-assisted NPC-MLI to obtain a high voltage gain without compromising in waveform quality. To attain a higher voltage, gain maximum dc-link voltage utilization and power switches stress must be reduced. From the above issues in the diode assisted NPC-MLI leads to vector selection approach PWM technique to perform uniform charging and discharging capacitor to obtain maximum voltage gain. The operation of proposed inverter and its relation between the voltage gain and boost duty ratio then voltage stress on the switching device and gain are theoretically investigated. Due to energetic performance, Z source diode assisted NPC-MLI is more capable for wide range dc/ac power conversion in single stage, which is more suitable for PV applications. Besides, theoretically investigated are validated via simulation and experimental results*

Key words: *Neutral Point Diode Clamed MLI, Space Vector Pulse Width Modulation, boost conversion, diode-assisted NPC-MLI*

1. Introduction

Extensively in innumerable power electronic bids, such as photovoltaic (PV) based power generation and distribution system. The most prominent advantage in these claims is the low voltage dc source and required high output ac voltage [2], [4]. The largest aid to the power grid will be based on the development of the photovoltaic generation system through which renewable energy is utilized. The main drawback of the existing solar photovoltaic panels is the wide range voltage drop and high investment cost [5], [6]. Hence, there is a necessity to increase the low dc source voltage into a high constant ac voltage. Voltage source converter (VSIs and MLIs) are added to obtain the necessary alternating supply voltage for power grid [7], [14-21]. The initial cost can be minimized by decreasing the number of stages of inverter. Cuk and SEPIC, which have both buck-boost conversion and bidirectional power processing [8]. For improved performance, the buck-boost converter is modulated by addition of an extension, where commutation count area is studied and improved efficiency is achieved [9]. Nevertheless, the semiconductor devices used in buck- boost circuit lead to huge DC current and higher middle DC-link voltage when the boost duty ratio is extremely high [10]. Considering adding a power conversion stage, causing increase in system cost and reduction in efficiency, Peng[1] introduced Z source converter. This Z source inverter involves of a unique inductor and capacitor connected impedance network (Z network) between the DC source and the main inverter switching circuit and obtain the boost/buck operation characteristics [13]

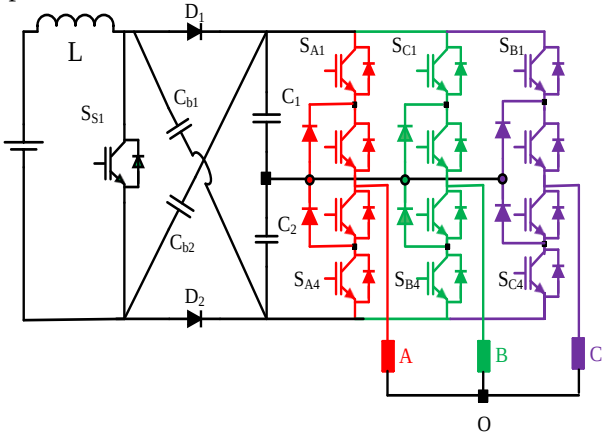


Fig.1.Circuit diagram of diode assisted buck-boost converter with NPC-MLI

In Shoot through (ST) manner a particular leg inverter switch is shorted and providing the bath to charge Z network inductors is to enhance the output voltage. This is offers a single-stage dc to ac power conversion with high the voltage gain [12]. This circuit incorporates an X-shaped capacitor and inductor connected network with diode-assisted in front end of the dc source. When S_{s1} is OFF, the two capacitors (C_1 and C_2) are linked in parallel over two diodes, which are forward-biased and the input dc-link voltage Vdc, Vi is equal to capacitor voltage, VC. At this duration, the 3-phase VSI output AC voltage is zero. Now the intermediate dc- link voltage can improve the voltage transfer ratio and reduce the voltage rating of the capacitors. The Numerous PWM approaches are elucidated to obtain the high voltage

gain as well as to abate the voltage stress on the conducting switches [13], [25], Diode-assisted buck–boost MLI validates rewards in development cost and noteworthy performance in dc/ac power conversion for simultaneously much higher and extensive choice voltage regulation [15,22-24]. Nevertheless, those methods are uses number of shoot through (ST) switching options and less bother on neutral point balancing.

Given that the neutral point balancing with minimal switching state usage was seldom investigated in the literature, this paper is demanding to cover the research gap. Within this context, in paper proposed the enhanced SVM techniques for Z-T-NPC-MLI with minimum number of ST state. The scheme feats the redundancy switching options for both ST switching and regular switching, which good voltage profile and maintain the quarter symmetry and harmonic spectra.

2. Proposed Inverter Derivation

Proposed Inverter Z-source MLI given in the Fig. 1 is having dual modes of operation based on the front-end shoot through switch (S_{ST}) "ON" and "OFF" state. When the S_{ST} is "ON", the source voltage is get short with inductor, hence the inductor stored the energy with respect to circuit current sand voltage as V_L=Ldi/dt. This mode is normally called as Shoot through (ST) mode.

When the S_{ST} is "OFF", the V_L=Ldi/dt. Energy will dissipate the X network capacitors as like boost converter. For convenience of the voltage transferring to the capacitance, the two capacitance C_1 and C_2 are connected in parallel, and terminal voltage across the C_1 and C_2 capacitors in the symmetrical X-shape network are expected as same values.

$$C_1 = C_2, V_{C1} = V_{C2} = V_C \quad (1)$$

The Fig. 2 shows the equivalent circuit for the diode based buck-boost converter when the switch S_{ST} is "ON". In this time period the two diodes are reverse biased.

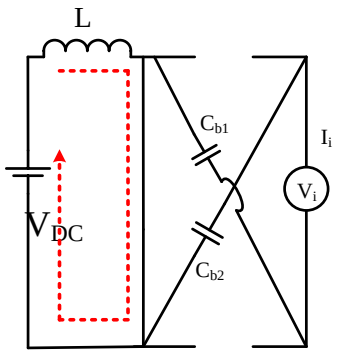


Fig.2. Converter during S_{ST} is ON

With this operation, the inductor present in the circuit absorbs the energy from the input DC by maximizing the current and the dual capacitors are coupled in series to feed the loads. The equations during this time period are expressed as below

$$V_L = V_S, V_{i(S_{ST}=ON)} = V_{C1} + V_{C2} = 2V_C \quad (2)$$

The Fig. 3 illustrates the diode based buck boost converter equivalent circuit when the switch S_{ST} is "OFF". Then the diodes D_1 and D_2 in the circuit are forward biased the energy gathered in the inductor L (V_L=Ldi/dt) is transferred to the capacitors, C_1 and C_2 and supply to the loads.

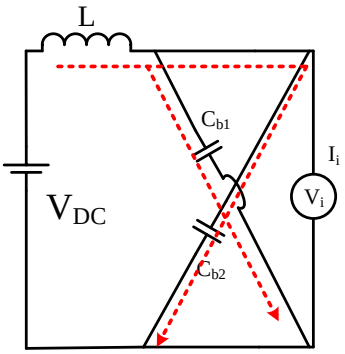


Fig.3. converter during S_{ST} is OFF

$$V_L = V_S - V_C. V_{i(S_{ST}=OFF)} = V_{C1} = V_{C2} = V_C \quad (3)$$

The inductor voltage during the switching period in steady state is zero. Hence, from (2) and (3), the voltage of the inductor is

$$V_L = \frac{p_{on}T_s \cdot V_{in} + (1-p_{on})T_s \cdot (V_s - V_c)}{T_s} \quad (4)$$

By using (4), the voltage across the capacitor is resulting as

$$V_C = \frac{1}{1-p_{on}} V_s \quad (5)$$

Where V_s is the input supply voltage, p_{on} is the ON state duty ratio, When S_{ST} is ON, T_s = 1/f_s, is switching time ON and OFF duration. In the similar way, the intermediate dc-link voltage across is,

$$V_i = \frac{p_{on} \cdot T_s \cdot 2V_c + (1-p_{on})T_s \cdot V_c}{T_s} = (1 + P_{on})V_S \quad (6)$$

The switching stress across the two diodes and switch present in front of the boost circuit is identical to the capacitor voltage V_C and similarly the switching devices voltage stress is the maximum.

The bridge voltage which is twice the capacitor voltage $2V_C$

$$V_{Sf} = V_C, V_{Si} = \hat{v_i} = 2V_C \quad (7)$$

The transfer ratio of the voltage for the diode assist NPC-MLI is defined as

$$G = \frac{\hat{v_i}}{\frac{V_S}{2}} = \frac{\widehat{2V_{ac}}}{V_{dc}} \quad (8)$$

When inverter in ST mode, the L is storing and during the Non –ST mode stored energy is dissipated into capacitor, since two capacitor is connected in parallel

the voltage are get doubled and the same dissipated to inverter DC-link capacitors C_3 and C_4. After, the DC-link capacitors voltage is connected to the load via MLI switching. The Fig. 4 show the proposed Z-MLI two mode of operation.

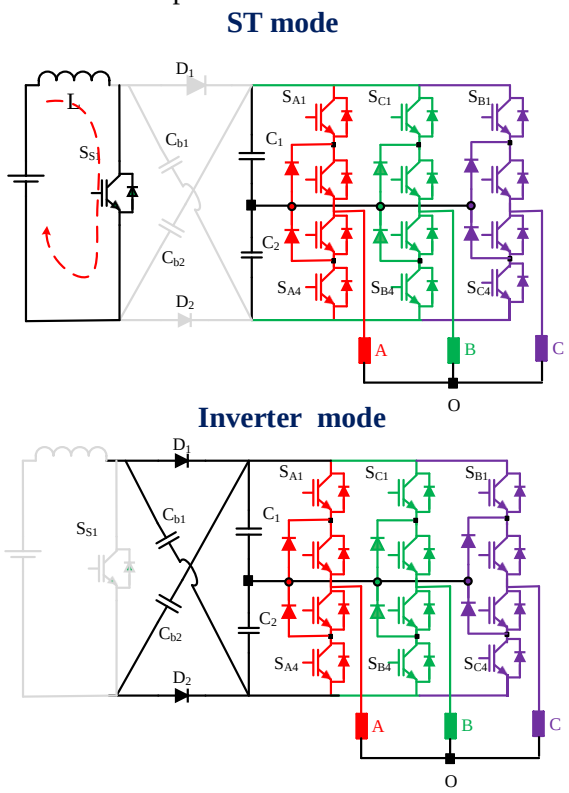


Fig.4 Mode of operation of the proposed Z –MLI

The inverter S_{ST} and other 12 MLI switches (S_{A1} to S_{C4}) are controlling through novel space vector modulation. The proposed SVM is following the conventional SVM procedure in the regular switching option, where the S_{ST} is operated in the suitable position of the SVM. The S_{ST} is chosen after near to small vector. The proposed SVM is explained clearly in the next section.

3.Proposed Pulse Width Modulation Strategies

The space vector diagram (SVD) for a 3-phase 3-level VSI is a hexagon, consisting of six sectors as shown in Fig.7, and each sector consists of four sub-triangles. Each inverter leg can have 3 states of switching, in which there are 27 switching options to produce the voltages. When switching states (111), (000), and (-1-1-1), taken place, there is no power is delivered to the load. These states are called as zero vector switching/ null voltage vector (NV). The Fig.6. Show the NV switching sequence [111],[000]. (Similarly, other 24 switching options are active vector (AV), which are producing output voltage on the MLI. The AVs have three phase voltage levels, which are 2/3Vs, $V_s/\sqrt{3}$, and $V_s/3$. Each voltage level links to the vertex of the big hexagon named the large vector (LV), that on the mid side of the big hexagon called the medium vector (MV) and vertex of the small (inside) hexagon named the small vector (SV), respectively. The six LVs forms the vertices of the hexagon and the three NVs are located at the origin. For theoretical analysis, a new concept introduced which is called as the natural point potential. The Fig.5 show the active vector switching sequence for [1-1-1] , [100] , [10-1].

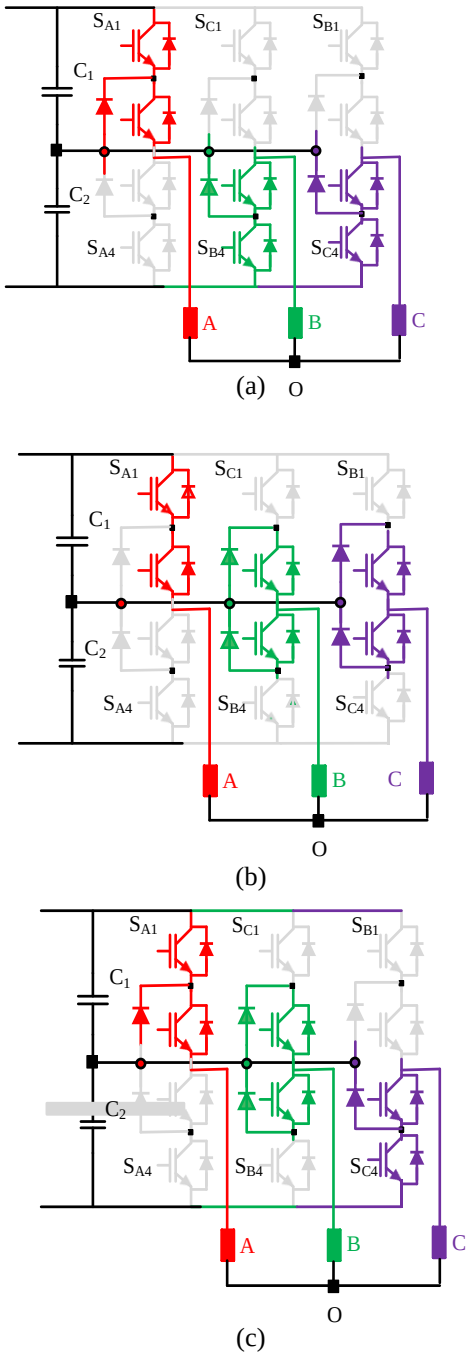


Fig.5 Regular MLI switching with active switching states; (a): [1-1-1] , (b):[100] , (c): [10-1]

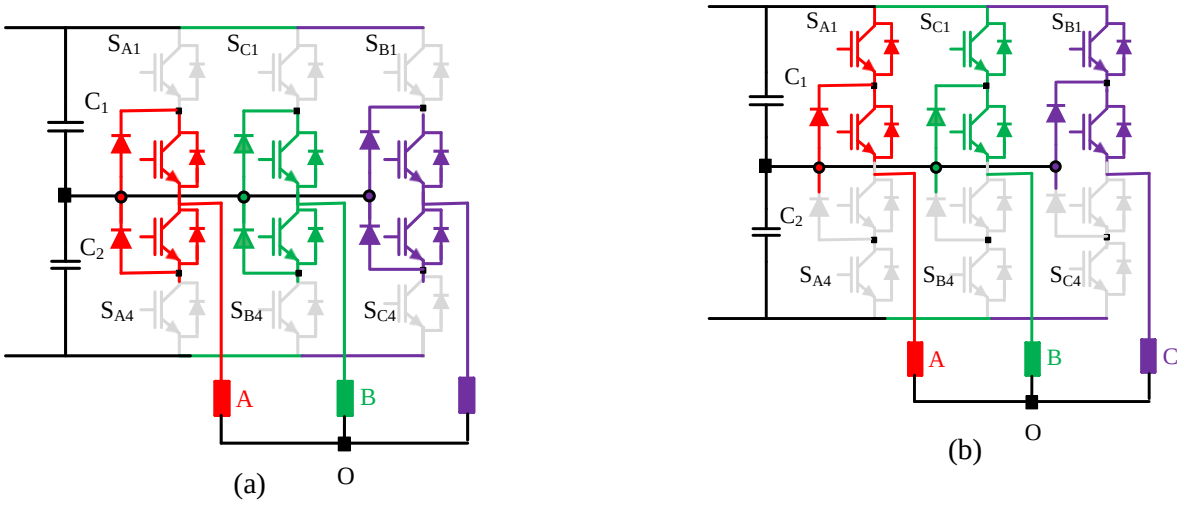
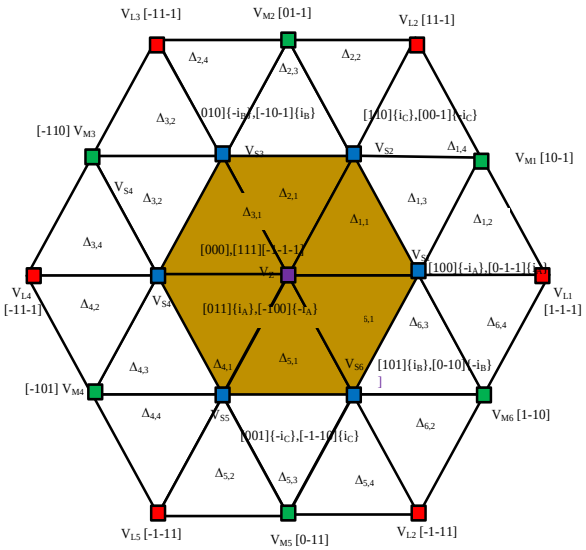


Fig.6 non- active switching states;
(a): [111], (b):[000]



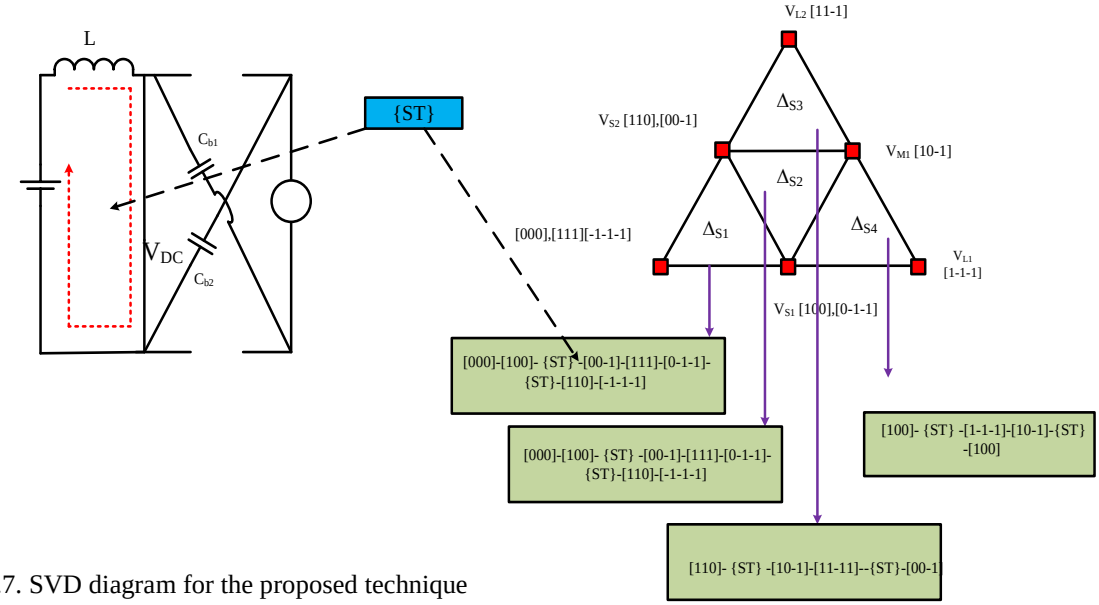


Fig.7. SVD diagram for the proposed technique

In the stationary coordinates SVM is defined as,

$$V_r = |V_r| e^{j\theta r} = \frac{2}{3}[V_{ao} + V_{bo} e^{j\frac{2}{3}\Pi} + V_{co} e^{-j\frac{2}{3}\Pi}] \quad (9)$$

In the above equations V_{ao}, V_{bo}, V_{co} are the line to neutral voltages, V_{aN}, V_{bN}, V_{cN} are the line to zero voltages, V_{oN} is the neutral to zero voltage

$$V_{ON} = \frac{1}{3}V_c, V_{ao} = \frac{2}{3}V_c, V_{co} = V_{bo} = -\frac{1}{3}V_c \quad (10)$$

$$V_1 = |V_1| = \frac{2}{3}V_c \quad (11)$$

$$|V_1| = |V_3| = |V_5| = |V_7| = |V_9| = |V_{11}| = \frac{2}{3}V_c \quad (12)$$

$$|V_2| = |V_4| = |V_6| = |V_8| = |V_{10}| = |V_{12}| = \frac{4}{3}V_c \quad (13)$$

Based on the above PWM strategy there is a necessity for the new PWM strategy to yield the full advantage on the small vectors. The Fig. 7 given SVM for the proposed Z-MLI and showing the categorizations of the switching voltage vectors in the first sector switching state including ST state. The active switching vectors are commanded during the both intervals when S_1 is ON and S_2 is OFF with one switching time period (T_s) to makes the reference (V_r). The V_r symmetrically distributed with two switching time periods ($2T_s$) by introducing the interval of S_1=ON equally in centre. In order to minimize the half-switching low frequency harmonics distortion, the second upgraded PWM approach is offered to ensure a symmetrical assignment of switching conditions in one switching time. The foremost feature of this modulation approach is that S_1 turns ON and OFF once with S_1=ON interval symmetrically introduced at the middle of one switching period T_s. There will be an added switching state for small vector V_1. With this introduces an added switching state in phase leg of the inverter bridge in OFF state (S_1=OFF). With the same design method, the switching states in other sextants can be obtained.

The modulation index, M_a is limited by the ON-state duty of the switching S_1 in th boost circuit.

$$G = \frac{2M_i}{1-p_{on}} (0 \le M_i \le P_{ON}) \quad (17)$$

V_{sf} I the voltage stress across the switching devices the boost circuit, which is same as the V_c

$$V_{Sf} = \frac{1}{1-p_{on}} V_S, V_{Si} = \frac{2}{1-p_{on}} V_S \quad (18)$$

For the conventional SPWM with third harmonic injection or SVM, The DC voltage consumption of the inverter bridge is increased and the maximum modulation index of M_t=1.15 p_{on}.

$$G_{max} = \frac{4}{\sqrt{3}} \frac{p_{on}}{1-p_{on}} (M_i = \frac{2}{\sqrt{3}} P_{on}) \quad (19)$$

$$V_{sf} = \frac{4+\sqrt{3}G_{max}}{4} V_s, V_{Si} = \frac{4+\sqrt{3}G_{max}}{2} V_s \quad (20)$$

4. Simulation study

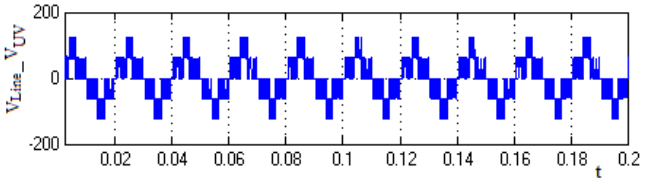
In order to validate the proposed diode- assist Z-MLI, the simulation system is performed using MATLAB/Simulink and results are obtained. The simulation parameters are given in Table-1.

Table -1

Simulation parameters- diode- assist Z-MLI

Parameters	Values
Z source network capacitors C_1 and C_2	640 µF
Input Inductor, L	10 mH
DC Link voltage	100V
DC Link capacitor C_3 and C_4	1000 µF

The simulation is tested for the different operating conditions based on the modulation index value. The M_a is fixed in the simulation from zero to 0.9. When the modulation index is increased, the ST switching period and MLI regular switching modulation index both are changing correspondingly. While the M_a is one, the inverter approaches to maximum boosting as 200%. When the inverter is operated in the linear modulation range with the maximum modulation index of 0.7. The internal resistance of IGBT is considered as 1 mΩ and snubber resistance is 10 micro Ohm. Two equal capacitors are considered across the supply to split the supply voltage in to two equal half and to create a neutral point. In this Simulation circuit the source voltage is considered as 100 V DC and the output of the NPC-MLI is 180 V AC (maximum). Line voltage and THD for the M_a of 0.65 and 0.85 for the NPC-MLI is shown in the Fig. 5 and 6. From the results, it could have understood that the proposed Z-MLI capable increasing the voltage level by using one inductor itself.



(a)

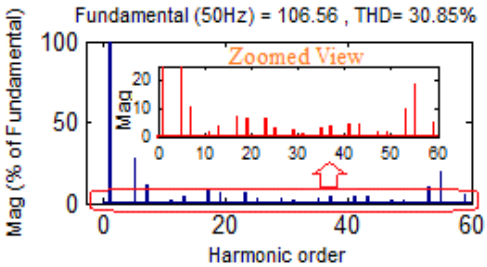
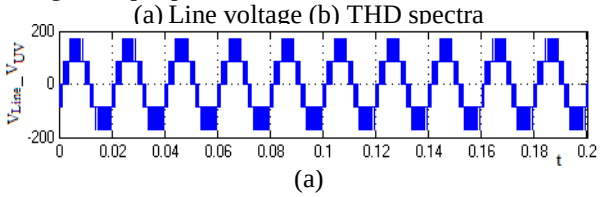
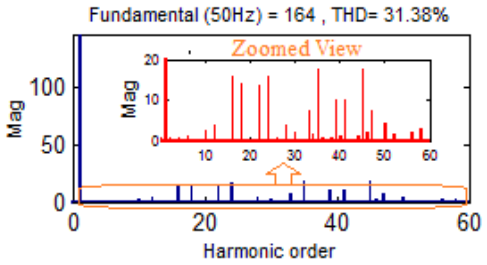


Fig.8. output performance characteristics for M_a=0.7 (a) Line voltage (b) THD spectra



(a)



(b)

Fig.9. Output performance characteristics for M_a=0.9 ,(a)Line voltage (b) THD spectra

The inverter also maintains the DC-link capacitors values with in the acceptable limit IEEE values as 1%. The table- 5 shows the full range of modulation index and its corresponding inverter operating performance

Table -4
Proposed Z MLI performance

M_a	V_{line} in Volts	V_{THD} %	V_{C3} and V_{C4}
0.2	42	29.10	21.5, -20.5
0.4	78	29.50	39.26, -39.56
0.65	106.56	30.85	53.62,-53.89
0.9	164	31.38	82.41,-82.69

5. Experimental Study

In order to validate proposed Z source MLI, the 1kW experimental setup is derived via Spartan-6 FPGA controller. The inverter IPM is connected with 1kW induction motor with stator voltage control as sowh in Fig.10.

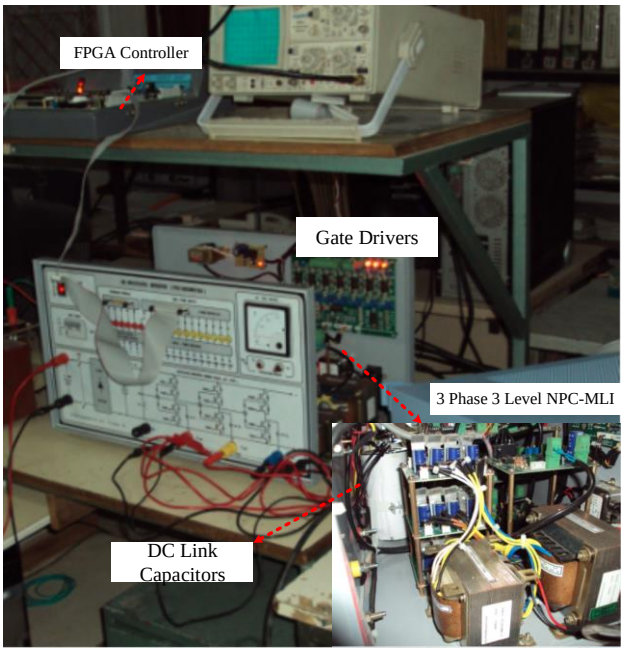


Fig.10 Experimental setup

DC link capacitor used for the inverter is two 100µF front-end DC-link capacitors. Two DC Link film capacitors (C_3 and C_4) with capacitance of 480 µF and a voltage range of 450 to 1300 is used to provide the self-balancing of capacitance. In the impedance network, two identical capacitances as a 3400uF µF and a voltage range of 450V is used with single source inductance of 15 mH. The HIRECT power diode is used with inductor for the shoot through option. The 1000V, 10A power MOSFET is used as boosting switching, which is connected in front of the circuit and which provide the isolation between source and load while inverter operating in ST mode.

Based ST switch, S_{ST} operation time, the MLI boosting factor is obtained. When S_{ST} switching provide is maximum, the MLI is approach to maximum boosting (nearly 200%) and when ST switch is fully OFF, the MLI is perform like a ordinary MLI. The Fig. X shows the gate trigging pulse of MLI lag A.

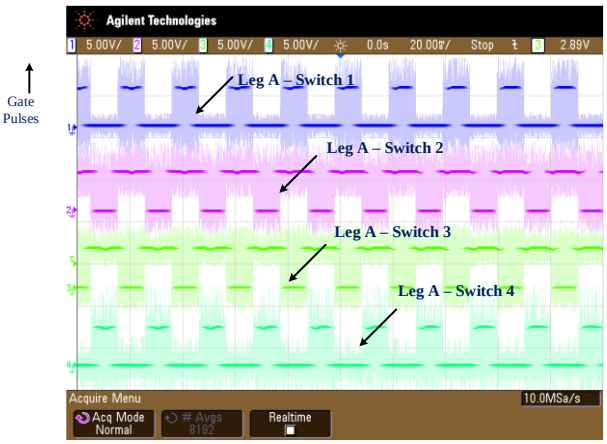


Fig.11. Gate pulses of leg-A of Z MLI

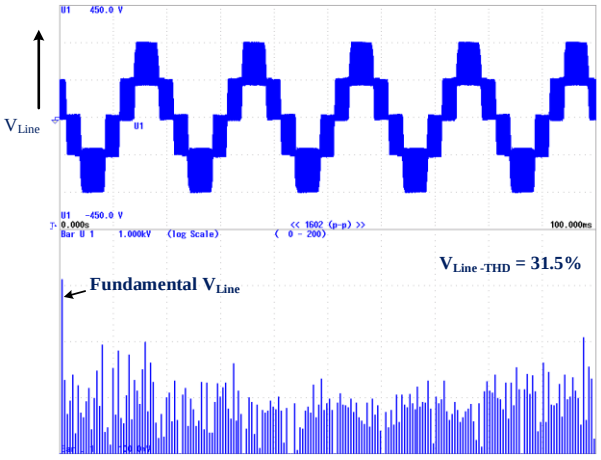


Fig.12 Experimental Line voltage (150Vdiv) THD spectra for M_a=0.65

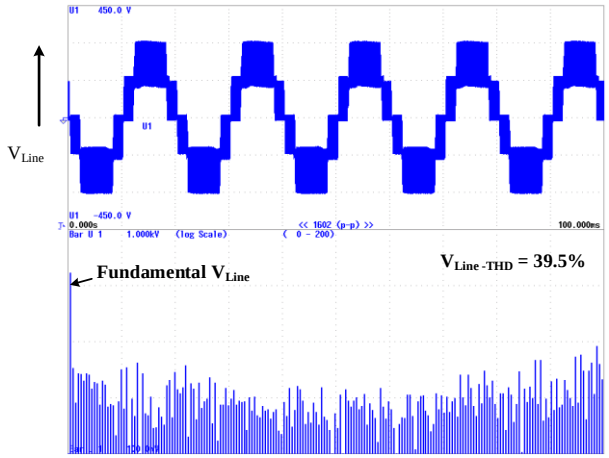


Fig.13 Experimental Line voltage (150Vdiv) THD spectra for M_a=0.9

Fig.14 Experimental capacitor C_1 voltage profile for M_a=0.9

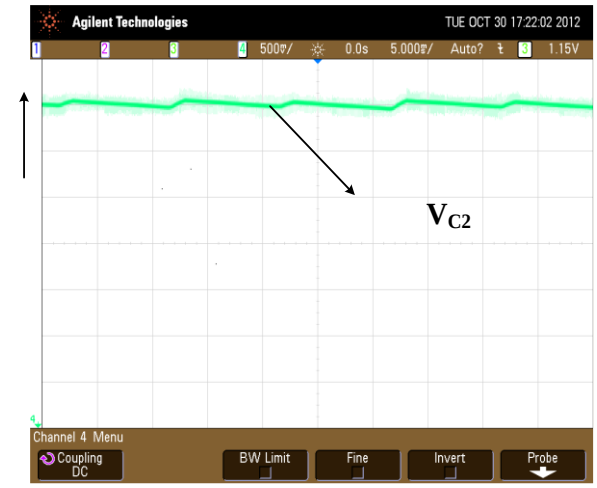


Fig.15 Experimental capacitor C_2 voltage profile for M_a=0.9

The experimental results for entire modulation region are shown in fig.12 for M_a=0.65. Here the line voltage and THD spectra is witnessed as 167V and 32.89% respectively. Similarly, when the M_a is 0.9 as shown in the Fig.13, the inverter about to reach their maximum boosting value as 256V, here the voltage THD percentage of the inverter is higher due to high boosting pulse dropping. However, this low value while comparing to the conventional X impedance network MLI performance. The DC link capacitors are balancing their charging and discharging in a self-balancing manner, since the SVM used in the proposed Z-MLI is using all redundant switching options. The Fig. 14 and 15, shows the DC-link capacitor C_3 and C_4 voltage profile. From the results, it could undershoot that, C_1 and C_2 both are having identical charging and discharging, which ensure the output voltage THD profile in a better way. From the simulation and experimental results, it could understand that the proposed SVM for Z NPC-MLI is produced more line voltage and less THD compare to the previous work [12]. In addition, the scheme uses less number of ST, which reducing the switching losses on the inverter. Here could understand that the conduction losses are low throughout the operating value of M_a, which lead the best efficiency of Z-T-NPC-MLI

5. Conclusion

This paper analyses the disadvantages of the available PWM approaches for the diode assisted buck-boost VSI and proposed innovative PWM strategy. The voltage gains and switching device stress are improved compared to the existing PWM strategy. The results experimental are provided in order to confirms the theoretical results. The advantages are high voltage gain and the wide range of voltage regulation, because of these advantages this topology is using for a wide choice of power adaptation in PV bids.

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