Design of Clocked SR and Clocked D Flip Flops using CNTFET Logic Gates

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Abstract*: The main objective of this paper is to develop a compact model for MOSFET like CNTFET with fabrication feasibility. The physical structure of CNTFET is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics. The modeled CNTFET has been used to design logic gates which shows superior performance over MOSFET based logic gates. The various clocked flip flop circuits have been designed using CNTFET logic gates and simulated using Hspice. The use of CNTFET logic gates for designing flip flop circuits can reduce the power consumption and size.*

Key words: *Carbon nanotube, Carbon Nanotube Field Effect Transistor, Flip Flop, Hspice, Logic gates, Nanotechnology.*

1. INTRODUCTION

Carbon Nano Tube have generated much interest in the last few years for application in electronic devices because of their demonstrated ability to serve as a possible alternative to silicon technology for fabrication of nanoscale electronic devices, in view of the challenges faced by the continuous scaling of existing silicon technology. Small size of the MOSFET, below a few tens of nanometers creates the low Trans-conductance, gate oxide leakage, low ON-current, Mobility degradation and increased delay.

CNTFETs are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon[1]-[3].

The main drawbacks of the MOSFET is that the sensitivity of a MOSFET's gate to static and high-voltage spikes makes it vulnerable to damage resulting from parasitic oscillation. This undesired self-oscillation could result in excessive gate-to-source voltage that permanently damages the MOSFET's gate insulation. Another MOSFET limitation is gate capacitance. This parameter limits the frequency at which a MOSFET can operate effectively. CNTFET overcomes these limitations to produce better performance than MOSFET.

In terms of the device operation mechanism, CNTFET can be categorized as either Schottky Barrier (SB) controlled FET or MOSFET-like FET [4]-[7]. Though good dc current can be achieved by SB-controlled CNTFET with the self-aligned structure, its ac performance is going to be poor due to the proximity of the gate electrode to the source/drain metal. The ambipolar behavior of SB-controlled CNTFET also makes it undesirable for complementary logic design. Considering both the fabrication feasibility and superior device performance of the MOSFET-like CNTFET as compared to the SB-controlled FET, we choose to focus on MOSFET-like CNTFETs in this work.

This paper is organized as follows. Section 2 and Section 3 introduces the Carbon Nanotube and Carbon Nanotube Field Effect Transistor. Section 4 deals with the modeling aspects of MOSFET like CNTFET. Section 5 deals with the design and performance analysis of the various clocked flip flop circuits designed using MOSFET like CNTFET gates. Section 6 concludes the work undertaken in this paper.

2. CARBON NANOTUBE ELECTRONICS

Carbon nanotubes were discovered by S. Ijiima[8][9] in 1991 while performing some experiments on molecular structure composed of carbonium. CNTs are hollow cylinders composed of one or more concentric layers of carbon atoms in a honey comb lattice arrangement [10]-[12]. It can be classified into SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube) shown in Figure1.

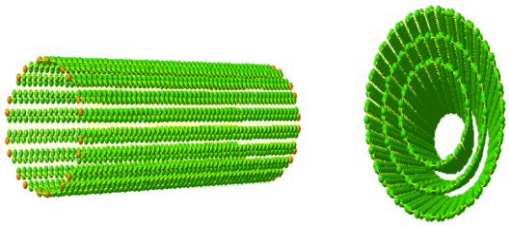

Figure 1: SWCNT and MWCNT

Based on the chiral vector, Circular vector that is perpendicular to the axis of the tube, CNTs are classified as Arm Chair, Zigzag & Chiral (Figure 2).

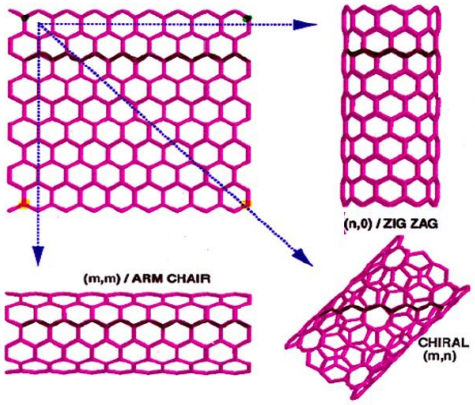

Figure 2: classification based on chiral vector

CNTs can be either metallic or semiconducting; this raises the scope for new integrated circuit technologies made from CNT transistors and interconnects. However, in this research we confine our study to CNT Field Effect Transistor.

3. CARBON NANO TUBE FIELD EFFECT TRANSISTOR

It has been shown that semiconducting carbon nanotubes can be used as the conducting channel in Carbon nanotube field effect transistors. To create such devices, nanotubes are grown on top of a thick silicon dioxide. When metal contacts are laid along the length of a nanotube, many transistors are formed along CNT. The length of the nanotube, between two contacts, acts as the channel of a transistor with metal source and drain. Because of the fixed CNT diameter once a nanotube is grown, the width of the nanotube cannot be changed to increase the current drive, instead, a transistor's width and current drive can be increased by adding nanotubes in parallel.

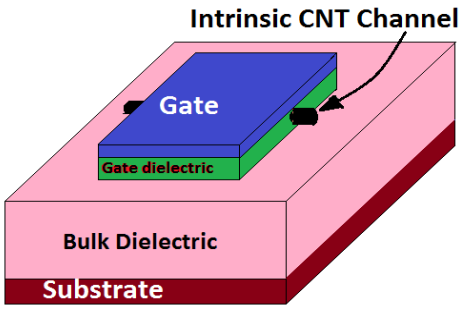

Figure 3: Structure of MOSFET like CNTFET

The metal gate is used to modulate the electronic band structure of the source, drain and carbon nanotube through a thin gate oxide. The metal gate and oxide must overlap slightly with the source and drain contacts. This overlap limits the area savings of CNTFETs. The current is regulated by the gate to source and gate to drain interactions. Figure 3 is a theoretical illustration of a carbon nanotube FET structure. The structure resembles that of a MOSFET[13][14], but the nanotube is the channel for conduction.

4. SIMULATION MODEL OF CNTFET

The MOSFET-like CNTFET model used in this study is schematically shown in Figure 4. A brief description of the theoretical analysis is given as follows. We assume near-ballistic transport and contacts in this work, i.e. eVDS ≈ μd−μs so μs remains almost constant in the source-channel region and μd remains almost constant in the channel-drain region.

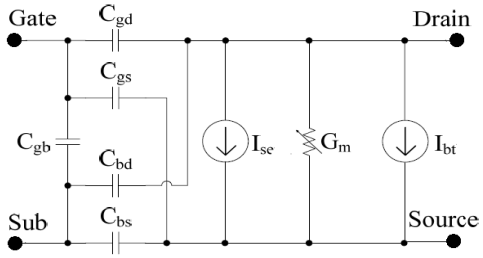

Figure 4: Equivalent circuit of MOSFET like CNTFET

We consider three current sources in this CNTFET model: (1) the thermionic current contributed by the semiconducting sub-bands (Ise) with the classical band theory, (2) the current contributed by the metallic sub-

bands (Im), and (3) the leakage current (Ibt) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

A. Current and Capacitance Expressions

The thermionic current contributed by the semi conducting sub-bands is given by,

$$I_{se}\left(V_{ch,DS},V_{ch,GS}\right) = \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{M} T_m\cdot\left[V_{ch,DS}+\frac{kT}{e}\ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/kT}}{1+(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/kT}\right)\right] \quad (1)$$

Vch,DS and Vch,GS denotes the Fermi potential differences near source side within the channel, e is the unit electronic charge, ΔΦB is the channel surface potential change with gate/drain bias, Tm is the transmission probably, k is the Boltzmann constant and T is the temperature in Kelvin and Em,0 is the half band gap of the mth sub-band.

For metallic sub-bands of metallic nanotubes, the current Im includes both the electron current and the hole current,

$$I_m = 2(1-m0)T_{met}\sum_{\substack{k_l \\ l=1}}^{L}\left[J_{e\_0,l}+J_{h\_0,l}\right] \quad (2)$$

$$J_{h\_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\left(f_{FD}(-E_{0,l}-\Delta\Phi_B)-f_{FD}(-E_{0,l}+eV_{ch,DS}-\Delta\Phi_B)\right) \quad (3)$$

$$J_{e\_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\left(f_{FD}(E_{0,l}-\Delta\Phi_B)-f_{FD}(E_{0,l}+eV_{ch,DS}-\Delta\Phi_B)\right) \quad (4)$$

fFD(E) is the Fermi-Dirac distribution function, $f_{FD}(E)=\frac{1}{1+e^{E/kT}}$ and the transmission probability Tmet is given by,

$$T_{met} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op}+(\lambda_{ap}+\lambda_{op}).L_g} \quad (5)$$

Lg, the channel length , λop (~ 15 nm[15]), the optical phonon scattering mean free path (MFP) and λap (~ 500 nm[16]), the acoustic phonon scattering MFP.

In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling current from drain to source becomes significant. We include a voltage controlled current source Ibt in the device model in order to evaluate the device sub-threshold behavior and the static power consumption.

$$I_{bt} = \frac{4e}{h}kT \quad * \quad \sum_{\substack{k_m \\ m=1}}^{M} T_{bt}\ln\left[\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+(E_{m,0}-E_f)/kT}\right).\frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right] \quad (6)$$

To model the intrinsic ac response of CNTFET device, we use a controlled transcapacitance array among the four electrodes (G, S, D, B) with the Meyer capacitor model [17], thereby the equations for capacitance calculation are given as follows.

$$C_{bs} = C_{gs}\frac{C_{sub}}{C_{ox}} \quad (7)$$

$$C_{gs} = \frac{L_g C_{ox}(C_{Qs}+(1-\beta C_c))}{C_{tot}+C_{Qs}+C_{Qd}} \quad (8)$$

$$C_{bd} = C_{gd}\frac{C_{sub}}{C_{ox}} \quad (9)$$

$$C_{gb} = \frac{L_g C_{sub}C_{ox}}{C_{tot}+C_{Qs}+C_{Qd}} \quad (10)$$

$$C_{gd} = \frac{L_g C_{ox}(C_{Qs}+\beta C_c)}{C_{tot}+C_{Qs}+C_{Qd}} \quad (11)$$

C_{tot}, is the total electrostatic coupling capacitance per unit length between channel and other electrodes, C_{Qs} and C_{Qd} as the quantum capacitance due to the carriers from source (+k branch) and drain (−k branch), respectively.

5. FLIP FLOPS

The storage elements employed in clocked sequential circuits are called flip flops. A flip flop is a binary cell capable of storing one bit of information. It has two outputs, one for the normal value and one for the complement value of the bit stored in it. A flip flop maintains a binary state until directed by a clock pulse to switch states[18]. The difference between various types of flip flops is in the number of inputs they possess and in manner in which the inputs affect the binary state.

In order to demonstrate the versatility of MOSFET like CNTFET, we employed it to design basic logic gates followed by various flip flops such as SR flip flop and D flip flop.

A. 2 input NAND Gate

Figure 5 shows an exemplary NAND gate comprising of CNTFETs as discussed herein in accordance with some embodiments. It comprises of driver CNTFETs coupled together in parallel between a high supply reference (VDD) and a series active load transistors, which is coupled to a low supply reference VSS, as shown.

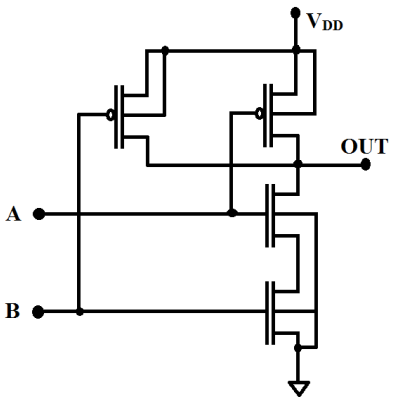

Figure 5: Structure of 2 input CNTFET NAND gate

The gates of the driver transistors provide first and second NAND gate inputs respectively and a gate output is provided at the drain of third transistor as shown. If either input or any one of the input is LOW (e.g., 0V) then the output is HIGH (approaching VDD), if both inputs are HIGH, then the output will be LOW as shown in Figure 6.

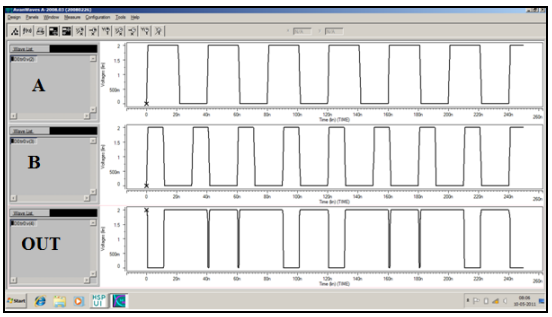

Figure 6: Behavior of 2 input CNTFET NAND gate

B. Clocked SR Flip Flop

The clocked SR flip-flop shown in Figure 7 consists of four NAND gates.

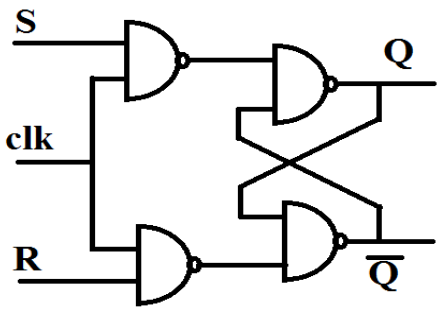

Figure 7: Clocked SR Flip Flop

The outputs of the two AND gates remain at 0 as long as the clock pulse is 0, regardless of the S and R input values. When the clock pulse goes to 1, information from the S and R inputs passes through to the basic flip-flop. With both S=1 and R=1, the occurrence of a clock pulse causes both outputs to momentarily go to 0.

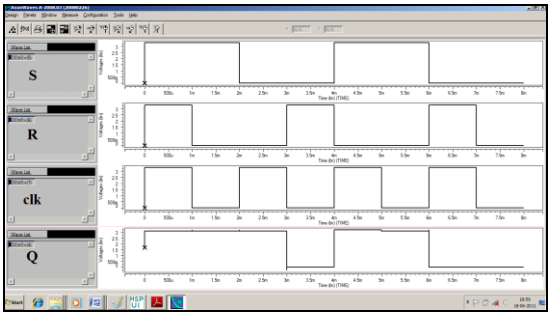

Figure 8: Behavior of Clocked SR Flip Flop

When the pulse is removed, the state of the flip-flop is indeterminate, i.e. either state may result, depending on whether the set or reset input of the flip-flop remains a 1 longer than the transition to 0 at the end of the pulse as shown in Figure 8.

C. Clocked D Flip Flop

The D flip-flop shown in Figure 9 is a modification of the clocked SR flip-flop.

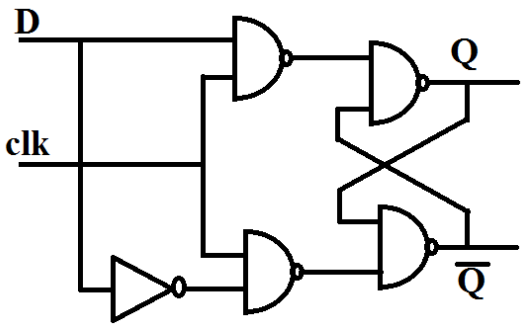

Figure 9: Clocked D Flip Flop

The D input goes directly into the S input and the complement of the D input goes to the R input. The D input is sampled during the occurrence of a clock pulse. If it is 1, the flip-flop is switched to the set state (unless it was already set). If it is 0, the flip-flop switches to the clear state as shown in Figure 10.

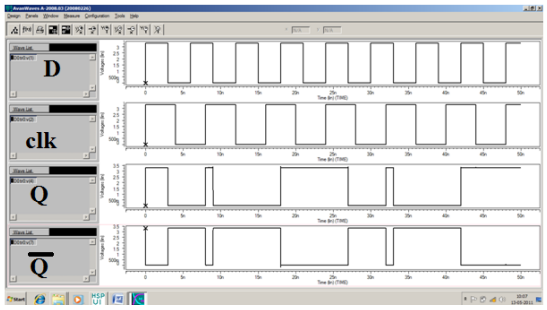

Figure 10: Behavior of Clocked D Flip Flop

6. CONCLUSION

The largest potential of carbon nanotube FET to clocked flip flop is illustrated in this paper. The carbon nanotubes transistors have the ability to scale the technology into new feature sizes and generations with similar I-V characteristics to MOSFETs. CNTs can have a varied energy bnd gap depending on their chirality and CNT diameter. We have presented a circuit compatible model of the MOSFET like single walled Carbon Nanotube Field Effect Transistors (CNTFETs). The model so developed has been used for designing clocked RS and clocked D flip flop circuits. The simulation results showed that the use of CNTFET logic gates for designing the flip flop circuits can reduce the area by 23% and power dissipation by 18% to 20%.

References

[1] H.-S. P. Wong, “Beyond the Conventional Transistor,” IBM J. Research & Development, March/May, pp. 133-168, 2002.

[2] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong, F. Beouff, “The Road to the End of CMOS Scaling,” IEEE Circuits and Devices Magazine, pp. 16 – 26, 2005.

[3] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, H. Dai, “Self-Aligned Ballistic Molecular Transistors and Electrically Parallel Nanotube Arrays,” Nano Letters, vol. 4, pp. 1319-1322, 2004.

[4] A. Bahari, G. Arasteh and S. Taghizadeh, ”Nanometer-Scaled Contacts in CNTFETs,” World Applied Sciences Journal 7 (Supplement 1): 18-21, 2009

[5] J. Deng and H.-S P. Wong, “A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part I: Model of the Intrinsic Channel Region,” Submitted to IEEE Transactions on Electron Devices, 2007.

[6] J. Deng and H.-S P. Wong, “A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part II: Full Device Model and Circuit Performance Benchmarking,” Submitted to IEEE Transactions on Electron Devices, 2007.

[7] L.Castro,”Modeling of Carbon Nanotube Field Effect Transistors,” Ph.D. dissertation, The University of British Colombia, July 2001.

[8] S. Iijima, “Helical microtubles of graphitic carbon”, Nature 354, pp. 56–58, 1991.

[9] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon nanotube electronics," Proceedings of the Ieee, vol. 91, pp. 1772-1784, 2003.

[10] Fabien Pr´egaldiny et.al.,“Compact Modeling and Applications of CNTFETs for Analog and Digital Circuit Design”, IEEE Trans. Elec.dev., pp. 1030–1033, 2006.

[11] Fabien Pr´egaldiny et.al.,“Design Oriented Compact Models for CNTFETs”, IEEE Trans. Elec.dev., 2006.
[12] Paul L.McEuen, Michael Fuhrer, Hongkun Park, “Single walled carbon nano tube Electronics”, IEEE Trans. on Nano Technology, 2002.
[13] Yunfei Gao,”Benchmarking proposed logic technologies against silicon CMOS,” Ph.D. thesis, Purdue University, Dec 2008.
[14] Jing Guo,”Carbon Nanotube electronics modelling, Physics and applications,” Ph.D. dissertation, Purdue University, August 2004.
[15] A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, and H. Dai, “High-Field Quasiballistic Transport in Short Carbon Nanotubes,” Physical Review Letters, vo. 92, pp. 106804, 2004.
[16] J. Guo and M. Lundstrom, "Role of Phonon Scattering In Carbon Nanotube Field-Effect Transistors," Applied Physics Letters, vol. 86, pp. 193103, 2005.
[17] T. A. Fjeldly, T. Ytterdal, M. S. Shur, “Introduction to Device Modeling and Circuit Simulation,” Wiley-Interscience, New York, 1998.
[18] Jingye Xu, “Strategies of Handling Global Signals in Nanometer Integrated Circuits,” University of Illinois at Chicago, 2009

BIO-DATA

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