

# A Simplified Control Strategy for the Shunt Active Power Filter for Harmonic and Reactive Power Compensation

Mohamed Adel Ahmed<sup>1</sup>, Sherif Ahmed Zaid<sup>2</sup>, Osama Ahmed Mahgoub<sup>2</sup>

<sup>1</sup> Banha High Institute of Technology, Banha University, Qalyobia, Egypt.  
PB 13512, Tel. 020110619409, e-mail: madel\_ss@yahoo.com.

<sup>2</sup> Faculty of Engineering, Cairo University, Egypt.

## Abstract

Implementation of a cost-effective practical shunt active power filter (SAPF) depends on microcontroller was the key for developing a simplified control strategy that modifies a previously published one which named on-line compensating method [1]. The objective is to eliminate harmonics and compensate reactive power generated by non-linear loads to improve the power quality. The SAPF is realized using three phase voltage source inverter (VSI) with dc-bus capacitor and the proposed control algorithm is elaborated using a low-cost (Intel 80C196KC) microcontroller. The simulation and experimental results are presented to prove the efficient performance of the SAPF under the proposed controller.

*Keywords: active power filter; non-linear loads; digital control; total harmonic distortion.*

## I. Introduction

Harmonic pollution caused by nonlinear loads such as electric arc furnaces, electric arc welders, adjustable speed drives and switch mode power supplies has been a serious problem in electrical power systems. These loads generate high amount of harmonic currents injected into the power system. The flow of these harmonic currents through the system causes voltage distortion due to harmonic voltage drop across the system series impedance. As a result, not only the harmonic producing loads, but also all of the other loads supplied from the point of common coupling will be affected by this harmonic voltage distortion. The concern of the harmonic distortion is increased because of its unwanted effects such as resonance on series and parallel circuits, additional losses in feeders, transformers and rotating electric machines, maloperation of protection systems, error of measuring instruments, and malfunction and low-efficiency of sensitive loads [2].

Conventionally, passive filters have been used to limit the harmonic currents in power distribution systems. However, they have several drawbacks such as inability to compensate random frequency variations in the currents, degradation of filtering

performance due to parameters variation, tuning problems, and parallel resonance [3]

In order to solve these problems, APF have been designed [4, 5] to cancel the current harmonic distortion by injecting the same detected distortion, but with the opposite polarity, thereby improving the power quality.

This paper presents a modified on-line compensating method for generating the reference current required to the APF circuit for the function of harmonic elimination and reactive power compensation. The principle of operation of both conventional and modified on-line compensating methods is presented with the aid of simulation to prove the effectiveness of the modified method. The experimental prototype of the SAPF under the modified on-line method is implemented using a low-cost (Intel 80C196KC) microcontroller. All control tasks is elaborated digitally to increase the reliability of the system and the control algorithm is written using the assembly language to maximize the controller performance.

## II. General compensation principle of the SAPF

The basic principle of a three-phase shunt active power filter is shown in Fig.(1). The non-linear load current contains fundamental and harmonic components, which can be written as

$$\begin{aligned} i_L(t) &= \sum_{n=1}^{\infty} I_n \sin(n\omega t + \phi_n), \\ &= I_1 \sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \end{aligned} \quad (1)$$

$$i_L(t) = I_{1a} \sin(\omega t) + I_{1r} \cos(\omega t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \quad (2)$$

where  $I_{1a} = I_1 \cos(\phi_1)$  and  $I_{1r} = I_1 \sin(\phi_1)$ .

The terms  $I_{1a} \sin(\omega t)$  and  $I_{1r} \cos(\omega t)$  refer to the active and reactive component of the fundamental load current respectively, and the term  $\sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n)$  refers to load current harmonic components.

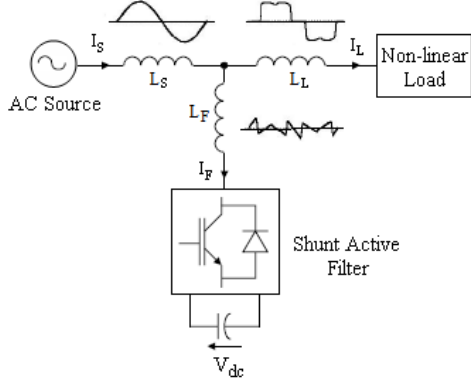


Fig.(1) Compensating Principle of Shunt Active Power Filter.

According to Fig.(1), the source current is given by;

$$i_s(t) = i_L(t) + i_F(t) \quad (3)$$

The perfect SAPF supplies both harmonics and reactive components of the load current, so that the source current supplies only the active component of that current, or  $i_s(t) = I_{1a} \sin(\omega t)$ , therefore the source current will be sinusoidal and in phase with the source voltage. In practice, because of the switching losses in the PWM inverter and the leakage of DC capacitor, the active filter should draw a fundamental active component to maintain the DC capacitor voltage at its desired value. Then, the total current supplied by the AC source will be;

$$i_s(t) = I_{1a} \sin(\omega t) + I_{Floss} = I_s \sin(\omega t) \quad (4)$$

where the  $I_{Floss}$  is the fundamental active component of SAPF current. The amplitude of the source current is obtained over the control of the DC-link voltage.

### III. Operation and Model of SAPF

The three phase SAPF system is shown in Fig.(2). The APF circuit consists of three phase VSI using six IGBT switches, its AC side is connected to the Point of Common Coupling (PCC) through three line inductors  $L_f$  to limit the magnitude of the ripple current of the inverter circuit, and the DC bus is connected to energy storage capacitor  $C_d$ . A three phase diode bridge rectifier, which acts the non-linear load, is connected to PCC through inductors  $L_L$  to limit the large  $di/dt$  of the load current.

The six IGBT-diode combination switches of the VSI can be classified into high-side and low-side switches, forming a conjugate pair per phase. The simultaneous operation of a conjugate pair is not allowed to prevent short circuit faults. At any instant of time, only three of the six switches participate in current conduction. Assuming negligible conduction drops across the switches, equivalent diagram of VSI according to the switching states of (S1 S3 S5) = (0 1 1) is presented in Fig.(3).

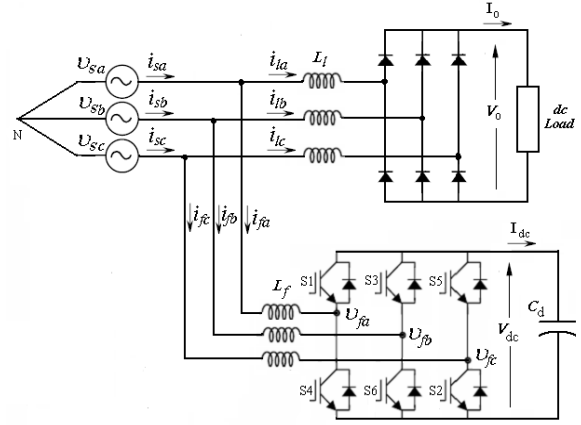


Fig.(2) The three phase SAPF circuit.

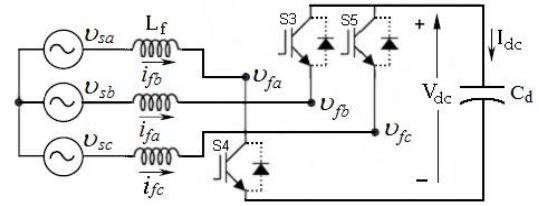


Fig.(3) Representation of a particular switching state for VSI.

The equations representing the switching state of Fig.(3) are developed due to the filter voltage  $v_{fa}$  which takes values of  $(\pm \frac{2}{3} V_{dc})$  or  $(\pm \frac{1}{3} V_{dc})$  depending on the switching state, thus;

$$\frac{di_{fa}}{dt} = \frac{1}{L} (V_{sa} + \frac{2}{3} V_{dc}) \quad (5)$$

$$\frac{di_{fb}}{dt} = \frac{1}{L} (V_{sb} - \frac{1}{3} V_{dc}) \quad (6)$$

$$\frac{di_{fc}}{dt} = \frac{1}{L} (V_{sc} - \frac{1}{3} V_{dc}) \quad (7)$$

Similarly, equations can be generated for the remaining valid switching states according to Table (1)

Table (1) Possible switching states with filter voltages and dc currents

	S <sub>1</sub>	S <sub>3</sub>	S <sub>5</sub>	V <sub>fa</sub>	V <sub>fb</sub>	V <sub>fc</sub>	I <sub>dc</sub>
1	1	0	0	$\frac{2}{3} V_{dc}$	$-\frac{1}{3} V_{dc}$	$-\frac{1}{3} V_{dc}$	$i_{fa}$
2	1	1	0	$\frac{1}{3} V_{dc}$	$\frac{1}{3} V_{dc}$	$-\frac{2}{3} V_{dc}$	$-i_{fb}$
3	0	1	0	$-\frac{1}{3} V_{dc}$	$\frac{2}{3} V_{dc}$	$-\frac{1}{3} V_{dc}$	$i_{fb}$
4	0	1	1	$-\frac{2}{3} V_{dc}$	$\frac{1}{3} V_{dc}$	$\frac{1}{3} V_{dc}$	$-i_{fa}$
5	0	0	1	$-\frac{1}{3} V_{dc}$	$-\frac{1}{3} V_{dc}$	$\frac{2}{3} V_{dc}$	$i_{fc}$
6	1	0	1	$\frac{1}{3} V_{dc}$	$-\frac{2}{3} V_{dc}$	$\frac{1}{3} V_{dc}$	$-i_{fb}$

Filter voltages can be represented as function of switching states as follows;

$$v_{fa} = \frac{V_{dc}}{3} (2S_1 - S_3 - S_5) \quad (8)$$

$$v_{fb} = \frac{V_{dc}}{3} (-S1 + 2S3 - S5) \quad (9)$$

$$v_{fc} = \frac{V_{dc}}{3} (-S1 - S3 + 2S5) \quad (10)$$

where, S1, S3, S5 are the high-side switching functions of the inverter. If the switch is open S is digitally equal to “zero” whereas if it is closed S equals “one”.

The dc-bus voltage can be expressed as;

$$\frac{dV_{dc}}{dt} = \frac{I_{dc}}{C_d} \quad (11)$$

where,  $I_{dc}$  is the dc capacitor current, which can be expressed as;

$$I_{dc} = i_{fa} S1 + i_{fb} S3 + i_{fc} S5 \quad (12)$$

Equations (5-12) are used to develop the APF model under any switching techniques.

#### IV. Control Schemes of SAPF

Many researches have been developed for extracting the reference compensating current required by the filter circuit [6-7]. However, most of these methods require transformation from  $abc$  frame to  $\alpha\beta$  stationary frame or  $dq$  rotating frame. Therefore, the implementation of the SAPF under these methods requires high processing tool such as DSP which is not costly wise.

Implementation of a cost-effective practical SAPF depends on a low cost microcontroller was the key for developing a simplified control strategy that can be presented digitally and elaborated in assembly language of this controller. The on-line compensating method presented in [1], is a simplified method in which the generation of the reference compensating current is done without any transformations. In this paper, useful reductions in some blocks of the conventional on-line compensating method are presented which simplify the control algorithm and reduce the sampling time of the software program.

##### a) Conventional on-line compensating scheme [1]

The block diagram of the conventional on-line compensating scheme is shown in Fig.(4). The distorted load current is filtered using a band-pass filter tuned at the fundamental frequency for extracting its fundamental component. The peak value of the source current is estimated by adding the PI controller output to the peak value of the fundamental load current. The instantaneous reference source current is obtained by multiplying the output of the summing point by a unity sine wave synchronized with the phase-to-neutral source voltage. If the load current is subtracted from the estimated source current, the reference filter current required to compensate harmonic and reactive power is obtained. Then a hysteresis current controller is used to

generate the required switching pattern for the APF power devices.

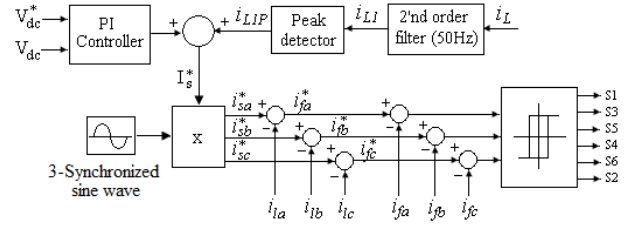


Fig.(4). Block diagram of conventional on-line compensating scheme.

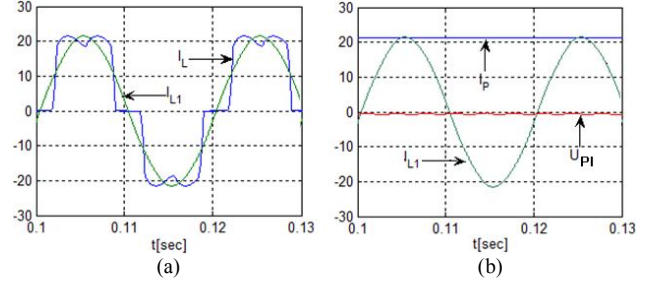


Fig.(5) Principle of conventional on-line compensating scheme,

(a) Load current and its fundamental component,

(b) PI-controller output and peak value of the fundamental current.

As shown in Fig.(5), the output of the PI-controller has a low value that corresponds to the switching losses and the regulation of the DC-bus voltage.

##### b) Modified on-line compensating scheme

Figure (6) shows the block diagram of the modified on-line compensating scheme.

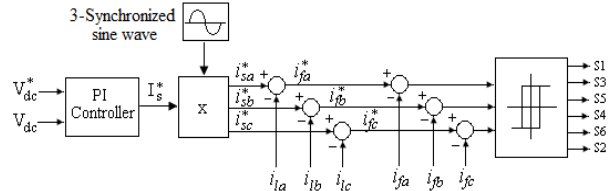


Fig.(6). Block diagram of modified on-line compensating scheme.

The principle of this method is based on the concept of power balance between the source and load. At steady state the real power supplied by the source is equal to the real power consumed by the load plus small power to the APF circuit. Therefore a real power balance is occurred and dc-bus voltage can be maintained at its reference level. If the load is increased, the power balance between will not be sustained. Therefore the real power difference is compensated by the dc capacitor, and the capacitor voltage is decreased from its reference level. In order to keep the dc bus voltage constant, the mains current must increase, and the real power supplied by the source is increased to match the real power consumed by the load. In this manner, the peak value of the source current can be obtained directly over the control of the dc-bus voltage. Thus two blocks can be reduced from

the conventional on-line method (i.e. Band pass filter and peak detection blocks).

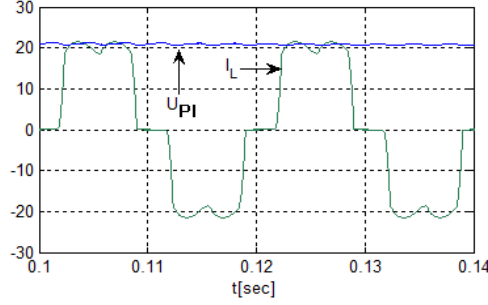


Fig.(7) Principle of modified on-line compensating scheme.

As shown in Fig.(7), the output of the PI-controller represent the peak value of the source current.

Form practical implementation point of view; these reductions are helpful for reducing the sampling time of the software algorithm especially for the use of low speed microcontrollers.

## V. Design and Simulation of SAPF

The power circuit of active filter is a pulse width modulated three phase voltage source inverter typically based on fast switching devices. To design the APF power circuit, it is necessary to select the semiconductor devices, select the value of inductor  $L_f$ , dc-bus voltage  $V_{dc}$ , dc-side capacitor  $C_{dc}$ , and switching frequency by considering the maximum capacity of active filter.

### Selection of the filter line inductor $L_f$

The performance of the SHAPF is strongly affected by the line inductor  $L_f$  where the current passing through it must track the reference signal of the harmonic component of the supply current. The large value of  $L_f$  makes the rate of change of the current is going to be small, and hence tracking the reference signal will be lost. On the other hand, for small  $L_f$  value, a good tracking will be achieved but the switching frequency will be increased, which is limited by the switching capability of the power devices and switching power losses of the inverter circuit.

Considering the ripple value of the filter current, the line inductor can be calculated by [8];

$$L_f = \frac{V_s}{2\sqrt{6} \cdot f_s \cdot \Delta I_{f \max}} \quad (13)$$

where  $V_s$  is the rms value of the phase voltage and  $\Delta I_{f \max}$  is the maximum ripple current, and is considered to be 15% of peak filter current.

### Selection of the dc-side Capacitor $C_d$ and dc-side Voltage $V_{dc}$

The dc-side capacitor value of the APF is another important parameter. With a small capacitance, large

ripples at the steady state and wide fluctuation at the transient conditions are observed in the dc-side voltage. While a higher capacitance reduces the ripples and fluctuations in the dc-side voltage, but increases the cost and size of the filter.

The selection of  $C_d$  can be governed by reducing the voltage ripple of the dc-bus voltage. As per the specification of peak-to-peak voltage ripple ( $V_{dcp-p}$ ) and rated filter current ( $I_{f1}$ ) the dc-side capacitor can be found from [9];

$$C_d = \frac{\pi \cdot I_{f1}}{\sqrt{3} \cdot \omega \cdot V_{dcp-p}} \quad (14)$$

where,  $V_{dcp-p}$  is the peak-to-peak voltage ripple and  $I_{f1}$  rated filter current.

For linear modulation mode of the PWM inverter, in which  $0 \leq m_a \leq 1$ , the dc-bus voltage can be written as [10];

$$V_{dc} \geq \frac{2\sqrt{2}V_s}{m_a} \quad (15)$$

### Selecting the Switching Frequency

The switching frequency is selected based on the highest order of harmonic to be compensated. Theoretically it is possible to control the harmonics up to half the switching frequency. Therefore the switching frequency must be at least twice the highest order harmonic frequency to be compensated. Other factors like switching ripple filters, switching characteristics and losses of the power module also influence the selection of the switching frequency.

According to the previous design procedures, a case study for 10KVA compensation capacity, 220V/50Hz system, and average switching frequency of 10KHz, gives SHAPF parameters as;  $L_f=5mH$ ,  $V_{dc}=800V$ , and  $C_d=1000\mu F$ .

Figure (8) shows the distorted waveform of the line current drawn by non-linear load.

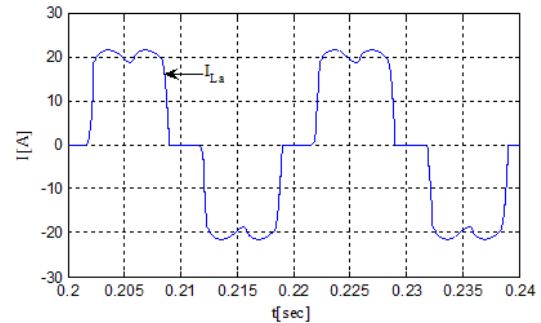


Fig.(8) Non-linear load current waveform.

According to the harmonic spectrum shown in Fig.(9), the non-load current has a THD value of 26.91% with high amplitudes of the low order harmonics.

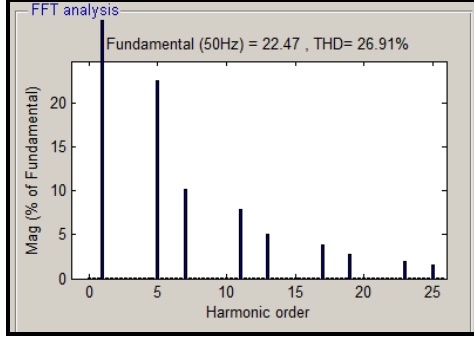


Fig.(9) Harmonic spectrum of the non-linear load current.

The steady state performance of SAPF according to the modified on-line compensating method is shown in Fig.(10). The source current has sinusoidal current waveform and in phase with the source voltage.

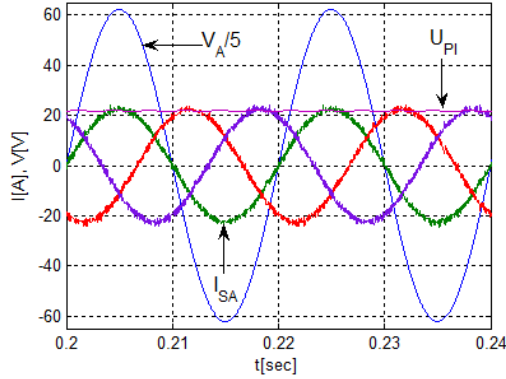


Fig.(10) Steady state performance of SAPF according to modified on-line compensating method.

According to the harmonic spectrum shown in Fig.(11), the source current has a low THD value of 1.16% with low amplitudes of the low order harmonics.

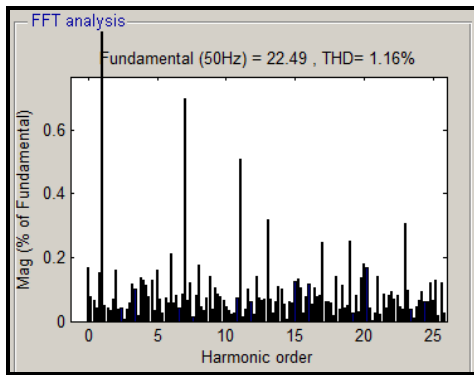


Fig.(11) Harmonic spectrum of the source current after compensation.

The transient response of the SHAPF system for a step change in load current is presented according to modified on-line compensating method in Fig.(12) and conventional on-line compensating method in Fig.(13).

According to Fig.(12), the settling time of the dc-bus voltage is within three cycles without overshoot, while

in Fig.(13) the settling time is within five cycles with an overshoot of 25V.

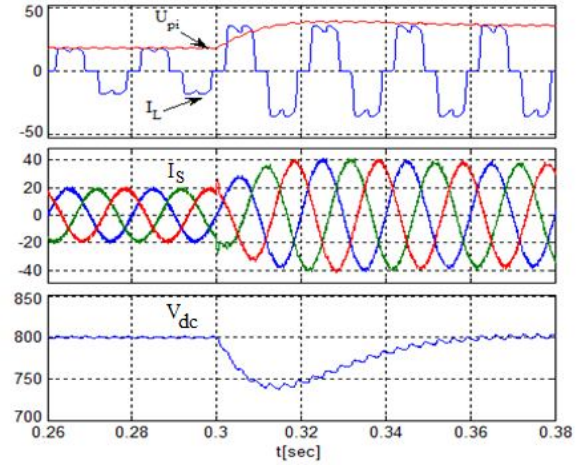


Fig.(12) Transient response of SAPF according to modified on-line compensating method.

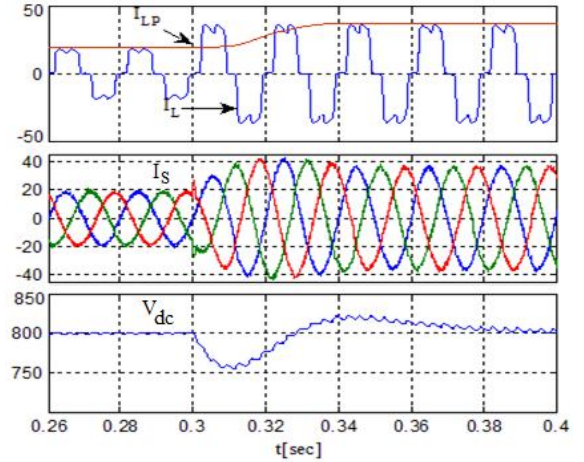


Fig.(13) Transient response of SAPF according to conventional on-line compensating method.

## VI. EXPERIMENTAL SETUP

The block diagram of the proposed experimental setup is shown in Fig.(14). Principle connections between the different elements in the complete system are indicated. The software algorithm is implemented using Intel 80C196KC 16-bit embedded microcontroller. This microcontroller provides an A/D converter with multiplexed eight-input channels, which is used for the various A/D operations required by the controller algorithm. The output ports provided by the 80196 microcontroller are used for interfacing the switching signals to the IGBT drivers. The flowchart of the implemented algorithm is shown in Fig.(15). The high-speed input unit (HSI) is used for phase voltage zero-crossing detection. A unity sine wave is stored as a lookup table (LUT) in the microcontroller memory. The pointer of the LUT starts with zero count every zero-crossing transitions and then incremented every



sampling period. These enable the formation of a phase-locked loop (PLL) for the current controller, which, thus, tracks the grid frequency.

The control algorithm is implemented digitally to increase the reliability of the system.

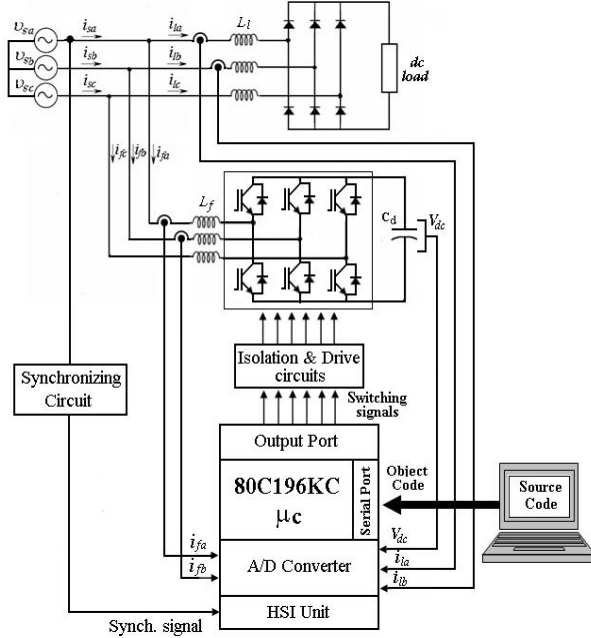


Fig.(14) Block diagram of the experimental setup.

Figure (16) shows the experimental waveforms of load current, filter current, source current, and supply voltage. The load current has a low quality waveform with high THD value of 17.45% and PF of 0.88 as shown in the harmonic spectrum in Fig.(17).

After compensation by SAPF, the source current is in phase with system supply voltage and has a low THD value of 5.05% and PF of 0.986 as shown in the harmonic spectrum in Fig.(18).

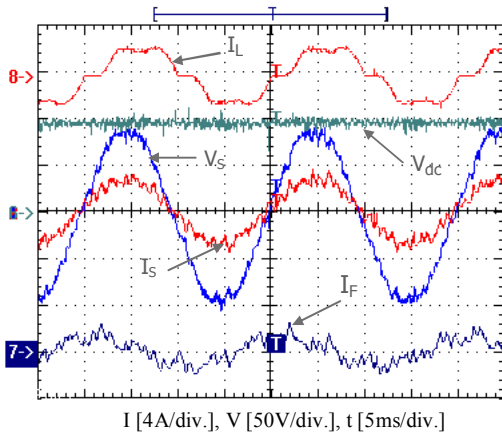


Fig.(16) Experimental waveforms of load current, filter current, source current, and supply voltage.

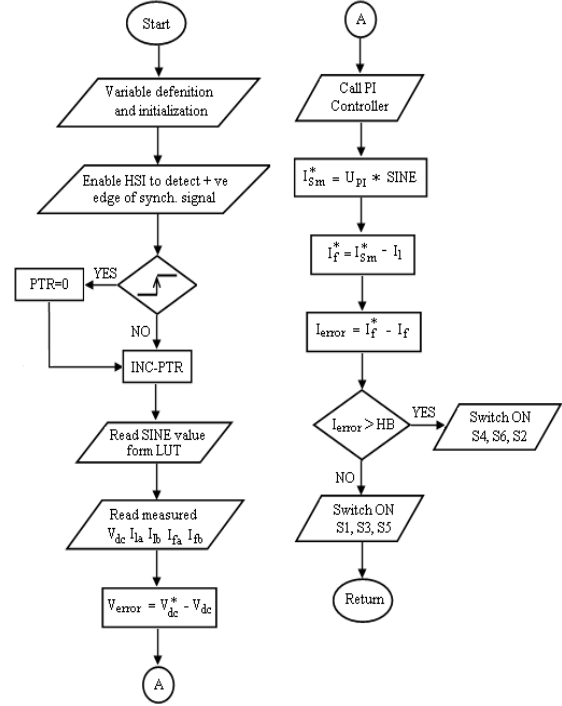


Fig.(15) Flowchart of the software algorithm.

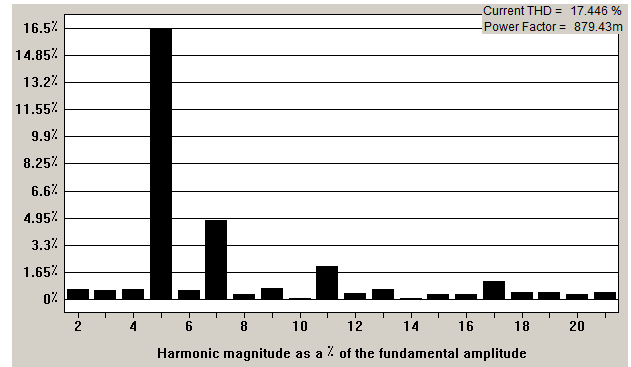


Fig.(17) Harmonic spectrum of the source current before compensation.

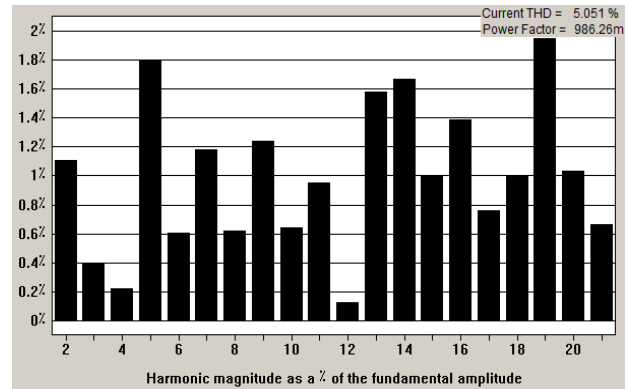


Fig.(18) Harmonic spectrum of the source current before compensation.

## VII. CONCLUSION

A high performance three-phase shunt active power filter with a simplified control algorithm has been implemented using a single chip Intel 80C196KC microcontroller. A useful modification applied to the conventional on-line compensating method helps to reduce the control algorithm and increase the sampling rate of data, which in turn improves the performance of the system. The software program of the experimental prototype is elaborated directly in assembly language to maximize the controller performance. The obtained experimental results prove that the source current after compensation has sinusoidal waveform with low THD value of 5.05% and PF of 0.986.

## VIII References

- [1] Luis A. Moran, Juan W. Dixon, and Rogel R. Wallace, "A Three-phase Active Power Filter Operating with Fixed Switching Frequency for Reactive Power and Current Harmonic Compensation," IEEE Trans. Ind. Elec., Vol. 42, No. 4, pp. 402-408, August 1995.
- [2] K. W. Louie, P. Wilson, R. A. Rivas, A. Wang, and P. Buchanan, "Discussion on Power System Harmonic Analysis in the Frequency Domain," IEEE PES Transmission and Distribution Conference and Exposition Latin America, Venezuela. 2006
- [3] H. Fujita, T. amasaki, and W. Akagi, "A Hybrid Active Filter for Damping of Harmonic Resonance in Industrial Power Systems," IEEE Transaction on Power Electronics, Vol. 15, No. 2, pp. 215-222, 2000.
- [4] H. Akagi, "New trends in active filters for power conditioning," IEEE Transaction on Industrial Application, Vol.32, No.6, pp. 1312-1322, 1996.
- [5] B. S. Rajpurohit and S. N. Singh, "Performance Evaluation of Current Control Algorithms Used for Active Power Filters," EUROCON, The International Conference on "Computer as a Tool" Warsaw, September, pp.2570-2575, 2007.
- [6] H. Akagi, Kanazawa, Yoshihira; Nabae, Akira, "Instantaneous reactive power compensators comprising switching devices without energy storage components," IEEE Transactions on Industry Applications, Vol. IA-20, No. 3, pp. 625-630, 1984.
- [7] S. Bhattacharya, and D. Divan, "Synchronous frame based controller implementation for a hybrid series active filter system", IEEE Industry Applications Conference, IAS '95, Vol. 3, pp. 2531-2540, 1995.
- [8] S. Ponnaluri, A. Brickwedde, "Generalized System Design of Three phase Active filters," IEEE Power Electronics Specialist Conference, PESC, Vol. 3, pp 1414-1419, 2001.
- [9] S. J. Chiang and J. M. Chang, "Design and Implementation of the Parallelable Active Power Filter", IEEE Power Electronics Specialists Conference, PESC 99, Vol. 1, pp.406-411, 1999.
- [10] N. Mohan, T.M. Undeland and W.P. Robbins, Power Electronics: Converters, Applications and Design, John Wiley & Sons, third edition.