DESIGN AND IMPLEMENTATION OF FLYBACK CONVERTER WITH SYNCHRONOUS RECTIFICATION FOR SATELLITE ELECTRIC POWER SYSTEMS

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Abstract: *The DC-DC switching mode converter for an electric power system (EPS) to provide a regulated voltage is one of the important components of a satellite mission and subsystem. The flyback converter is one of the most attractive isolated converters in SMPS applications because of its simple configuration, less component count and cost effectiveness. This present work describes the recent EPS structure and implementation of flyback converter based on self-synchronous rectification with suitable choices of interface driver with secondary side, as it features a low cost and high efficiency. The steady-state analysis and operating principle of the synchronous rectifier flyback converter is presented. The characteristics of a 50W (5V, 10A) output prototype converter are implemented and verified experimentally with a 20 V to 45 V maximum power point tracking (MPPT) based photo voltaic (PV) dc-dc converter output. This presented design illustrates an example for a future space-grade isolated intermediary bus converter of commercial communication satellites. The various design factors for space applications are considered while designing and are implemented successfully.*

Key words: *EPS, PV, MPPT, SMPS, Flyback, Synchronous Rectifier, PWM controller, Space, Driver*

1. Introduction

In most of the low wattage isolated SMPS applications, the single-stage Flyback converter is extensively used because of its simple structure and low cost [1],[2]. This converter is a very attractive solution due to the absence of output filter inductor and transformer reset circuit and employing only one power switch and output rectifier diode. However, the design with low magnetizing inductance can minimize the transformer size but increases the primary peak current which intern increases the switch turn off loss and conduction loss [2]. The high conduction losses of the output rectifier diode result in low power conversion efficiency.

Hence to minimize both switching losses on the primary switch and conduction losses on the secondary rectifier diode, certain techniques of improvement such as using synchronous rectifier on secondary side is widely used [3],[4]. The present works employ design and implementation of synchronous rectifier flyback converter to achieve high conversion efficiency for space applications. The increased use of ultra-low drain source resistance, R_{ds}(on) MOSFETs based synchronous rectification has an attractive solution than passive Schottky rectification [5],[6],[7]. It is proved that for less than 40A, synchronous rectifiers have less conduction loss than Schottky diodes.

The topologies of synchronous rectifier flyback converter can be classified based on control method as primary isolated gate drive control and self-driven control based synchronous rectifier.

The self-driven control-based topology is a widely used feature as it requires simple gate driving logic, absence of complex control circuits, cost-effective solution and can be easily realized by additional winding or through self-synchronous driver circuit [8]. However, the control timing is not accurate in the self-driven synchronous rectifier driver circuit. Hence the improvement of the system efficiency is limited, and it is mainly used in low frequency applications. In this mode of operation, when the primary switch is turned on, the gate to source voltage across the secondary synchronous switch is negative and hence it is turned off. Similarly, when the primary switch is turned off, the gate to source voltage across the secondary synchronous switch is positive and hence it is turned on.

External gate control drive synchronous rectifier is a very common topology with improved control accuracy and increased circuit complexity. The efficiency of the converter is sensitive to the dead time and is greatly affected due to conduction of body diode. Hence the dead time is maintained shortly to minimize the turn on time of body diode but increases the control complexity and cost.

The main objective of the presented paper is to design and implement an efficient method of synchronous rectifier flyback converter by using an analogue integrated circuit. The designed converter is used for satellite EPS power distribution converter [15],[16],[17]. The goal of the design is to demonstrate that an optimized distributed EPS can be realized such that the efficiencies of the distributed power dc-dc converter design are not significantly different than the inherently non-optimized converters [18].

The proposed structure of the EPS system is presented in section 2. Brief description and analysis of the MPPT dc-dc converter system is given in section 3. Section 4 describes the proposed dc-dc flyback converter, and their steady analysis. Section 5 illustrates the design criteria of the flyback converter. Section 6 presents the simulation details and experimental hardware prototype results of the synchronous rectifier flyback converter. Finally, the conclusion is presented in section 7.

This presented work has focused into following important contributions,

1) A new variation of a PV-MPPT dc-dc flyback converter integration system for satellite EPS.
2) The application of MPPT dc-dc converter with improved dynamic response controller.
3) The dynamic interaction among the MPPT controller, dc-dc flyback converter and loads.
4) Mitigation of low frequency bus voltage oscillations reflecting to the PV bus.

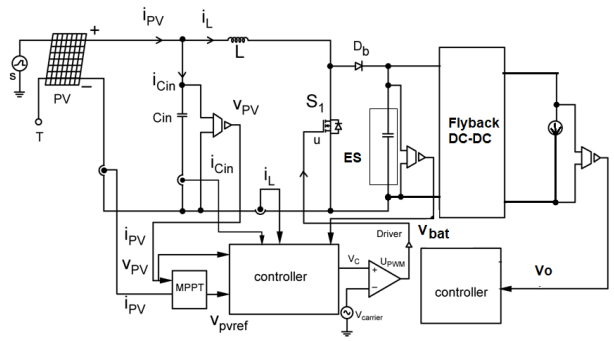


Figure 1. EPS architecture

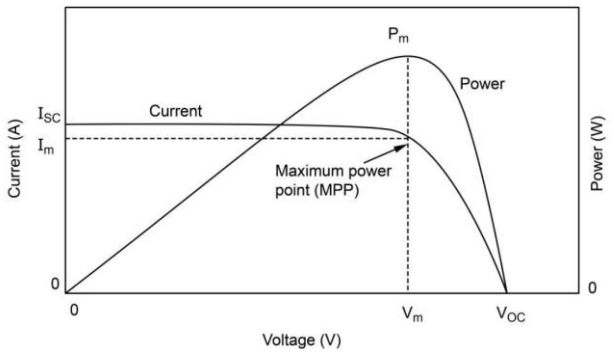


Figure 2. MPP Operation of PV Array

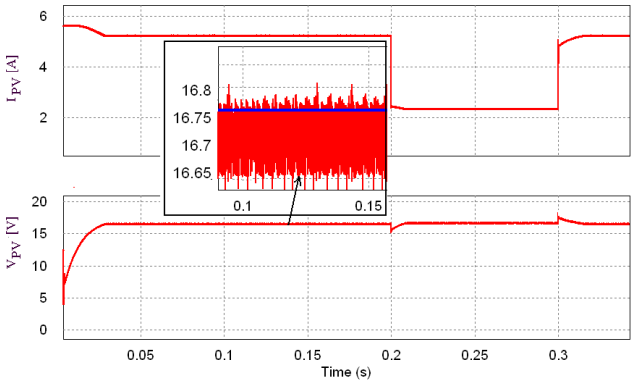


Figure 3. Tracked PV current and PV voltage

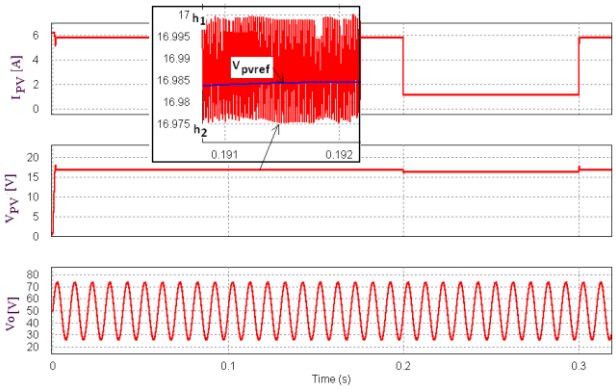


Figure 4. Tracked PV current and PV voltage

2. DESCRIPTION OF THE PROPOSED STRUCTURE OF EPS SYSTEM

The proposed structure of the satellite EPS system shown in Figure 1 are the PV source used to convert the solar energy to electrical energy, MPPT converter for power regulation and control, energy storage (ES) system typically rechargeable batteries and power distribution system. The power distribution system of a typical dc-dc converter is considered as a part of the EPS in modern satellite systems. High efficiency MPPT converters based on fixed frequency nonlinear controllers are used for regulation and control [14],[17].

The MPPT architecture consists of a dc-dc regulator usually buck, boost or buck boost converter between the PV array and the loads. The MPPT converter regulates the voltage (V_{pv}) and current (I_{pv}) extracted from the array such that it maintains its Maximum Power Point called as (MPP). Advantages of this MPPT based architecture is that the PV array can be decoupled from the load, permitting simpler array designs.

To utilize the energy provided by the PV panel maximally, its operating point must be kept at the maximum called MPP as represented in Figure 2. From Figure 2 the point near the knee of the I-V curve is called the MPP in which the voltage and current at

the MPP are designated as V_m and I_m. Figure 3 shows the illustration of MPPT architecture with tracking performance of PV current and PV voltage with different environmental conditions. Similarly Figure 4 shows the tracked PV voltage and converter output voltage (typical 24V to 70V bus system) under different environmental conditions. The bus voltage is unregulated during the eclipse portion of the orbit. The battery state of charge regulates the bus voltage for this time period.

This bus voltage is further regulated down to the different voltage levels and is distributed to the various loads of the satellite and power required by modern electronic components.

3. DESCRIPTION OF MPPT DC-DC CONVERTER

The dc-dc converters are widely employed to "match" the load impedance to the panel equivalent impedance to maximize the power drawn from the PV panel. Power circuit diagrams of the MPPT boost converter shown in Figure 1, includes PV module voltage V_{PV}, input capacitor C_{in}, inductor L, power switch S_1, output capacitor C_o, diode D_o and load impedance.

During the on condition of power switch S_1 shown in Figure 5 (a), the input PV voltage source V_{PV} supplies energy to the inductor L and the diode D_o is reverse biased. Also, the increase in supply current flows through the inductor L, capacitor C_o and releases energy to output load terminals.

During the off condition of power switch S_1 shown in Figure. 5 (b) the diode D_o is forward biased due to the energy stored in the inductor L. The input PV voltage source V_{PV}, and the inductor L supply energy to load terminal through the capacitor C_o and the diode D_o.

3.1 Gain of the Boost Converter

The voltage on capacitor C_o can be derived from energy balance on inductor L during on and off periods of switch S_1 and can be written as:

$$\frac{1}{T}\int_0^{t_{on}} V_{PV}\ dt = \frac{1}{T}\int_0^{t_{off}} (V_O - V_{PV})\ dt$$

$$\frac{1}{T}\int_0^{dT} V_{PV}\ dt = \frac{1}{T}\int_0^{(1-d)T} (V_O - V_{PV})\ dt$$

$$V_O = \frac{1}{(1-d)} V_{PV} \qquad (1)$$

where d is duty cycle of boost converter.

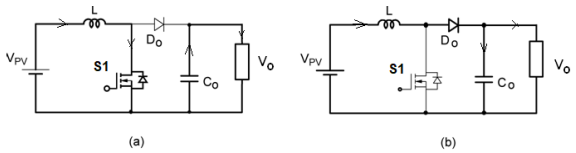


Figure 5. Steady-state Operating Modes of Boost converter (a) S_1 ON (b) S_1 OFF

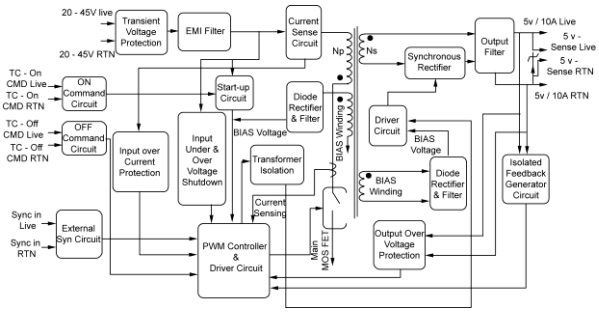


Figure 6. Functional block of a flyback converter with synchronous rectification

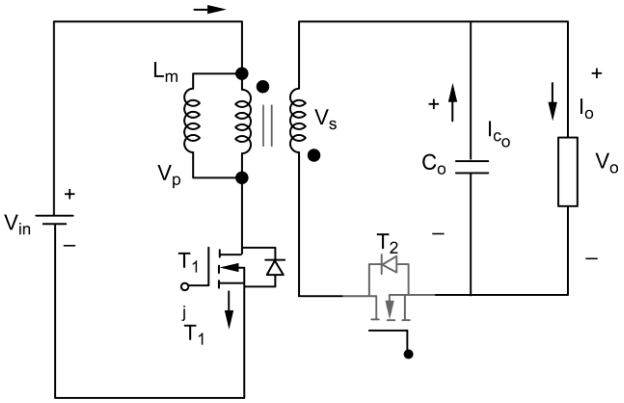


Figure 7(a). Mode 1 operation (T1 is on and T2 is off).

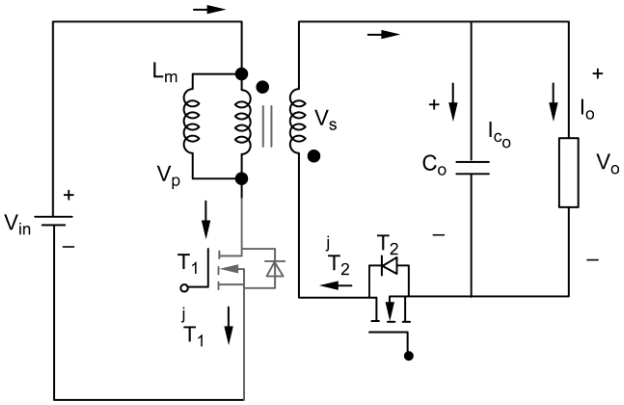


Figure 7(b). Mode 2 operation (T_1 is off and T_2 is on)

4. DESCRIPTION OF PROPOSED FLYBACK DC-DC CONVERTER

The flyback dc-dc converter is usually employed between bus voltage and various loads as less weight,

low cost, tight regulations, high reliability, and high efficiency. The functional block representation of synchronous rectifier flyback converter is shown in Figure 6. The proposed structure consists of a synchronous rectifier flyback converter as shown in Figure 7.

The magnetic isolated feedback generator circuit (using UC2901) senses the output voltage and provides isolated feedback to the PWM controller (UC2825) to complete the control loop. The power circuit schematic for a synchronous rectifier flyback converter with low-side configuration at the output is shown in Figure 7. When the primary MOSFET T_1 is turned off, the secondary current will flow through the body diode of the synchronous MOSFET T_2 which is analogous to the current flowing through the conventional output diode rectification.

4.1 STEADY STATE OPERATIN OF FLYBACK CONVERTER

From power circuit diagram of the dc-dc flyback converter shown in Figures 7, include input voltage V_{in}, main switch T_1, synchronous rectifier switch T_2, isolation transformer, magnetizing inductance L_m, output capacitor C_O and load impedance r_o. Two operating modes are analyzed under steady-state operation.

During mode 1 operation of the converter, main switch T_1 is turned on and synchronous switch T_2 is turned off as shown in Figure 7. (a). The input voltage source V_{in} supplies energy to the magnetizing inductance L_m of transformer. The energy stored in capacitor C_O releases energy to output load terminals.

During mode 2 operation of converter main switch T_1 is turned off and auxiliary switch T_2 is turned on as shown in Figure 7. (b). During on condition of power switch T_2, the secondary current will flow through the body diode of the synchronous MOSFET T_2, which is analogous to the current flowing through the conventional output diode rectification. The magnetizing inductance L_m supply energy to load terminal through the capacitor C_O and the body diode of T_2.

4.1.1 Input and Output Voltage Relation

The output voltage on capacitor C_O can be derived from energy balance on magnetizing inductor L_m during on(t_{on}) and off periods(t_{off}) of main switch T_1 and can be written as:

$$\frac{1}{T}\int_0^{t_{on}} v_L dt = \frac{1}{T}\int_0^{t_{off}} n\, v_s\, dt$$

$$\frac{1}{T}\int_0^{dT} V_{in}\, dt = \frac{1}{T}\int_0^{(1-d)T} n\, V_O\, dt\,; \quad v_s = n\, V_O$$

$$V_{in}\, dT = n\, V_O (1-d)T$$

$$V_O = \frac{V_{in}}{n}\frac{d}{(1-d)} \qquad (2)$$

Where, d is duty cycle of flyback converter and 'n' is the primary to secondary turns ratio of flyback transformer.

5. DESIGN CONSIDERATIONS

5.1 Switching Frequency

The choices of switching frequency selection have a crucial parameter between efficiency and bandwidth. The selection of higher switching frequencies will have more bandwidth, but a lower efficiency at lower switching frequencies [8],[9],[10]. The sufficient values of timing resistor (R_T) and timing capacitor (C_T) in PWM controller chip (UC2825) determines the desired switching frequency of the converter.

5.2 Transformer Design

The two major parameters in the design of flyback transformer are turns ratio and magnetizing inductance [5]. The equation (2) describes the relation between the turns ratio as a function of maximum duty cycle (d_{max}) with minimum input voltage.

$$V_O = \frac{V_{in\_\min}}{n}\frac{d_{\max}}{(1-d_{\max})};$$

Where; $n = \frac{N_p}{N_s}$ (3)

5.3 Primary peak current (I_{pp})

$$I_{pp} = \frac{I_o}{n}\frac{1}{(1-d_{\max})} + \frac{\Delta I_L}{2}; \qquad (4)$$

where $\Delta I_L = \frac{I_{pp}}{2}$ in CCM operation.

5.4 Peak to Peak ripple current (ΔI_L)

Peak to peak ripple current of magnetizing inductance is.

$$\Delta I_L = \frac{V_{in\_\min}\, d_{\max}}{L_m f_s} \quad (5)$$

5.5 Minimum number of primary turns

$$N_P = \frac{L_m\, I_{pp}}{B_m A_e} \quad (6)$$

5.6 Number of secondary turns

$$n = \frac{N_p}{N_s};\ N_s = \frac{N_p}{n} \quad (7)$$

5.7 Primary RMS current

$$I_{prms} = I_{pp}\sqrt{\frac{D_{\max}}{3}} \quad (8)$$

5.8 Secondary RMS current

$$I_{srms} = I_{sp}\sqrt{\frac{1-D_{\max}}{3}} \quad (9)$$

5.9 Synchronous Rectifier MOSFET Selection

The voltage stress of primary MOSFET can be calculated as

$$V_{ds1} = V_{in\_\max} + V_F \quad (10)$$

The voltage stress of SR-MOSFET can be calculated as

$$V_{ds2} = \frac{V_{in\_\max}}{n} + V_o \quad (11)$$

The current stress is equal to the secondary peak current. The power loss in the SR-MOSFET can be calculated as below:

5.10 Output Capacitor

The following equation describes the calculation of desired value of output capacitor with the desired output voltage ripple.

$$C_o = \frac{(I_{spk} - I_o)^2 (1 - D_{\max})}{2\Delta V_o I_{spk} f_s} \quad (12)$$

The ESR of the capacitor considering the output voltage ripple and can be calculated as,

$$\Delta V_o = ESR\ (I_{spk} - I_o) \quad (13)$$

The operation of flyback converter in CCM has lesser peak current than operating in DCM. Hence the ESR is the main criteria for output capacitor selection. In this design, the output voltage ripple must be less than 200mV with approximately 10A of secondary side ripple current. A capacitor with an ESR less than 15m-Ohm is required.

5.11 Current Sensing and Slope Compensation

The ripple current of the converter is sensed by the current transformer (CT) and makes to shut down the converter if sensed current is too high. The threshold voltage level of the current sensing (CS) pin is 1 V.

5.12 Feedback Loop Compensation

The Feedback loop compensation of converter is used to prevent oscillation. The design of loop compensation in CCM Flyback is complicated compared to DCM, due to the existence of right half plane zero in the power design stage [11]. A PID-type-3 compensation is required for achieving stability and sufficient faster response. A detailed discussion and analysis about feedback loop compensation can be well presented on [12]. The PID controller loop is constructed using UC2825 PWM controller. The controller gains are tuned in order to mainatin stability and regulation at all conditions of perturbations in output load and input voltage [13],[14].

Table 1. System Specifications and Components

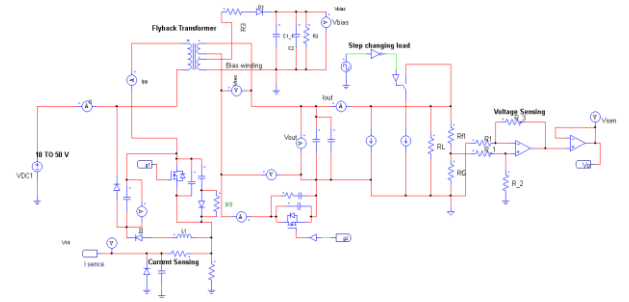
Parameter/Components	**Values**
Input voltage	20 V to 45 V
Output voltage	5 V
Output current	10A
Output power	50W
Switching frequency of magnetic isolation	500 KHz
Switching frequency of PWM controller	150 KHz
Band width	2 KHz
Maximum duty cycle	0.45
Transformer ratio (n)	1.3
Magnetizing inductance (L_m)	15µH
Primary peak ripple current (I_{pp})	10A
MOSFETs T_1 and T_2	IPB107N20N3 G, IPI075N15N3 G
Output capacitor C_o	940µF
PWM controller	UC2825
Main switch driver	UCC27512
Synchronous MOSFET driver	UCC27511

6. SIMULATION & EXPERIMENTAL RESULTS

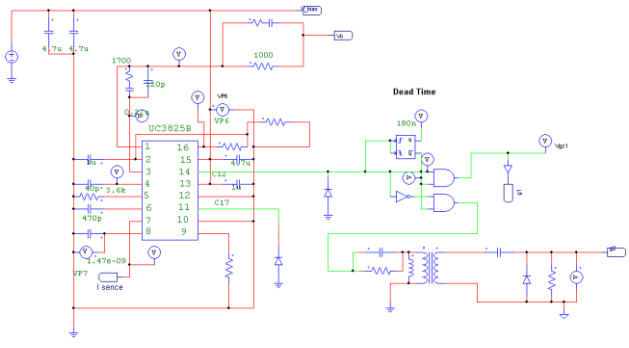
The features of the synchronous rectifier flyback converter for EPS architecture are verified with the various simulation studies performed. The parameter considered for simulation studies are

represented in Table.1. The implemented simulation schematic is represented in Fig. 8. In simulation studies, the flyback transformer is considering as a magnetic inductor L_m, and leakage inductor L_k.

The simulation studies are performed with various values of input voltage and load current. Figure.9 represents the simulated switching voltage waveform of primary MOSFET and secondary synchronous MOSFET and its gating signal at 20V input with a load current of 5A. The simulation results are presented in Figures 10 and 11 represents the switch voltage of primary MOSFET, primary peak current and gating signal with input voltage of 20V at load current of 5A and 10A respectively. Similarly, the Figures 12 and 13 represent the simulated switching voltage waveform of primary MOSFET and secondary synchronous MOSFET and its gating signal at 45V input with a load current of 5A and 10A respectively. The simulation results are presented in Figures 14 and 15 represents the switching voltage of primary MOSFET, primary peak current and gating signal with input voltage of 45V at load current of 5A and 10A respectively. Simulation result of output voltage (Vo) with step change in load current of 5A to 10A is shown in Figure.16.



(a)



(b)

Figure 8. Simulation scheme of proposed 50W synchronous rectifier flyback converter (a) power circuit (b) PWM controller circuit.

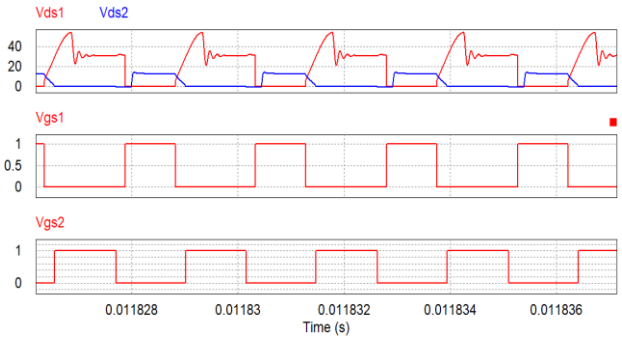


Figure 9. Simulation results of switch voltages (Vds1 and V_{ds2}) and per unit gating signals (V_{gs1} and V_{gs2}) at V_{in}:20V and I_{load}:5A).

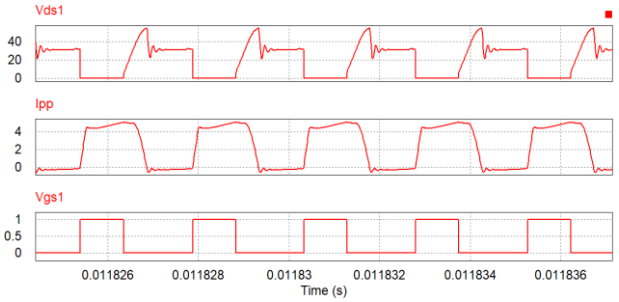


Figure 10. Simulation results of main switch voltage (V_{ds1}), primary peak current (I_{pp}) and per unit gating signals (V_{gs1}) at V_{in}:20V and I_{load}:5A).

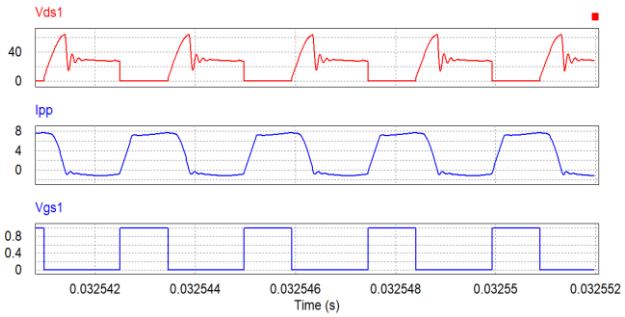


Figure 11. Simulation results of main switch voltage (V_{ds1}), primary peak current (I_{pp}) and per unit gating signals (V_{gs1}) at V_{in}:20V and I_{load}:10A).

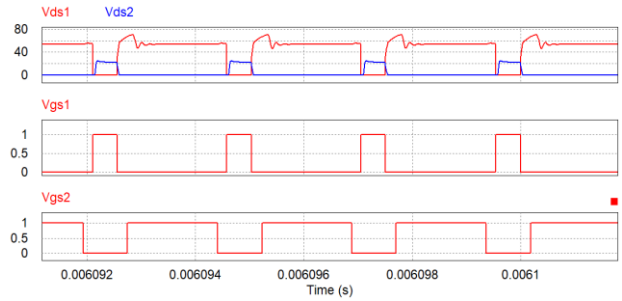


Figure 12. Simulation results of switch voltages (V_{ds1} and V_{ds2}) and per unit gating signals (Vgs1 and V_{gs2}) at V_{in}:45V and I_{load}:5A).

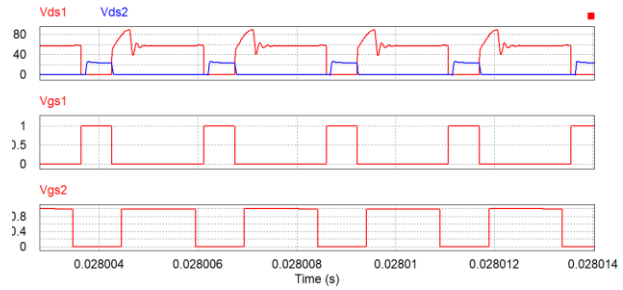


Figure 13. Simulation results of switch voltages (V_{ds1} and V_{ds2}) and per unit gating signals (V_{gs1} and V_{gs2}) at V_{in}:45V and I_{load}:10A).

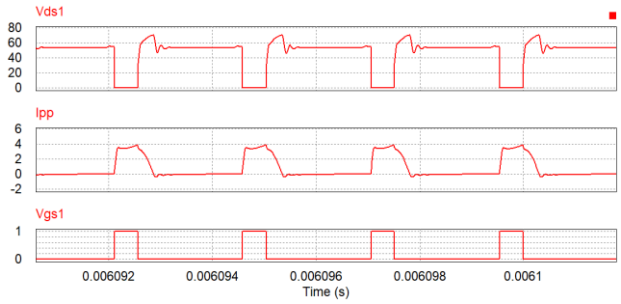


Figure 14. Simulation results of main switch voltage (V_{ds1}), primary peak current (I_{pp}) and per unit gating signals (V_{gs1}) at V_{in}:45V and I_{load}:5A).

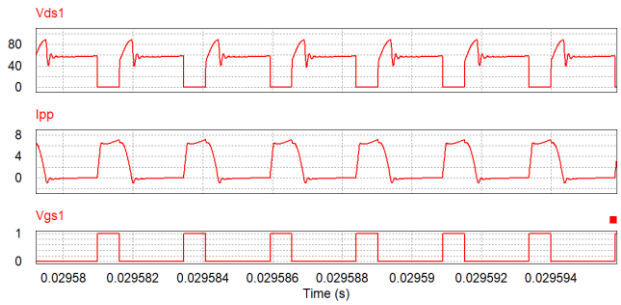


Figure 15. Simulation results of main switch voltage (V_{ds1}), primary peak current (I_{pp}) and per unit gating signals (V_{gs1}) at V_{in}:45V and I_{load}:10A).

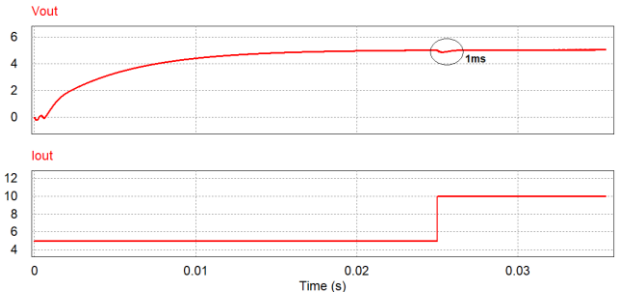


Figure 16. Simulation results of output voltage (Vo) with step change in load current of 5A to 10A.

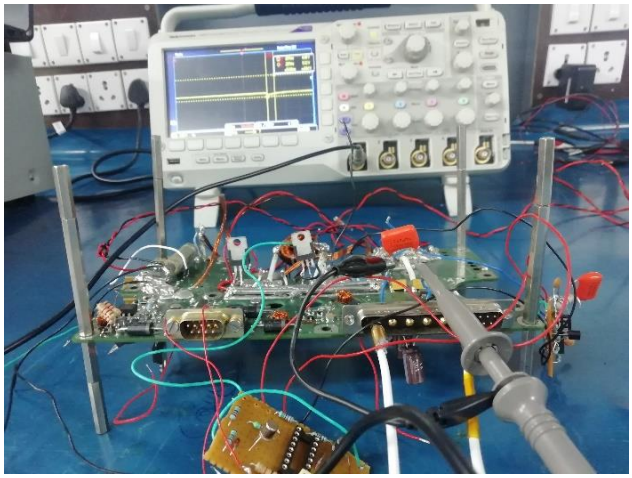


Figure.17 Experimental hardware prototype (BBM) test bench.

The designed flyback converter shown in simulation circuit of Figure.8 has been implemented in experimental hardware prototype. Figure. 17 shows the test bench setup of designed 50W prototype of the flyback converter. The specifications and key parameters of the designed prototype are shown in Table 1. Choices of a selection of a Flyback converter PWM controller and driver circuit mainly depends on precise requirements and certain design consideration such as cost, size, and various design form factor, respectively. Also, the requirements such as undervoltage, overvoltage, over current protection features, and standby power are easily be met by selecting the sufficient controller. UCC27511 is a compact driver IC which is configured to drive secondary synchronous power MOSFETs in this design. The presented driver IC has a feature to control single or cascaded MOSFETs to match the behavior of Schottky rectifiers.

Figure 18 represents the switching voltage and gating signal of the main switch with minimum input voltage (20V) at full load condition. Similarly Figure 19 represents the switching voltage and gating signal of synchronous MOSFET with minimum input voltage (20V) at full load condition.

Figure 20 represents the switching voltage of both main MOSFET and synchronous MOSFET with minimum input voltage (20V) at full load condition.

Figure 21 shows the gating signal of both main MOSFET and synchronous MOSFET with minimum input voltage (20V) at full load condition.

Similarly, Figures 22 to 25 represents the switching voltage and gating signal of main and synchronous MOSFET with maximum input voltage (45V) at full load condition.

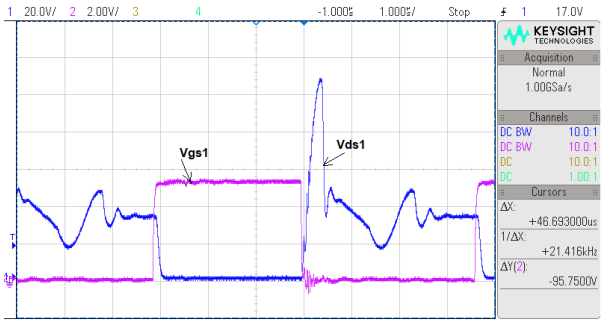


Figure18. Main switch voltage V_{ds1} and gating signal V_{gs1} at V_{in}:20V and I_{load}:10A).

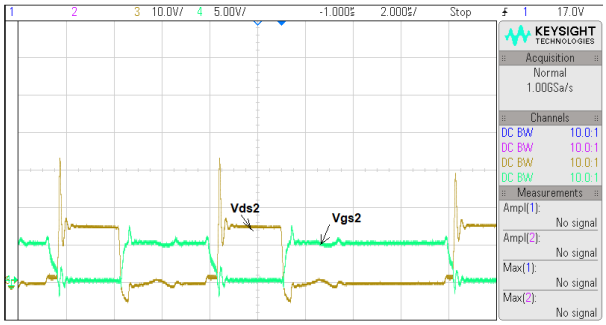


Figure 19. Synchronous switch voltage V_{ds2} and gating signal V_{gs2} V_{in}:20V and I_{load}:10A).

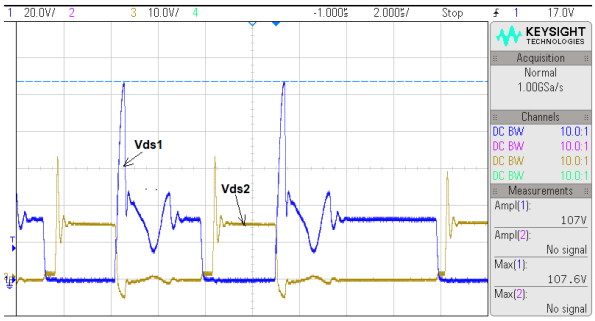


Figure 20. Switching voltage of main switch V_{ds1} and synchronous switch V_{ds2} (V_{in}:20V and I_{load}:10A).

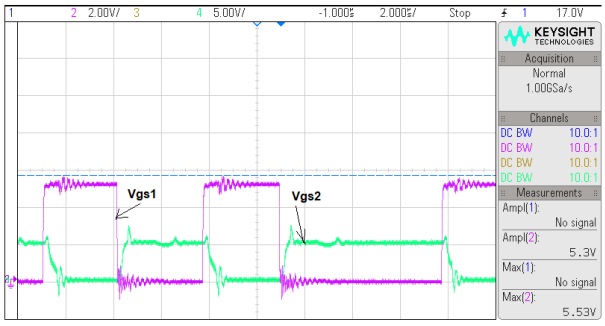


Figure.21 Gating signal of main switch V_{gs1} and synchronous switch V_{gs2} V_{in}:20V and I_{load}:10A).

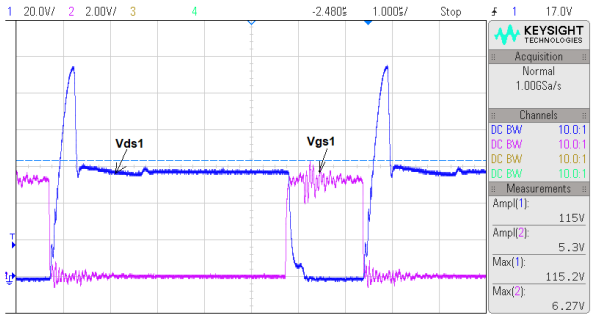


Figure 22. Main switch voltage V_{ds1} and gating signal V_{gs1} V_{in}:45V and I_{load}:10A).

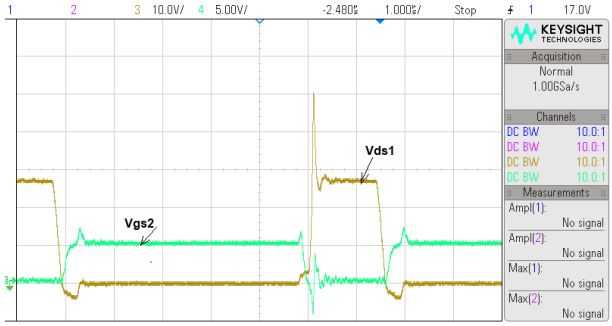


Figure 23. Synchronous switch voltage V_{ds2} and gating signal V_{gs2} (V_{in}:45V and I_{load}:10A).

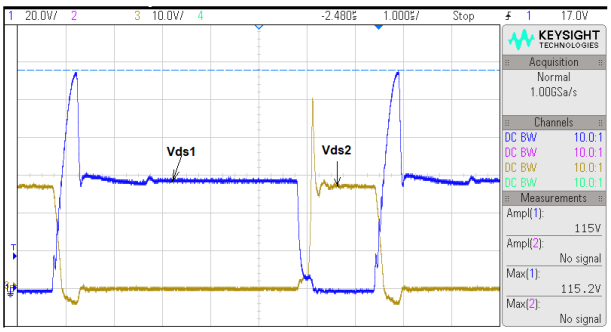


Figure 24. Switching voltage of main switch V_{ds1} and synchronous switch V_{ds2} (V_{in}:45V and I_{load}:10A).

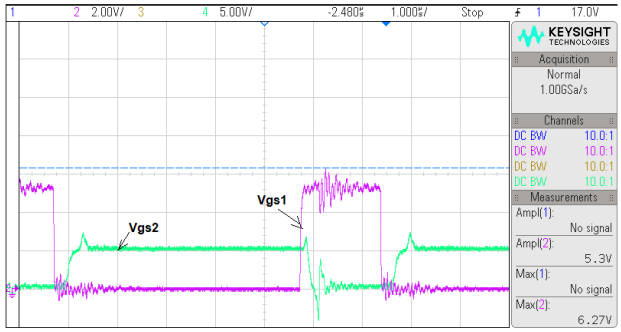


Figure25. Gating signal of main switch V_{gs1} and synchronous switch V_{gs2} (V_{in}:45V and I_{load}:10A).

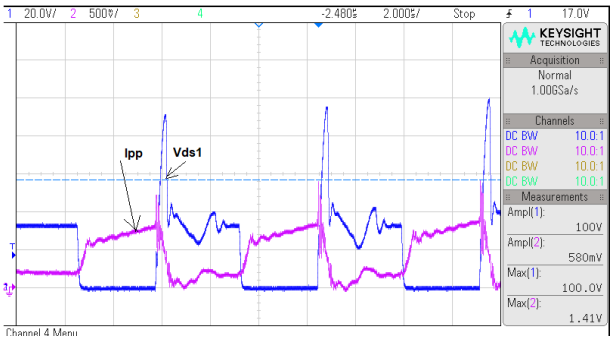


Figure 26. Measured main switch voltage (V_{ds1} and Primary peak current I_{pp} at (V_{in}:20V and I_{load}:10A).

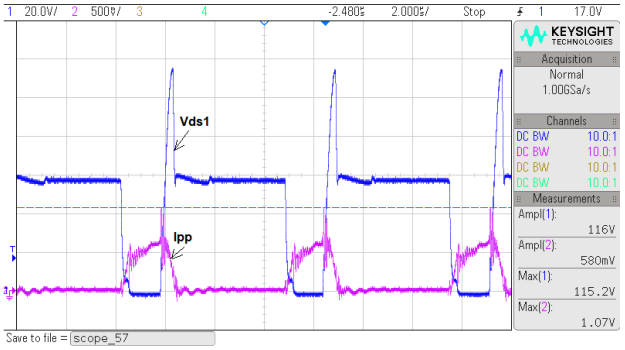


Figure 27. Measured main switch voltage and peak current (V_{ds1} and Primary peak current I_{pp} at (V_{in}:20V and I_{load}:10A).

Table 2. Line and Load Regulation

Input Voltage (Vin)	Input current at full load (Iin)	Output voltage at full load (Vo)	Line Regulation (%)	Load Regulation (%)
20.475	3.280	5.031	-0.020	-0.179
27.94	2.255	5.030		0.000
36.29	1.773	5.029		-0.358
45.158	1.432	5.040		-0.179

Table 3. Measured Efficiency at Full Load (10A)

Input Voltage (V_{in})	Input current at full load (I_{in})	Output voltage) at full load (V_o)	Input power (P_{in})	Output power (Po)	Efficiency (%)
20.475	3.280	5.031	67.16	50.290	74.898
27.94	2.255	5.030	63.93	50.290	79.810
36.29	1.773	5.029	64.34	50.290	78.160
45.158	1.432	5.030	65.66	50.290	77.768

Figure 26 and 27 shows the measured primary peak current (I_{pp}) and main switch voltage (V_{ds1}) with minimum and maximum input voltage at full load conditions respectively. Figure 28 and 29 shows the measured ripple waveform with minimum and maximum input voltage of 20V and 45V at full load condition, respectively. Table 2, 3 and 4 illustrates the line and load regulation, measured efficiency, and measured peak to peak ripple voltage with the variation of input voltage and load condition respectively. It is noted that the obtained experimental results had similar performance obtained in simulation results with various value of input voltage and load conditions.

Table 4. Peak-Peak Ripple Voltage

Input Voltage (V_{in})	Measured ripple voltage (peak-peak) at full load (mV)
20	103
28	72
36	67
45	64

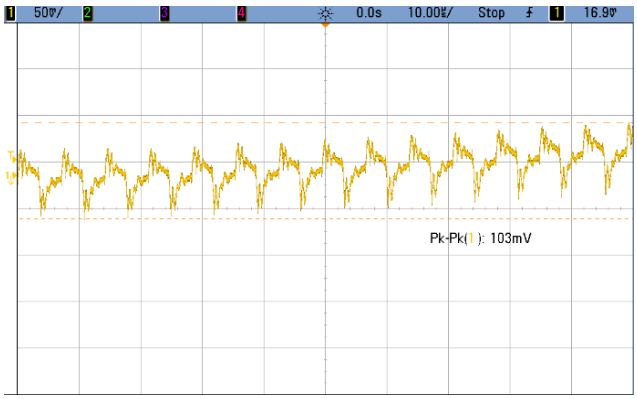


Figure.28 Measured ripple voltage at Vin: 20V and full load

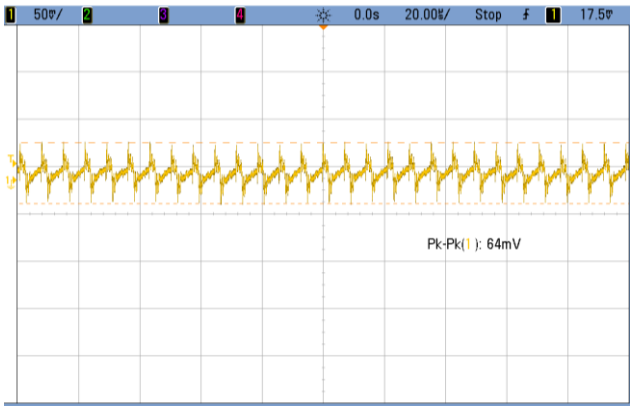


Figure.29 Measured ripple voltage at V_{in}: 45V and full load.

7. CONCLUSIONS

A fixed-frequency PWM-based current mode synchronous rectifier flyback converter for satellite EPS mission is presented from a circuit design perspective. Subsequently, the designed nonlinear controller based MPPT dc-dc converter has been used to input the interfacing flyback dc-dc converter. The synchronous rectifier-based flyback converter is a cost-effective solution for low output power application in EPS. The steady-state operation and the converter design methodology is described in detail. A practical approach to the design of the self-synchronous secondary driver circuit is also proposed in this paper. An analog form of the PWM controller is presented. The tuned controller used for voltage regulation is type-3 PID compensator to satisfy the sufficient magnitude and phase margin. The experimental results show that the response of the converter agrees with the theoretical and simulation design. The developed converter in a prototype model can be extended for space grade electric power systems in future. The efficiency of the converter can be improved further by tuning the snubber network and feedforward control technique. The goal of the design is to implement an optimized EPS can be realized such that the efficiencies of the distributed flyback dc-dc converter design are not significantly varied.

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