

Design Analysis and Experimentation of High step-up, High-efficiency Isolated SEPIC Converter

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Abstract— Due to energy crisis in the world the sources of renewable energy sources (RES) have to be enhanced. Out all RES, solar plays a main role. In photovoltaic (PV) power generation system, the dc to dc converter is unavoidable and which are prerequisite the high voltage gain conversion. Out of all converter topologies, SEPIC is a straight forward converter which can give high step continuous conduction operation. The SEPIC has a full degree of freedom to boost the voltage at 200%. Nevertheless high voltage gain is not possible, which is highly needed for PV based power electronics system. This high step voltage gain is possible only when transformer is converter circuit and through that the ratio of the inductance is increased and achieved maximum voltage gain. With this voltage gain improvement, the paper proposed a transformer connected modified SEPIC converter with high voltage gain degree of freedom. The proposed converter able to work for continuous current conduction mode since it is highly recommended for any converter to supply current to the load continuously and these converters are not affecting with switching frequency. The proposed converters different modes operation and it's design studies is clearly explained. The MATLAB based simulation studies for 1kW. The PIC microcontroller based 100W experimental test bench is developed and results are verified.

Keywords—DC to DC converter, SEPIC converter Continuous current mode operation.

I. INTRODUCTION

The attention in with RES has grown considerably in the last years. In 2017, PV was the foremost RES technology in the world. This because of high range of sun light availability [1]. Other main advantages of these PV systems are the modularity, allows the easy enlarge of the installed power. Hence, the world power installation PV is significantly increasing year on year with 5 to 7% in margin. In India alone installed 7.83GW capacity in 2016 and 2017 in a row [2]. In any PV system, the DC to DC conversion (converter) and DC to AC conversion (inverter)

essential and this is achieved either in single stage two stage conversion. Though the single stage conversion is reduces the power switches by avoiding the DC to DC conversion stage, the Z source inverters suffered with stability which is the major issue to attain the reliability on PV system [3]. Hence, two stage power conversions are unavoidable to connect to grid or utility loads. Since PV panels out is DC supply. Normally, the output DC voltage from PV panels is in the range between of 30 to 80 V. Hence, high step-up DC-DC converters are extensively used with MMPT controller to match the grid inverter DC –link requirement [a]. This DC-link balancing is attempted by using various control algorithms [4]. Through the DC-link betterment is satisfied through the different control methods, the converters fail to attain the required DC link voltage to the inverters. The other side high gain converter is necessary to enhance the low voltage to a high voltage, about 60 V to 380V to suit the DC-link voltage requirement of full bridge inverter [5]. Hence, the researchers giving important to develop the high step-up DC-DC converters with high boost factor and gain [6-8]. In addition, lightweight, compact, and high efficient converters are paying the high attendance for both reasonably priced and have acceptable cycle life. Besides PV power generation systems applications, such as UPS, multi-voltage-bus for DC micro grid, and electrical vehicles etc. [9]. The conventional approach to converting power from multiple sources is to connect two or more dc voltage sources to independent dc-dc power converters to produce a stable output voltage for the load with an appropriate control arrangement [10]–[12]. The use of high static gain and low-switch voltage topologies can improve the efficiency operating with low input voltage, as presented in [13]–[16]. The voltage multiplier technique was presented in [16] for a boost converter in order to increase the static gain with reduced switch voltage.

Hence, based on the aforementioned discussion the transformer connected modified SEPIC converter with high voltage gain degree of freedom. The proposed converter able to work for continuous current conduction mode since it is highly recommended for any converter to supply current to the load continuously and these converters are not affecting with switching frequency. The proposed converters different modes operation and it's design studies is clearly explained. The MATLAB based simulation studies for 1kW. The PIC microcontroller based 100W

Experimental test bench is developed and results are verified. The converter is very suitable for PV system application and can operate with wide range of voltage gain.

II. SEPIC CONVERTER OVERVIEW

The development of high static gain DC-DC converters is an important research area due to the crescent demand of this technology for several applications supplied by low DC output voltage power sources. Some examples are renewable energy sources as low power wind turbine, photovoltaic (PV) modules and other applications as fuel-cells, embedded systems, portable electronic equipment, uninterruptable power supply and battery powered equipment. Fig.1 shows the Circuit diagram of SEPIC Converter.

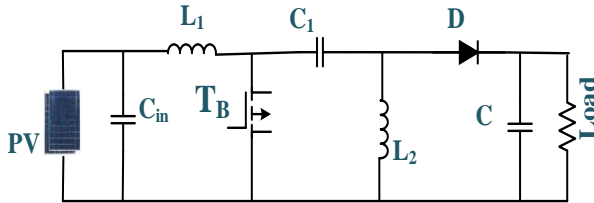


Fig. 1 Circuit diagram of SEPIC Converter

The power transformer also presents an important contribution in the converter weight and volume. The power converters used with renewable energy sources must present a high efficiency due to the high cost of the energy source, as photovoltaic module or fuel-cells. Also in embedded systems and portable equipment, the converter power density is an important design parameter. Therefore, the solutions that allow the elimination of the power transformer can improve the efficiency and power density of the power conversion system. However, due to the configuration of the power circuit proposed, the usual problems presented by the single switch isolated DC-DC converter are not presented by the proposed structure with transformer. Only part of the power processed by the converter is transferred to the output through the coupling inductor and another part of the power is transferred directly by the non-isolated converter, reducing the weight, volume and losses of the transformer. The leakage inductance is a problem for the single switch isolated DC-DC converters resulting in switch overvoltage and the energy stored in the leakage inductance must be dissipated in or clamping circuits. However, the leakage inductance is necessary in the proposed converter with transformer in order to obtain ZCS turn-on commutation and to reduce the diodes reverse recovery current, increasing the converter efficiency. The energy stored in the leakage inductance is transferred to the converter output through the diodes and capacitor of the circuit. The voltages in all semiconductors are clamped by the intrinsic converter operation without dissipative components.

III. MODIFIED SEPIC CONVERTER

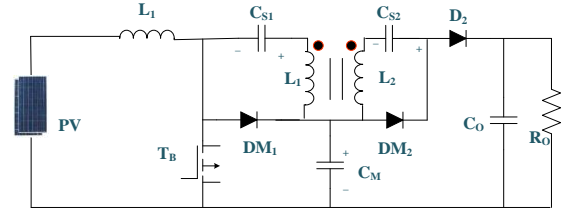


Fig. 2 Circuit diagram of proposed SEPIC Converter

The modified single-ended primary-inductor converter (SEPIC) shown in the Fig.2 is a type of DC/DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC is essentially a boost converter followed by a buck-boost converter, therefore it is similar to a traditional buck-boost converter, but has advantages of having non-inverted output (the output has the same voltage polarity as the input), using a series capacitor to couple energy from the input to the output (and thus can respond more gracefully to a short-circuit output), and being capable of true shutdown: when the switch is turned off, its output drops to 0 V, following a fairly hefty transient dump of charge. Fig. 3 to Fig 7 showing the different mode of operation of proposed SEPIC converter

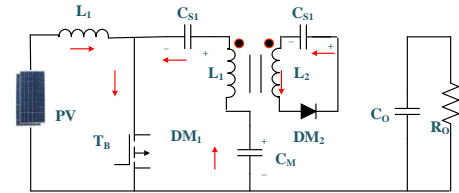


Fig. 3 Proposed SEPIC Converter operation during Mode-1

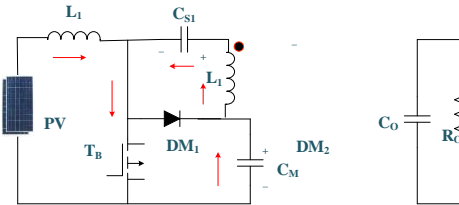


Fig.4 Proposed SEPIC Converter operation during Mode-2

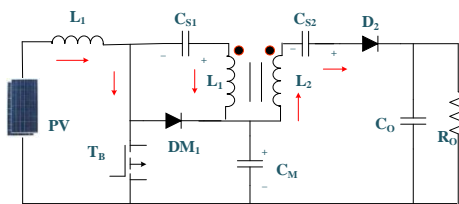


Fig.5 Proposed SEPIC Converter operation during Mode-3

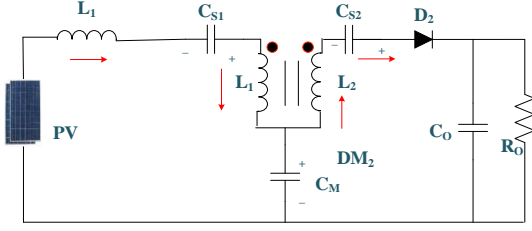


Fig.6 Proposed SEPIC Converter operation during Mode-4

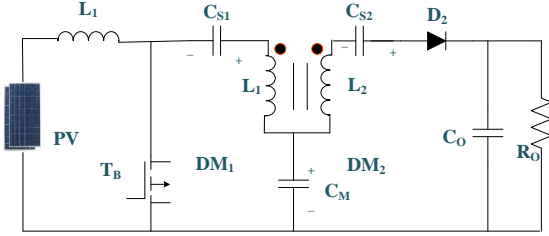


Fig.7 Proposed SEPIC Converter operation during Mode-5

Mode-1 [t₀–t₁]: The switch T_B is conducting as well as the inductor, L₁ stores input energy. The capacitor, C_{S2} is charged through the secondary winding, L₂ and diode D₂. The leakage inductance, L_L restrict the current along with the energy transfer occurs in a resonant mode. In this time, the output diode, D₂ is blocked; with the maximum diode voltage is equal to (V_o–V_{in}). During the instant at t₁, the energy transfer to the capacitor C_{S2} is finished as well as the diode, D_{M2} is blocked-up the conduction.

Mode-2 [t₁–t₂]: During mode-2, From the t₁ to t₂, when the diode, D_{M2} is blocked-up the conduction, to the instant t₂ while the switch T_B is turned OFF, the inductors (L₁ and L₂) accumulate energy and the currents of the inductors increase linearly.

Mode-3 [t₂–t₃]: After mode 2. At t₂, the both the inductor are fully charged. Hence, at the instant t₂ the switch T_B is turned OFF. The input energy a store in the inductor, L₁ inductor and it is transferred to parallel connected the C_M capacitor. In addition, during that instant the energy transfer to the output load through the capacitors C_{S1}, and C_{S2} inductor, L₂ and output diode, D_o.

Mode-4 [t₃–t₄]: During the instant t₃, the energy transferred to the C_M is completed and the diode, D_{M1} is reversed biased Hence, the energy transferred to the output is retained until the time t₄ (end of mode-4), at what time the switch T_B is ON.

Mode-5 [t₄–t₅]: When the switch, T_B is turned ON. During the instant t₄, the current at the output diode, D_o linearly reduced as well as the circuit di/dt is restricted through the leakage inductance of the transformer. Hence, diode reverse recovery current started reduce. While the diode D₂ is

blocked, the converter precedes with mode -1 operation again. The ideal characterises of the proposed SEPIC converter is shown in figure 8 with model 1 to mode 5 operation.

The static gain of the modified proposed SEPIC converter with is calculated by Eq. (1). It is calculated based on magnetic coupling as well as voltage multiplier

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \{1 + n\} \quad (1)$$

Here, when n is transformer windings turns ratio as,

$$n = \frac{L_2}{L_1} \quad (2)$$

The converter static gain could be increased through the transformer windings turns ratio not including rising the switch voltage. The ideal voltage gain characterises of the proposed SEPIC converter is shown in Fig.9.

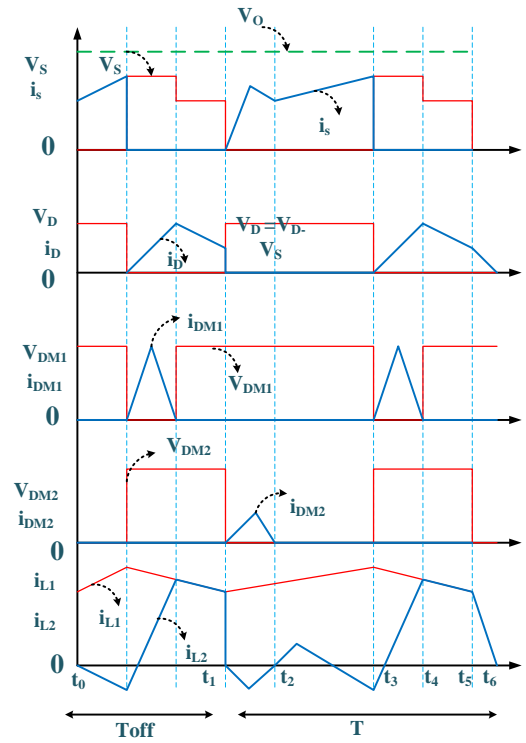


Fig.8 ideal characterises of the proposed SEPIC converter

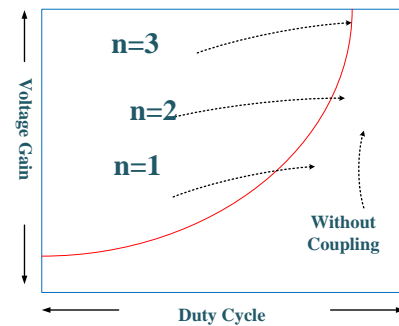


Fig.9 ideal voltage gain characterises of the proposed SEPIC converter

IV. SIMULATION STUDY

The proposed modified SEPIC converter is designed and modelled in MATLAB–Simulink simulation software and the designed and simulation parameter is described in the table-1. The power circuit with the component's parameters and a representation of the simplified MATLAB–Simulink presented in Fig. 17.

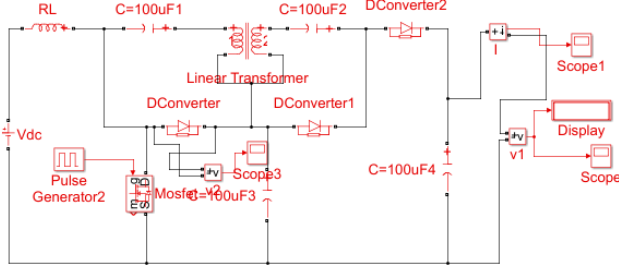


Fig.11 Simulation model of proposed SEPIC converter
The main equations to design the modified SEPIC converter with transformer magnetic coupling in view of the following specifications: Output power, $P_o = 1000\text{ W}$; Input voltage, $V_i = 44$, Output voltage, $V_o = 440\text{ V}$; Switching frequency, $f_s = 30\text{ kHz}$.

In the view of a static gain equal to 10 as well as an L_1 and L_2 winding turns ratio $n = 1.2$, the converter duty cycle, D is obtained using Eq. (1) is equal to

$$D = 1 - \frac{V_o}{V_{in}} \{1 + n\} = 1 - \frac{44}{440} \cdot (1 + 1.2) = 0.78 \quad (3)$$

The switching voltage MOSFET and Diode is calculated using the following Eq,

$$V_s = V_{DM1} = \frac{V_i}{1-D} V_{io} = 44 \cdot (1-0.78) = 85.6\text{V} \quad (4)$$

Doide, D_2 voltage is calculated as

$$V_o = V_D = \frac{V_i}{1-D} = 370\text{V} \quad (5)$$

The inductors L_1 and L_2 Inductance is calculated from inductor current ripple (Δi_L) is

$$L_1 = L_2 = 102\text{ MicroH.}$$

The leakage Inductance, L_l is calculated using following eq.

$$L_l = \frac{V_i}{1-D \left(\frac{di}{dt} \right) n} = 1.67\text{ MicroH.} \quad (6)$$

The capacitor C_1 and C_m is calculated by below eqs.

$$C_M = \frac{I_o \cdot n}{\Delta V_{C,f}} = 45\text{ MicroF} \quad (7)$$

$$\Delta V_C = \frac{V_i}{1-D} \cdot 100\% = 12.7\% \quad (8)$$

The simulation results are verified with different values for all duty cycle with different transformer ratio. The results is shown the $V_i = 44\text{V}$ and $V_o = 420\text{V}$ for full duty cycle $D=0.76$. The fig 13 , shows the input and output voltage waveform of the proposed converter when the duty cycle is use as $D=0.78$. From the results is could see that, the converter increasing the voltage again about 10time. The fig.14 shows the current profile of the input and output side, since the voltage is increased the output current is reduced from 22A to 4.4A. While increasing converters transformer ratio this boosting factor is increased further. However due to the magnetic saturation affect, practically

getting higher voltage gain through transformer ratio is difficult after some extent. The simulation results are obtained is detailed in table.-2 The static gain of the proposed converter can be obtained considering null the average inductors voltage at the steady state and it is presented considering the CCM operation. The static gain of the proposed converter is higher than the obtained with the classical boost. The CM capacitor voltage is calculated and that is the same output voltage of the classical boost converter. The maximum switch voltage is equal to the VCM voltage. Therefore, the switch voltage will be lower than the converter output voltage.

Table-1 Proposed Converter Circuit Parameters for simulation

Circuit Parameters	Range/Value
Input voltage, V_{in}	44V
Output voltage, V_o	420V
Out power, P_o	1000W
Switching Frequency, F_s	30kHz
Duty Cycle, D	0.76
Switch Voltage	160
Static Gran , G_s	10

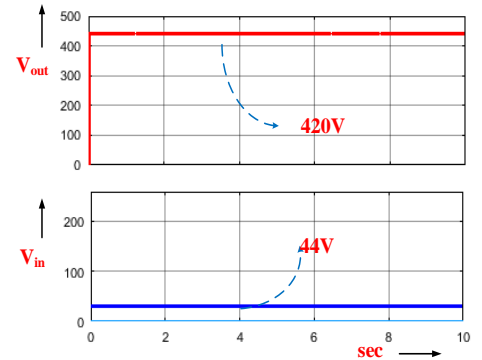


Fig. 12. Simulation results: Input voltage (V_{in}), output voltage (V_{op}) (100 V/div, 100 V/div, 2 sec/div).

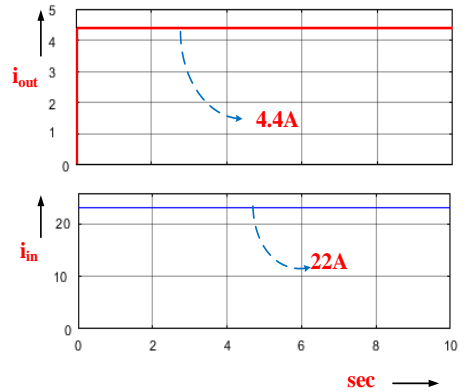


Fig. 13. Simulation results: Input current (I_{in}), output current (I_{op}) (10A/div, 1A/div, 2 sec/div).

Table-2 converter performance for the different input voltage with fixed duty cycle, $D=0.78$

Input voltage	Output voltage
10	100
20	198
30	298
40	397
44	440

V. EXPERIMENTAL STUDY

The proposed modified SEPIC converter is designed and implemented using PIC microcontroller. PIC 8-bit microcontroller is best chose for the small power converters and inverters design since it has a simple implementation and low cost [17]. Through the simulation study is considered for 1KW, 44V input voltage and, 440V output voltage, the proposed hardware validation has done for 100W. The IRF542-MOSFET used with IR driver circuits. The Fig.14 shows the input current of the converter , form the results it could seen that, the converter able to supply continues current.

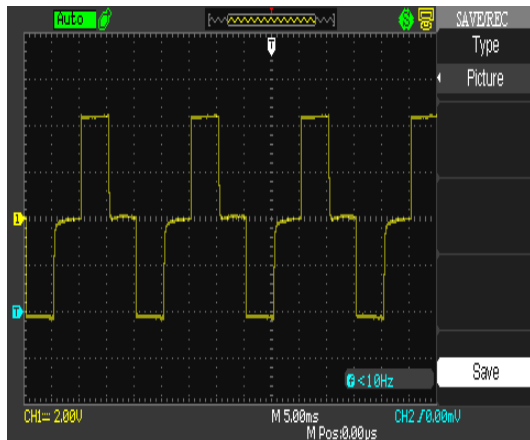


Fig. 14. Experimental results: Input current (I_{in}) (10 V/div, 2 msec/div)

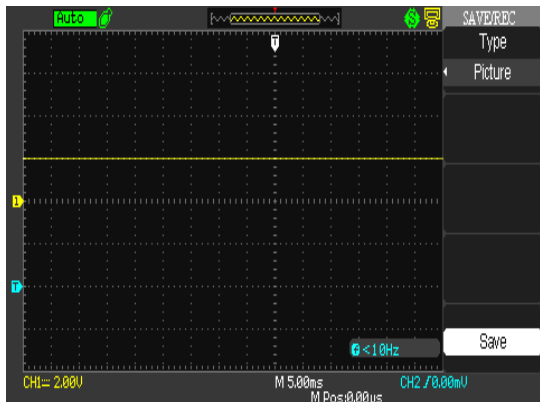


Fig. 15. Experimental results: Input volatge (V_{in}) (5 V/div, 2 msec/div).

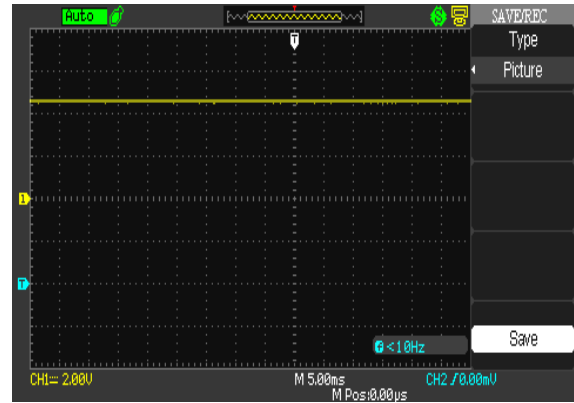


Fig. 16 Experimental results: output volatge (V_o) (20 V/div, 2 msec/div).

The Fig.15 show the input voltage of the converter. Here the converter input voltage is fixed with input rectifier as 4.4V, 15A. At this same instant, the scope results are measured with output terminal as shown in Fig.16. Now, the voltage in the outside is observed as 40V with 1.2 A. Based on the excremental results similar to simulation study performance, the proposed converters able to maintain 10 time voltage boosting with continuous current mode operations. Based on the analytical discussion and simulation and hardware study, the proposed SEPIC converter is highly recommended for PV applications and Electrical vehicles application for battery charging.

VI. CONCLUSION

In this paper proposed a high step voltage gain transformer connected modified SEPIC converter. The converter is has a continuous current conduction with high voltage gain nearly, 10 time. The proposed converter able to work for continuous current conduction mode in all modes, since it is highly recommended for any DC to DC converter. The converter switching and conduction losses are less than 1%, which is give a high efficiency. The proposed converters different modes operation and it's deign studies is clearly explained. The MATLAB based simulation studies for 1kW. The PIC microcontroller based 100W experimental test bench is developed and results are verified.

REFERENCES

- [1] H. J. Chiu, C. J. Yao, and Y. K. Lo, "A DC-DC converter topology for renewable energy systems," Int. J. Circuit Theory Appl., vol. 37, no. 3, pp. 485–495, Jul. 2009.
- [2] Indian Energy senior, MHRD, 2017 report.
- [3] T.K.S Sathayanarayanan, M Ramasamy, C Bharatiraja, JL Munda "Modelling, Impedance Design, and Efficiency Analysis of Battery Assists PV tied Quasi-Z source inverter", in International Journal of Power Electronics and Drive Systems, vol.3, no.7, pp. 816-825, Dec 2016
- [4] C.Bharatiraja, S.Jeevananthan., Latha, R., "FPGA based practical implementation of NPC-MLI with

- SVPWM for an autonomous operation PV system with capacitor balancing”, in *International Journal of Electrical Power and Energy Systems/ Elsevier*, vol. 61, pp.489-509, Oct 2014
- [5] C. Bharatiraja, S. Jeevananthan, and J. L. Munda, “A Timing Correction Algorithm-Based Extended SVM for Three-Level Neutral-Point-Clamped MLI in Over Modulation Zone,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 233–245, Mar. 2018
 - [6] Q. Zhao and F. C. Lee, “High-efficiency, high step-up DC–DC converters,” *IEEE Transaction on Power Electronics*, vol. 18, no. 1, pp. 65–73, Jan. 2003.
 - [7] R.-J. Wai and R.-Y. Duan, “High step-up converter with coupled-inductor,” *IEEE Transaction on Power Electronics*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.
 - [8] G. Henn, R. Silva, P. Praça, L. Barreto D. Oliveira, “Interleaved Boost Converter with High Voltage Gain”, *IEEE Transaction on Power Electronics*, vol. 25, no. 11, pp. 2753–2761, Nov. 2010.
 - [9] C. Bharatiraja, Aishwarya Ravi, Sanchari Banerjee, Abhishek Chakraborty, “A Hybrid Cascaded Multilevel Inverter with Diode Assisted Boosting Network”, *Energy Procedia/ Elsevier*, Vol. 117, 2017, pp. 1024–1031, June 2017
 - [10] Y. M. Chen, Y. C. Liu, and S. H. Lin, “Double-input PWM DC-DC converter for high/low voltage sources,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1538–1544, Oct. 2006.
 - [11] H. Wu, K. Sun, S. Ding, and Y. Xing, “Topology derivation of nonisolated three-port DC-DC converters from DIC and DOC,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3297–3307, Jul. 2013.
 - [12] F. Liu, Z. Wang, Y. Mao, and X. Ruan, “Asymmetrical half-bridge double-input DC-DC converters adopting pulsating voltage source cells for low power applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4741–4751, Sep. 2014.
 - [13] C. Bharatiraja, S. Jeevananthan, S. R. Latha, and V. Mohan, “Vector selection approach-based hexagonal hysteresis space vector current controller for a three phase diode clamped MLI with capacitor voltage balancing,” *IET Power Electronics*, vol. 9, no. 7, pp. 1350–1361, June 2016.
 - [14] R.-J. Wai and R.-Y. Duan, “High step-up converter with coupled-inductor,” *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.
 - [15] R.-J. Wai and R.-Y. Duan, “High-efficiency power conversion for low power fuel cell generation system,” *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 847–856, Jul. 2005.
 - [16] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. R. Romanelli, and R. Gules, “Voltage multiplier cells applied to non-isolated DC–DC converters,” *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.
 - [17] C. Bharatiraja, Mohammad Shabin, “A Novel reduced switch single source MLI topology with variable input overvoltage control”, in *Procedia Engineering/Elsevier*, vol. 64, pp. 205–214, 2013.
 - [18] C. Bharatiraja and J. L. Munda, “Simplified SVPWM for Z Source T-NPC-MLI including neutral point balancing,” 2016 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE), Penang, Malaysia, 30–31 May
 - [19] Santhakumar, C., Shivakumar, R., Bharatiraja, C., Sanjeevikumar, P. “Carrier shifting algorithms for the mitigation of circulating current in diode clamped MLI fed induction motor drive”, in *International Journal of Power Electronics and Drive Systems*, vol. 8, no. 2, pp. 844–852, June 2017
 - [20] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg and G. Town, “Y-Source Impedance Network,” in *Proc. APEC 2014*, Fort Worth, TX, pp. 3362–3366, Mar. 2014
 - [21] C. Bharatiraja, S. Raghu, Anathraj, Prabathkumar “Analysis and simulation of magnetically coupled Y shape impedance source inverter”, *Indian Journal of Science and Technology*, Volume 9, Issue 44, pp. 1–7, 2016.
 - [22] A. Bindu, M. Carolin Mabel, and C. Bharatiraja, “A Real-Time Energy Management Approach And Its Power Converter For PV Powered Plug-In Electric Vehicle”, in *Journal of Electrical Engineering*. vol. 17, no. 2, 2017, pp. 241–247, 2017.
 - [23] C. Bharatiraja, R. Latha, “A New Asymmetrical Single Phase 15 Level Reduced Switch Multilevel Voltage Source Inverter”, in *Journal of Electrical Engineering*. vol. 15, no. 4, pp. 1–9, Dec 2015.
 - [24] P. Ramesh .C. Sharmeeela, and C. Bharatiraja, “Nine Level MLI fed Single Phase Induction Motor Drive with Compressor Load Using Artificial Neural Network”, in *Journal of Electrical Engineering*, Vol. 17, No. 2, 2017, pp. 242–247, 2017