A Proto Type FPGA Based Reduced Switch Three Phase Inverter Fed Induction Motor Drive

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Abstract- A proto type implementation of FPGA based four switch three phase inverter (FSTPI) fed Induction Motor drive is presented in this paper. In this proposed approach both simulation and experimental work are demonstrated. The simulation of the system is carried out using MATLAB SIMULINK and experimental work is carried out using Spartan-3 processor and Xilinx software. In the experimental work, the in Xilinx software is used to generate the PWM pulses for FSTPI to drive the 0.5 hp 3-phase Induction Motor. The proposed FSTPI fed IM drive is found acceptable considering its cost reduction and other advantageous features.

Index terms- FSTPI- Four Switch Three Phase Inverter, FPGA-Field Programmable Gate Array IM-Induction Motor, PWM-Pulse Width Modulation.

I. INTRODUCTION

The 3-phase Induction motor is a rotating electric machine designed to operate from 3-phase alternating voltage source. Over the years Induction Motor (IM) has been utilized as a workhorse in the industry due to its easy build, high robustness, and generally satisfactory efficiency. AC induction motors, which contain a cage, are very popular in variable-speed drives. They are medium construction complexity, multiple fields in stator, cage on rotor, high reliability(no brush wear), medium efficiency at low speeds, high efficiency at high speed, low cost per horse power and easy to reverse the motor.

A standard three-phase voltage source inverter utilizes three legs [six-switch three-phase voltage source inverter (SSTPI)], with a pair of complementary power switches per phase. A reduced switch count voltage source inverter [four switch three-phase voltage source inverter (FSTPI)] uses only two legs, with four switches. Several articles report on FSTPI structure [1]–[6]. A Field-Programmable Gate Array (FPGA) is a type of logic chip that can be programmed. An FPGA is similar to a PLD, but whereas PLDs are generally limited to hundreds of gates, FPGA supports thousands of gates. They are especially popular for prototyping integrated circuit designs. Once the design is set, hardwired chips are produced for faster performance. The inherent parallelism of the logic resources on an FPGA

allows for considerable computational through put even at a low MHz clock rates. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. This has driven a new type of processing called reconfigurable computing, where time intensive tasks are offloaded from software to FPGA [7].

Another important advantage of VHDL is that it is technology independent. The same algorithm can be synthesized into any FPGA and even has a direct path to an ASIC, opening interesting possibility in industrial applications in terms of performance and cost. However, the major disadvantage of an FPGA-based system for hardware implementation is the limited capacity of available cells. The FPGA-based applications of various motor drives can be found in [8]–[10].

In this work, XILINX FPGA (Field Programmable Gate Array) is used to generate PWM pulses for FSTPI and the motor is fed from a four switch three phase PWM inverter instead of a conventional six switch three phase inverter. VHDL (Very high speed IC description language) program is developed and simulated in XILINX software and implemented on a SPARTAN Processor. Simulation and experimental results illustrate the use of the FSTPI to supply a three-phase induction motor.

II. PROPOSED TOPOLOGY

The block diagram of proposed FPGA based FSTPI fed IM drive is shown in Fig-1. The rectifier converts AC to DC. The FSTPI is used to convert DC to 3-phase AC. The Inverter output is three phase AC voltage which is fed to the induction motor. The FPGA software is used to

generate PWM pulse to drive the FSTPI. The FPGA output pulses are fed to the driver circuit. The PWM pulses from the driver circuit are fed to the FSTPI to drive the Induction Motor.
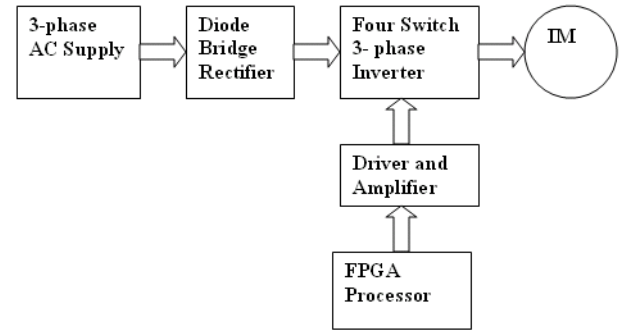

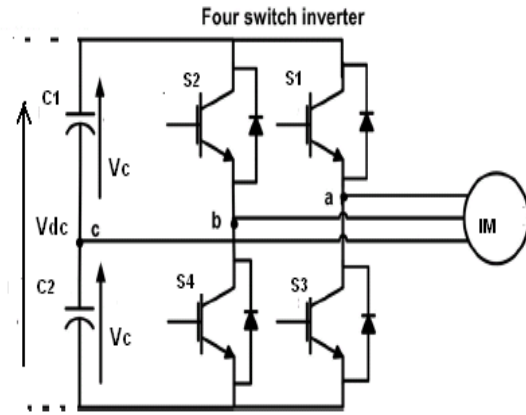Fig-1 Block Diagram of FPGA based FSTPI.

Fig.2 FSTPI with Induction Motor.

III. PRINCIPLE OF OPERATION OF FSTPI

The power circuit of the FSTPI fed drive is shown in Fig. 2. The power inverter has 4 switches, S1, S2, S3 and S4 and a split capacitor. The switches are controlled in order to generate an AC output from the DC input. The two phases 'a' and 'b' are connected through two legs of the inverter, while the third phase 'c' is connected to the center point of the dc link capacitors, C1 and C2. The capacitance value of C1 and C2 are equal.

It is assumed that the 4-power switches are denoted by the binary variables S_1 to S_4. The binary '1' corresponds to an ON state and the binary '0' corresponds to an OFF state. The states of the upper (S_1, S_2) and lower (S_3, S_4) switches of a leg are complementary that is $S_3 = 1-S_1$ and $S_4 = 1-S_2$. Considering a 3-phase Y-connected Induction Motor, the terminal voltages V_{as}, V_{bs} and V_{cs} can be expressed as the function of the states of the upper switches as follows:

$$V_{as} = \frac{V_c}{3}(4S_1 - 2S_2 - 1) \qquad (1)$$

$$V_{bs} = \frac{V_c}{3}(-2S_1 + 4S_2 - 1) \qquad (2)$$

$$V_{cs} = \frac{V_c}{3}(-2S_1 - 2S_2 + 2) \qquad (3)$$

Where V_{as}, V_{bs}, V_{cs} are the inverter output phase voltages. 'V_c' is the voltage across the dc link capacitors. 'V_{dc}' is the voltage across the capacitor C1 and C2 ($V_{dc} = V_c/2$). S_1, S_2 are taken as the switching functions for the 2-switches. In matrix form the above equations can be written as:

$$\begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \frac{V_c}{3}\begin{pmatrix} 4 & -2 \\ -2 & 4 \\ -2 & -2 \end{pmatrix}\begin{bmatrix} S_1 \\ S_2 \end{bmatrix} + \frac{V_c}{3}\begin{bmatrix} -1 \\ -1 \\ 2 \end{bmatrix} \qquad (4)$$

Table 1 shows the different modes of operation and the corresponding output phase voltage vector of the FSTPI.

Table 1: Switching states and output Phase voltages of FSTPI.

Switching states		Output voltage		
S_1	S_2	V_{as}	V_{bs}	V_{cs}
0	0	$-\dfrac{V_c}{3}$	$-\dfrac{V_c}{3}$	$\dfrac{2V_c}{3}$
0	1	$-V_c$	V_c	0
1	0	V_c	$-V_c$	0
1	1	$\dfrac{V_c}{3}$	$\dfrac{V_c}{3}$	$-\dfrac{2V_c}{3}$

IV. SIMULATION RESULTS

Digital computer simulation model has been developed to test the proposed FSTPI fed IM drive by using MATLAB SIMULINK. The simulations were performed for a FSTPI supplying at different load conditions. The drive system consists of a three-phase diode bridge rectifier, a split capacitors, Four switch three phase inverter, 3-phase squirrel cage Induction Motor.
• Input three-phase supply voltage = 400 V (rms), 50 Hz;
• Three-phase induction motor: 3 hp 400 V, 50 Hz, 1500 rpm.

The simulation is carried out by using MATLAB SIMULINK. Fig-3 shows the complete simulation circuit diagram of the system. The 3-phase output currents of FSTPI i_a, i_b and i_c are shown in fig-4. The speed and torque curve of Induction motor is shown in Fig-5, with load condition. The Speed increases linearly and reaches at rated speed (1500 rpm) in steady state at 0.75 sec. At starting the torque increases and reduces at minimum value when the speed reaches at rated value.
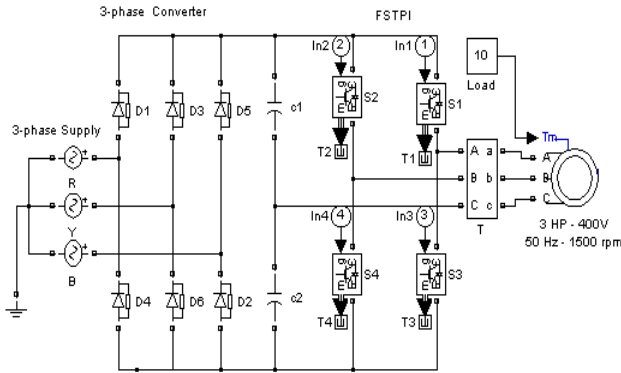

Fig 3, The complete Simulation Circuit diagram of FSTPI fed IM Drive system.
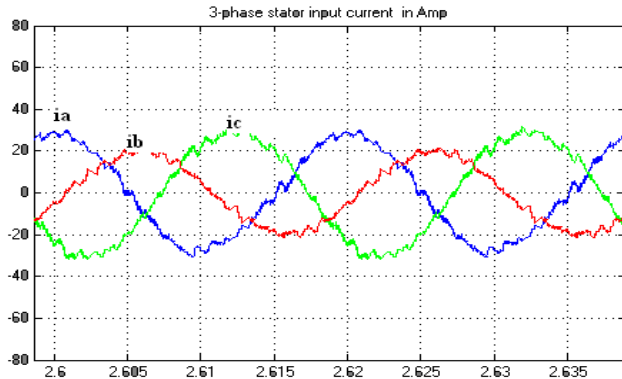

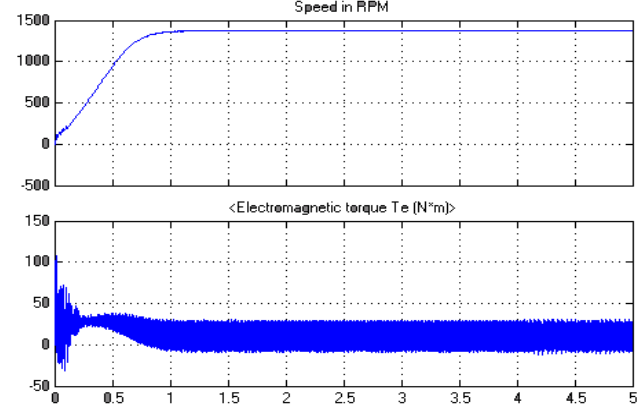Fig. 4 The stator currents i_a, i_b and i_c.

Fig-5, Rotor speed in rpm vs time in sec and Electromagnetic torque in N-m vs time in sec. with Load 10 N-m.

V. EXPERIMENTAL RESULTS

The experimental tests were performed by using a setup based on a SPARTAN processor equipped with appropriate plug-in boards for power switch control. The multi meter and digital oscilloscope is used to measure the output current and voltage of FSTPI. A complete hardware setup is described in the table-2.

Table 2. Hardware Component Details

Components	Ratings
Capacitor	1000μf, 250V
Inverter	MOSFET(IRF 460) switch
Induction Motor	0.5 hp ,3-phase, 50Hz,400v
Processor	SPARTAN-3,model XC3S200
Rectifier	110v,5A Bridge Rectifier

The complete set up (FPGA processor board, Driver Circuit, FSTPI, and 3-phase IM) is shown in Fig-6. The output pulses waveforms of switch S_1, S_2, S_3, and S_4 are obtained from the driver circuit are taken by the Digital Oscilloscope. The pulses of switch S1 are shown in Fig.7.

The output current waveform of phase-A is shown in Fig-8. It is found that the simulation and experimental results are almost similar. The simulation and experiment work of FSTPI fed Induction motor drive carried out successfully.
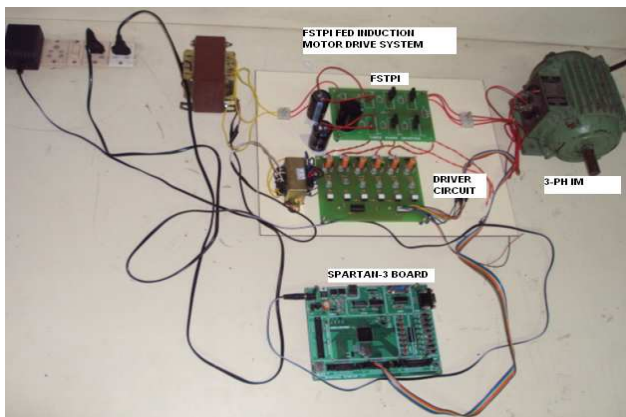

Fig-6, A complete hardware implementation of FPGA based FSTPI Drive.
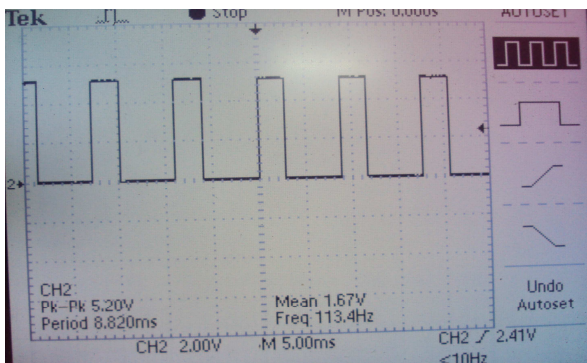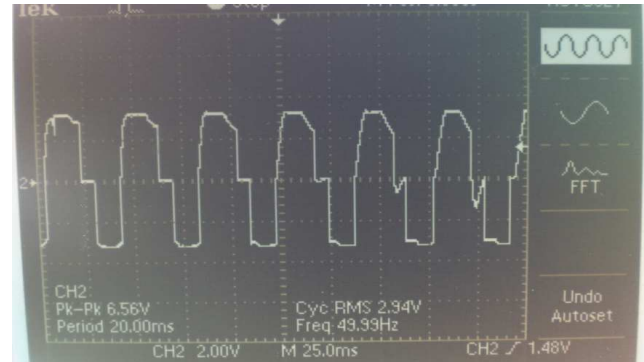

Fig. 7 Pulses of switches S_1

Fig.8, Output current of Phase-A.

VI. CONCLUSION

A proto type FPGA based implementation of FSTPI fed IM drive is carried out successfully. The results of both simulation and experimental work compared and found that almost similar. The software MATLAB SIMULINK is used as simulation work and the experimental work is carried out by using SPARTAN-3 processor. VHDL (Very high speed description language) program is developed and simulated in XILINX software to generate PWM pulses to drive the system.

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