ADAPTIVE CONTROL OF DSP BASED SHUNT ACTIVE POWER FILTER

Ahmed A. Elkousy **Sherif A. Zaid**
Faculty of Engineering, Cairo University, Cairo 12613
{aelkousy&sherifzaid3}@yahoo.com

Shokry M. Saad **Ashraf A. Hagras**
Atomic Energy Authority, AboZaabal, Cairo 13759
ashrafa1973@yahoo.com & shokryms@hotmail.com

Abstract: *In this paper, new adaptive current control technique was proposed for three phase shunt active power filter (SAPF) using Motorola DSP56F807. This control method based on sensing the reference supply current from the DC capacitor voltage and current control based on employing new version of the inverter model using the difference equations to generate the switching state functions for the inverter. This paper presents comparison between the current control employing the inverter model or constant gain of the reference filter current to show its effectiveness in eliminating the harmonics. The program of this method was elaborated by the assembly language of DSP56F807. The simple algorithm was able to reduce the cost of the system and complexity of the control circuitry. The proposed system was implemented and tested experimentally. The experimental results show the excellent performance of the proposed system and its adaptive capability to compensate parameters uncertainties, frequency variations and step load change.*

Key words: *Shunt Active Power Filter, Adaptive Control, Inverter Model, DSP56F807, Current Control.*

1. Introduction

Plofiration of power electronics equipments in the power system had given rise to current and voltage distortion in the local network. In addition, the local network has single phase loads, adjustable speed drives and immune to sever conditions like higher temperature degree of the power system components and deviation in supply frequency. These conditions motivate the research towards implementation of adaptive control of active filters. In the past, a majority of the controllers developed for active filters were focused on achieving the conventional objectives of active filter.

In the past, majority of the controllers are composed of analog circuits, so that the controller is costly, especially due to multiplication devices. The active filters are subject to signal drift inherent in analog circuits. Unlike analog control circuit, digital control has much outstanding advantages, such as reliability and flexibility. However, its performance is likely weakened by time delays and phase shift in the process of signal sampling, conditioning and computing. Elaborate design of digital system is needed to ensure satisfactory dynamic response of the shunt active power filter [1-3]. All these conditions ranging from the various conditions of the power network and the advantages of digital control led to DSP control of active filters.

Owing to economy, flexibility and reliable implementation, a digital controller using a DSP or a microcontroller is preferable to an analog controller. DSP implementation will allow real-time processing of the nonlinear load current to determine the harmonic content of the nonlinear load current using simple algorithm. The magnitude and phase information of the harmonics is passed to the PWM control algorithm of the filter for active cancellation of variable load-generated harmonics.

The SAPF consists of two main loops, DC voltage outer loop and inner current loop. In this paper, the DC voltage loop is regulated by PID controller. This outer loop was used to impose the sinusoidal reference supply current by multiplying the ideal three phase AC voltages e_a, e_b and e_c by the output of the PID controller. The current control employs new technique based on processing the reference filter currents through the model of the inverter to obtain the duty cycles of the three arms according to the inverter model equations. This method ensures the sinusoidal shaping of the source currents. The block diagram of the system is shown in fig. 1.

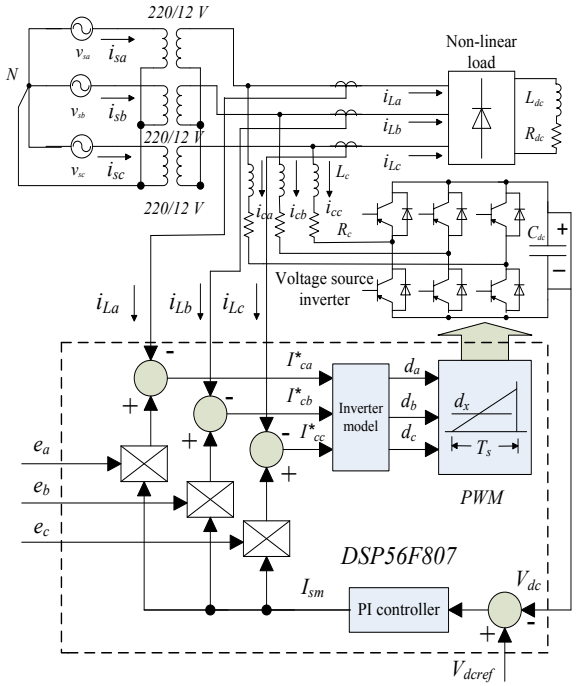

Fig. 1 Block Diagram of DSP 56F807 based SAPF

This paper presents DSP-based shunt active power filter with enhanced reactive power compensation. The current control is based on the least number of sensors. It employs four sensors for the three phase load currents and the DC voltage measurement. The current control loop is based on evaluating the switching functions and processing them using ramp comparison technique implemented inherently in DSP56F807 according to the model of the inverter. The digital control was implemented using the DSP56F807 EVM.

Most of the literature propose *p-q* or *d-q* frame for SAPF and apply the controllers through these frames on their axes. The type of controllers varies between PI, fuzzy, neural and other types of controllers. These methods require many transformations and filters and this represent a large computational ahead for DSP.

There are few papers in the literature which evaluate the switching state functions from the inverter model or the reference filter currents directly. These methods such as [4] don't depend on the model where it processes the reference filter current directly using sinusoidal pulse width modulation (SPWM). But in [5], although it evaluates the switching state functions from the inverter model using source currents and the output of PI controller of the DC voltage, this method is suitable only for high source currents to can measure it. In [6] it evaluates the switching state functions from the filter currents and the reference filter currents through the inverter model but it requires many transformations which need many calculations in the synchronous *d-q* frame.

This paper presents a less computational and concise implementation method for reference currents determination and current control using DSP56F807 in the stationary *a-b-c* frame. This method overcame the computational complexity of control system using DSP for SAPF by developing the difference equations for the inverter model and the PID controller. The difference equations were implemented by the assembly language as shown in the next section.

This paper is organized as follows: firstly the SAPF model in the *a-b-c* stationary frame and software set up of the system are developed in section 2. In section 3, shunt active power filter (SAPF) design details is presented. Section 4 presents the experimental results. Finally the conclusions are drawn in section 5.

2. Software Set up of the System

Figure 1 shows a standard six-switch three-phase shunt active power filter in parallel with nonlinear load. Under a balanced three phase ac supply and neglecting the resistance of the power switches. The dynamical model of the shunt APF under consideration in the stationary *a-b-c* frame may be expressed as in [7]:

$$L_c \frac{di_{ca}}{dt} = -R_c i_{ca} - V_{dc} d_{na} + v_{sa} \quad (1)$$

$$L_c \frac{di_{cb}}{dt} = -R_c i_{cb} - V_{dc} d_{nb} + v_{sb} \quad (2)$$

$$\frac{dv_{dc}}{dt} = (2d_{na} + d_{nb}) \frac{i_{ca}}{C_{dc}} + (d_{na} + 2d_{nb}) \frac{i_{cb}}{C_{dc}} \quad (3)$$

Where: i_{ca}, i_{cb} : The three phase inverter currents in the stationary *a-b-c* frame.

d_{na}, d_{nb}, d_{nc} : The three phase switching state functions in the stationary *a-b-c* reference frame.

w : The supply frequency.

v_{sa}, v_{sb} : The supply phase voltages in the stationary *a-b-c* reference frame.

R_c, L_c : The SAPF resistance and inductance.

V_{dc} : The capacitor DC voltage.

The reference supply currents I^*_{sn} are obtained by multiplying the output of the PID controller (DC voltage controller) I^*_{sm} by three ideal three phase voltages e_a, e_b and e_c. Then, the reference filter currents I^*_{cn} are obtained by subtracting the load currents I_{Ln}

from the reference supply currents I^*_{sn} as follows:

$I^*_{sn} = I_{sm} e_n$, e_n : is the ideal phase voltage.

$I^*_{cn} = I^*_{sn} - I_{Ln}$, *n (the phase number) =a , b* and *c.*

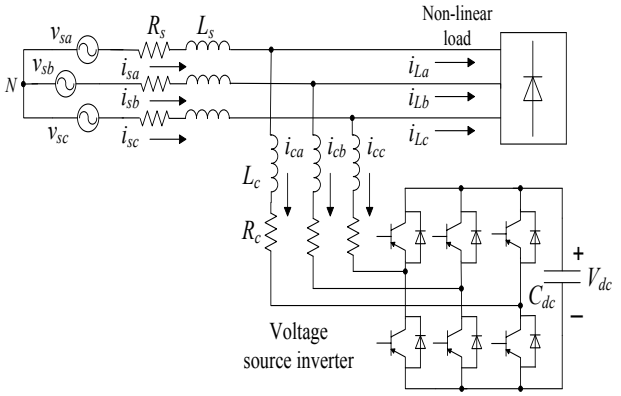

Fig. 2 SAPF with a voltage source inverter

Manipulation and substitutions of the SAPF model eqs. (1)-(3) and replacing the phase voltages by the ideal three phase voltages results the switching state equations (d_{na}, d_{nb} and d_{nc}) as described in [5-9].

$$d_a = \frac{1}{V_{dc}}\left[-L_c\frac{di_{ca}}{dt} - R_c i_{ca} + e_a\right] \quad (4)$$

$$d_b = \frac{1}{V_{dc}}\left[-L_c\frac{di_{cb}}{dt} - R_c i_{cb} + e_b\right] \quad (5)$$

$$d_c = \frac{1}{V_{dc}}\left[-L_c\frac{di_{cc}}{dt} - R_c i_{cc} + e_c\right] \quad (6)$$

The SAPF model was expressed in time domain and this permits transforming them into difference equations for the system model. Accordingly, these equations (4)-(6) can be implemented in the digital form using the assembly language for DSP56F807. Each equation can be represented by the difference equation as follows:

$$d_n(kT) = d_n((k-1)T) + \frac{1}{V_{dc}}\begin{bmatrix} -L_c I^*_{cn}((k-2)T) + (2L_c + R_c) I^*_{cn}((k-1)T) \\ -(R_c + L_c) I^*_{cn}(kT) + e_n(kT) \end{bmatrix} \quad (7)$$

Where: $d_n(kT)$ is the present switching state function for each phase, $d_n((k-1)T)$ is the previous switching state function for each phase, $I^*_{cn}(kT)$ is the present filter current for each phase $I^*_{cn}((k-1)T$ is the previous filter current for each phase, $I^*_{cn}((k-2)T$ is the filter current preceding the filter current $I^*_{cn}((k-1)T$, $f=1/T$ is the current control loop frequency iteration and *n=a, b or c*.

To achieve harmonics and reactive power compensation, the DC voltage loop can be controlled by the PID controller to achieve balancing of the operation of the active filter. The output of the PID controller is I_{sm} in fig. 2 which is the output of the difference equation of PID controller *u(kT)* can be expressed as [8]:

$$u(kT) = u((k-1)T) + k_0 E(kT) + k_1 E((k-1)T) + k_2 E((k-2)T) \quad (8)$$

Where: $k_0 = k_p + k_i T/2 + k_d / T$

$k_1 = -k_p + k_i T/2 - 2k_d / T$ and $k_2 = k_d / 2$

Where: *u(Kt)*is the output of the PID controller, *u(k-1)T)*is the previous output of the PID controller, *E(Kt)* is the present DC error voltage, *E((k-1)T)* is the previous DC error voltage, *E((k-2)T)*is the error preceding *E((k-1)T)* and k_p, k_i and k_d are the constant parameters of the PID controller and *F=1/T* is the sampling frequency of the controller which is the DC voltage control loop frequency iteration [8-9]. The detailed block diagram of the digital control system can be depicted as in fig. 3.

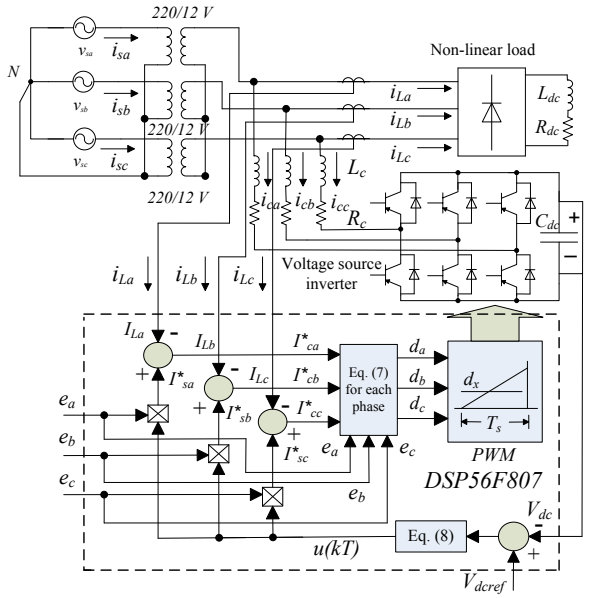

Fig. 3 The detailed block diagram of the proposed control system

3. Design of SAPF

In practice, the AF system should have energy storage and exchange capabilities to ensure energy balance between the filter and the supply [10-15].

A. Design rating of IGBT switches used in power circuit

The power rating of the SAPF circuit is based on the total harmonic distortion present in the load current. In general, the THD of a nonlinear *R-L* load varies in the range 20–50% for a load change from full load to light load conditions. The nonlinear load used in this paper has a THD of approximately 30% and this load is operated at 12V phase voltage. For a 0.1 kVA load operating with a 12VAC system, the IGBTs of the AF system are SKW30N60 rated at 30 A; this is to include an approximate tolerance factor in case of increasing the phase voltage for more DC load current. The tolerance allows the AF power circuit to withstand occurrence of overcurrent conditions.

B. Design of the filter resistance and inductor

The choice of the inductance value is dictated by (i) PCC voltage and (ii) the margin between the *di/dt* of the maximum harmonic component to be eliminated and the *di/dt* produced by the active filter.

The maximum *di/dt* of the compensating current has to be determined for each harmonic component based on its amplitude and frequency. The overall maximum *di/dt* for this current is therefore the highest individual *di/dt*. The harmonic giving the highest *di/dt* is generally the third for single phase rectifiers with capacitive loads, yet is the fifth for three phase rectifiers with inductive or capacitive loads.

$$i(t) = A\sin 2\pi ft \quad \text{then} \quad \max\left(\frac{di}{dt}\right) = A2\pi f t \qquad (9)$$

Considering the Kirchhoff´s Voltage Law, for one of the phases of the system (Fig. 2), it results:

$$-\sqrt{2}\sqrt{3}V_a - L_a\left(\frac{di}{dt}\right) + V_{dc} = 0$$

$$L_a = \frac{V_{dc} - \sqrt{2}\sqrt{3}V_a}{di/dt} \qquad (10)$$

From the standard inductor differential equation an expression for *di/dt* can be determined and is given by Eqn. (11) where $\Delta\mathbf{V}$ is the voltage across the inductor (assuming negligible resistance).

$$\left(\frac{di}{dt}\right) = \frac{\Delta V}{L} \qquad (11)$$

Such a compromise between the rate of change of filter current and the voltage drop across the inductor is important. This compromise is carried out by choosing suitable filter resistance to avoid the drop of the ac voltage of the nonlinear load.

C. Design of the DC bus capacitor

The DC bus capacitance of the AF system can be computed from following equation:

$$\Delta e_{dc} = \frac{1}{2}C_{dc}\left[\left(V^*_{dc}\right)^2 - \left(V_{dc}\right)^2\right]$$
$$= \frac{1}{2}C_{dc}\left(V^*_{dc} + V_{dc}\right)\left(V^*_{dc} - V_{dc}\right) \qquad (12)$$

Where Δe_{dc} is the energy exchange between the SAPF and the load in one interval sixth (T/6= 3.3333 ms) of the supply period and can be evaluated by multiplying the sixth of the interval cycle by load power (√3Va*Ia=64.4 watts).

$$\Delta e_{dc} = \sqrt{3}V_a I_L * (T/6)$$
$$= 64.4 * 3.3333 = 0.215J$$

In the DSP based control scheme of the AF system, on setting $V_{dc} > 2.0*V_{sm} = 33V$. V_{sm}: the peak supply voltage. For Δe_{dc} =0.215 J and for a proper current control of the AF system, V_{dc} is controlled to be within a ±10% range around.

Therefore, on substituting V^*_{dc}= 33V, V_{dc} = 0.9 V^*_{dc} and Δe_{dc} = 0.215 J in (12) results in C_{dc} = 2.073 mF. On the other hand, for V_{dc} = 1.1 V^*_{dc}, C_{dc} = 1.878 mF.

D. Isolation and driver circuits design

The objective is to digitally control the proposed SAPF to cancel the lower order harmonics and compensate the reactive power. To interface the DSP with the power circuit, isolation and driver circuits are required to switch the IGBT power transistors. The isolation circuit consists of six optocouplers TLP250. Each of them is preceded by 330 Ω to drive the optocoupler and followed by totem pole driver circuit of 2N2222 and 2N2907 and 10Ω series resistor to drive each of the six power transistors. The isolation and driver circuit is shown in fig. 4.

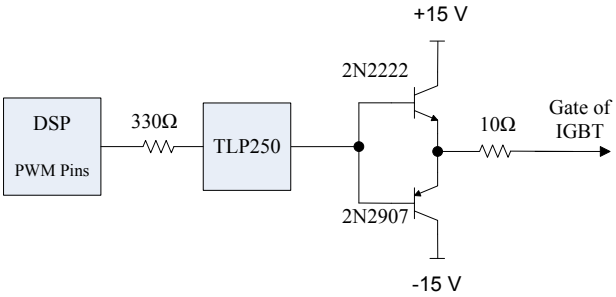

Fig. 4 The circuit diagram of isolation and driver circuit

The DSP requires 0-3.3V. The measured load currents from Hall sensors i_{La} , i_{Lb} and i_{Lc} and the ideal source voltages e_a, e_b and e_c from step down transformers 220/6 V are offset corrected by TL081

based electronic circuits to meet this requirement.

The Motorola DSP56F807 is well-suited for digital control, combining the DSP's calculation capability with MCU's controller features on a single chip. This DSP offers many dedicated peripherals, including a Pulse Width Modulation (PWM) unit, an Analog-to-Digital converter (ADC), timers, communication peripherals (SCI, SPI, CAN), on-board Flash and RAM.

The PWM unit has inserted dead time which is programmed as 2 μs and implements ramp comparison by comparing the PWM value register (pulse width) with the PWM modulus register (period) in the edge aligned mode. The Motorola DSP56F807 has two dual, four-inputs, 12-bit ADCs named ADCA and ADCB, totaling 16 analog inputs. In this work, ADCA module was used employing seven A/D inputs used for three AC voltages, one DC voltage and three AC load currents.

4. Experimental Results

The structure of the inverter used for testing the digital controller is shown in figure 3. V_{sa} = 12V and the IGBTs are 400V, 30 amp. (rated) SKW30N60. The set up parameters of the system is as in table I.

Table I Set up parameters of the proposed system

Model parameter	value
Supply voltage (rms)	12 V
Active filter parameters	R_c =1 Ω , L_c=1.7mH
DC link capacitance	2 mF
Load power	0.1kVA
Nonlinear load	R=5.7 Ω , L= 107 mH
Switching frequency	5000 Hz

The proposed system was tested to show its adaptive capability to compensate parameters uncertainties, frequency variations and step load change. The proposed system was tested for three cases:

A) *Open loop controlled SAPF without feedback signals.*

B) Closed loop controlled SAPF using the inverter model (Processing the reference filter currents through the model).

C) Closed loop controlled SAPF without the model (Processing the reference filter currents directly).

A. Open loop controlled SAPF

Fig. 5 shows the block diagram of proposed system in open loop mode. In the open loop mode, there are no feedback signals. The duty cycles were placed directly in the registers in the PWM unit of DSP56F807. The DC reference voltage was specified approximately by appropriate values of the duty cycles.

A.1 Transient response of open loop control

Fig. 6 shows the DC voltage response of SAPF in open loop mode without feedback signals. It was shown that the rise time is more than 1.5s (3 devisions of 500ms/dev.) resulting in slower response than closed loop system. Also, the THD of source currents after compensation was increased to about 14% as shown in fig. 7. However, this response ensures the robust performance of DSP to be used in closed loop system as shown in the next subsection.

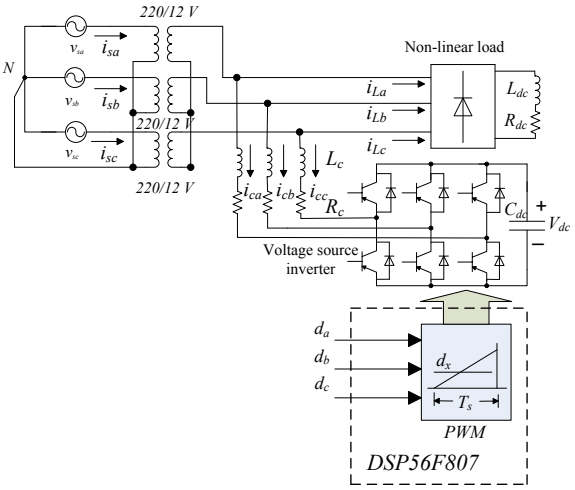

Fig. 5 the block diagram of open loop controlled SAPF

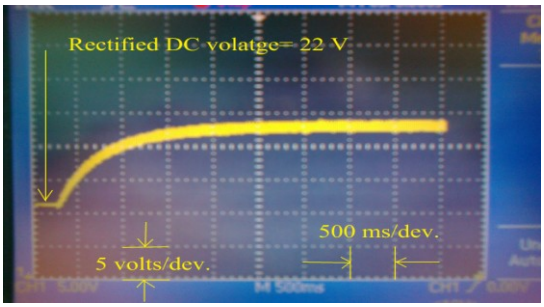

Fig. 6 The DC voltage response of open loop SAPF

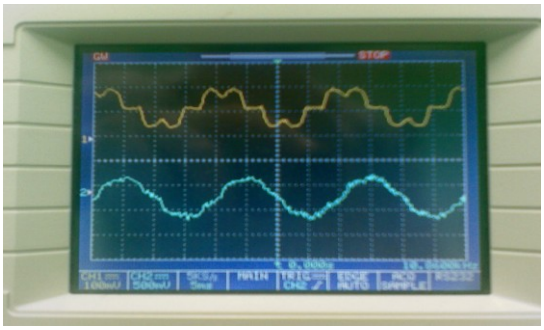

Fig. 7 The nonlinear load and source current after compensation in open loop mode

A.2 Step change of load

Fig. 8 Shows the DC voltage response of open loop controlled SAPF due to step change of the load resistance from 5.7 Ω to 7.3 Ω where there is small step in the DC voltage of the capacitor from 34V to 36V.

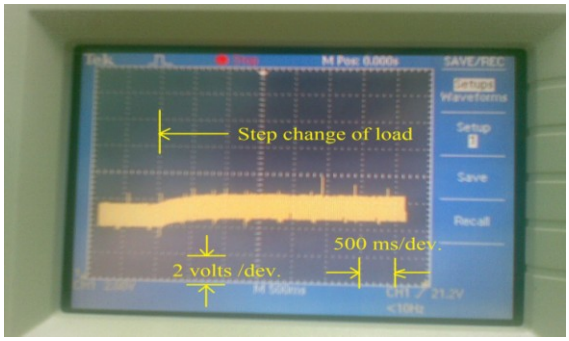

Fig. 8 The DC voltage response due to step change of load.

B. Closed loop controlled SAPF

B.1 Harmonic and reactive power compensation

Figures 9 and 10 show the source currents and voltages after compensation. This technique proved its superior performance by decreasing the THD from 29% to about 8% as shown in table II and achieves enhanced reactive power compensation. Also, as in fig. 11, the DC voltage response has faster transient response about 250 ms without overshoot or undershoot and low ripple voltage less than 3% at V_{dc}= 34V.

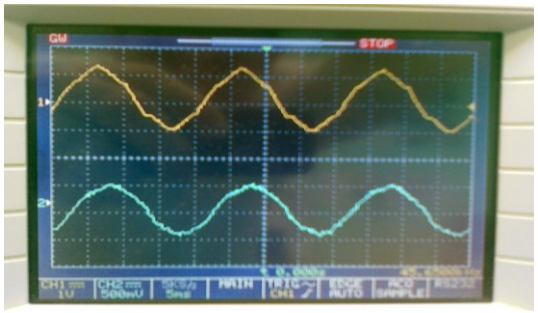

Fig. 9 The source currents and voltages of DSP based SAPF

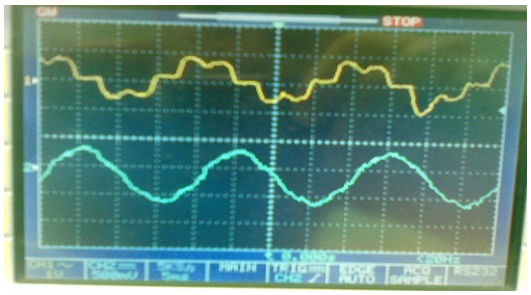

Fig. 10 The nonlinear load and source currents after compensation.

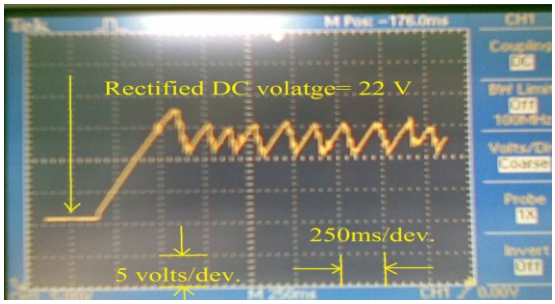

Fig. 11 The DC voltage response of DSP based SAPF

Table III THD of source current and voltage

THD% / Compensation	I_s	V_s
Without compensation	28.97%	2.47%
compensation SAPF	8.08%	1.47%

B.2 Compensation of filter capacitance uncertainties

Figures 12 and 13 show the DC voltage response of SAPF for variation of its capacitance when its value was decreased to half of its value at V_{dc} = 31 V. It was shown that the steady state DC voltage error is zero in both cases. Also, the rise time is about 200 ms (1 devision = 250ms) for the designed value 2 mF compared to the decreased value of C_{dc} = 1 mF which results in faster response (100 ms rise time) with higher overshoot from 15% to 25%. The THD of source currents after compensation may be not affected as shown in fig. 14.

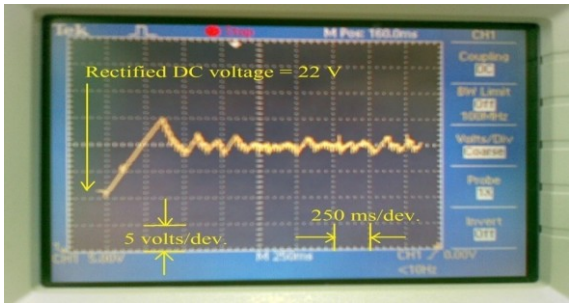

Fig. 12 The DC voltage response for the normalized C_{dc}

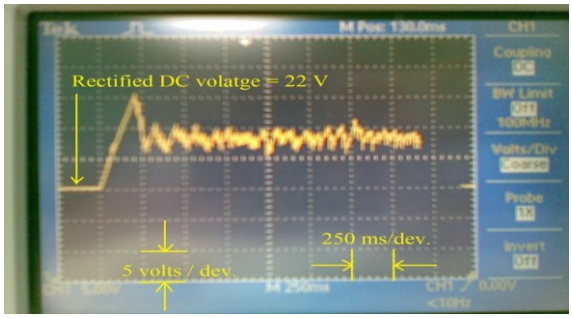

Fig. 13 The DC voltage response for -50% of C_{dc} uncertain.

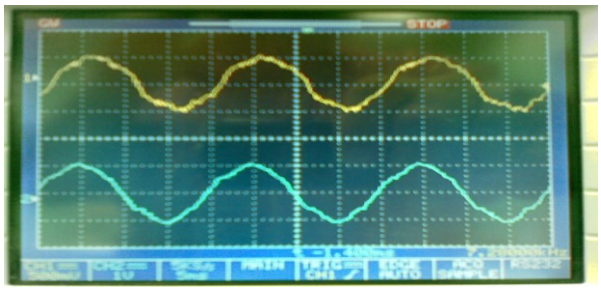

Fig. 14 The source current and voltage for half value of C_{dc}

Fig. 15 shows the DC voltage response has the same reference value i.e. the steady state DC voltage error is still zero for -75% uncertainties (C_{dc}=0.5mF). It is clear the response has faster rise time 40 ms with higher overshoot 45%. It can be concluded the proposed system has robust performance against large capacitance variations. The system has increased overshoot as the capacitance value deviates from its value.

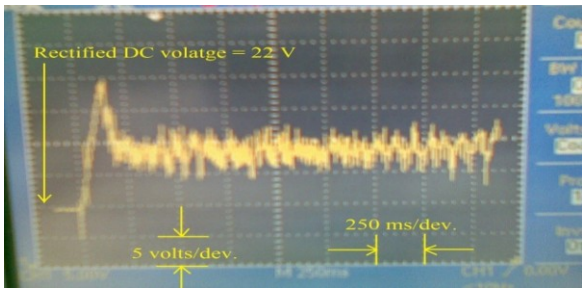

Fig. 15 The DC voltage response for -75% of C_{dc} uncertain.

B.3 Compensation of R_c and L_c uncertainties

This aspect tests the effect of R_c and L_c uncertainties when it was subject to 50% of R_c uncertainties as shown in fig. 16. As shown, the DC voltage response has the same rise time (200ms) without steady state error. The effect of uncertainties to increase the THD to about 11% was depicted in fig. 17.

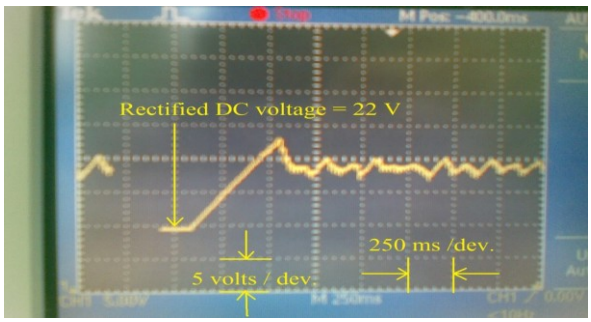

Fig. 16 The DC voltage response of SAPF for 50% of R_c uncertainties

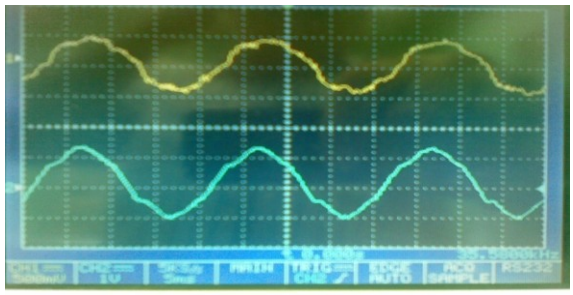

Fig. 17 The source currents of SAPF for 50% of R_c uncertainties

Fig. 18 shows the response of the DC voltage response due to the effect of increased 30% of L_c uncertainties. The THD of the source currents was little increased to 9% as shown in fig. 19. But, the steady state DC voltage error was zero in both cases of R_c and L_c uncertainties to ensure the adaptive capability and the robust performance of the proposed DSP based SAPF against large parameters uncertainties.

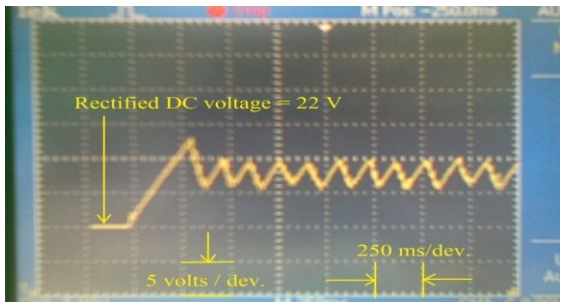

Fig. 18 The DC voltage response of SAPF for 30% of L_c uncertainties

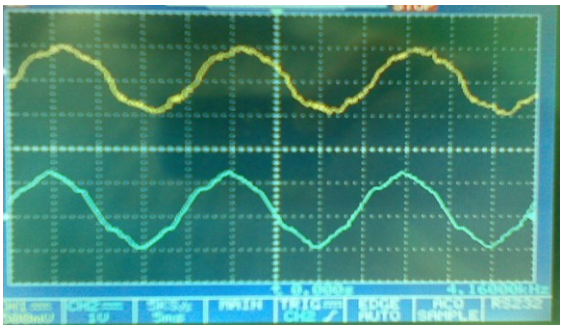

Fig. 19 The source currents of SAPF for 30% of L_c uncertainties

B.4 Compensation of switching frequency variations

This test shows the effect of switching frequency variation on the DC voltage response which may be the indication of stability of the proposed system. As shown in figs. 20, 21 and 22, the switching frequencies f_s are 7 kHz, 5 kHz and 4.5 kHz respectively at V_{dc} = 31 V and the steady state DC voltage errors are zero for all these frequencies. The rise time for these frequencies equals 150 ms, 200 ms and 250 ms

respectively. It can be concluded that the system is adaptable to frequency variations and the ac ripples decrease as the frequency decrease.

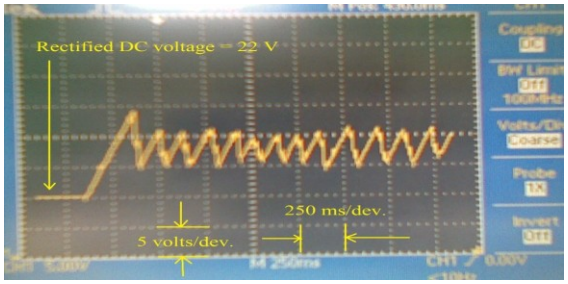

Fig. 20 The DC voltage response at f_s=7kHz

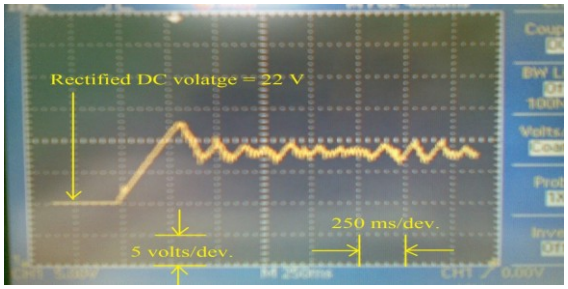

Fig. 21 The DC voltage response at f_s=5kHz

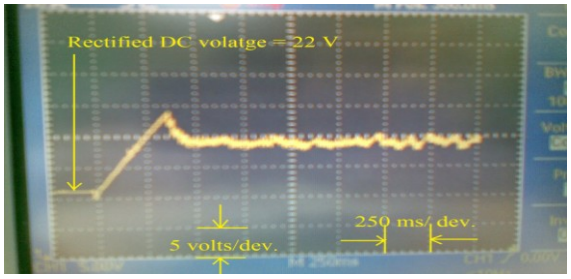

Fig. 22 The DC voltage response at f_s=4.5kHz

B.5 Step load change

Fig. 23 shows the robust performance of the proposed SAPF due to step load change from 5.7 Ω to 7.3 Ω. As shown, there is no change except some improvement in the DC voltage decreasing the ripple in the capacitor voltage from 0.6 Vac to 0.3 Vac that means the ripple decreases as the AC nonlinear load currents decrease. As shown in Fig. 24, there is little increase in THD of the source current due to the step change of load.

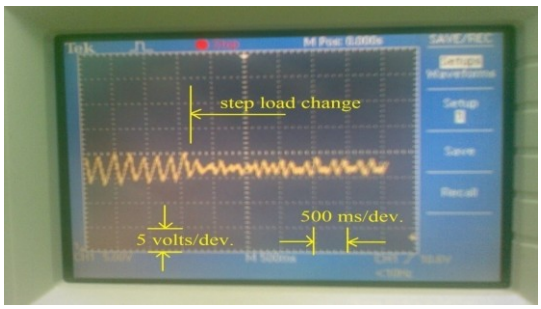

Fig. 23 The DC voltage response of closed loop SAPF due to step load change.

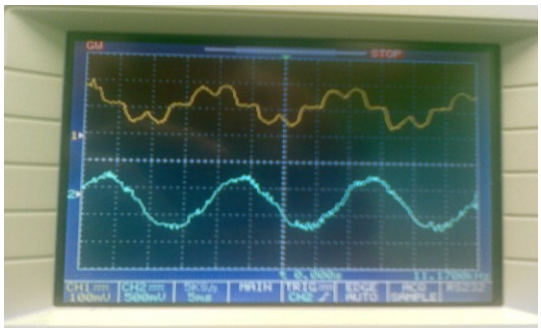

Fig. 24 The source currents of SAPF due to step load change.

C. Closed loop controlled SAPF without inverter model

Fig. 25 shows the block diagram of the proposed system without the inverter model where the reference filter currents are processed directly by multiplying them by constant gain.

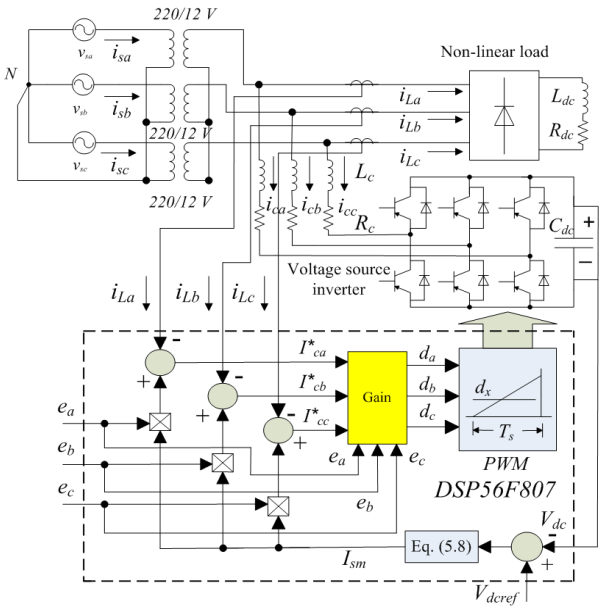

Fig. 25 The block diagram of the implemented proposed system using constant gain

Fig. 26 shows the load and source current after compensation using constant gain without the model to show the effectiveness of using the model to obtain the sinusoidal shape of the source current and avoiding the distortion of load current as shown in fig. 9.

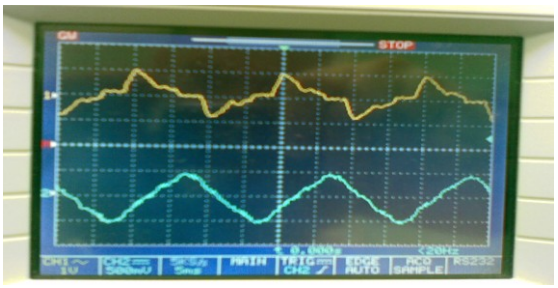

Fig. 26 The load and source currents after compensation without the model

CONCLUSIONS

This paper presents a novel DSP56F807 based SAPF with minimal hardware expense and excellent performance. A laboratory prototype has been built to verify the performance of SAPF. The proposed system was implemented and the design details were given. Also, the model of the system was derived using the difference equations to be implemented on DSP. This method was proven to be feasible approach for design using new version of the inverter model for DSP implementation.

This method has many advantages such as low switching frequency to decrease the switches losses, reduced hardware components, the ability to adapt to varying loads and switching frequency in real time, doesn't use any transformations and the current control system is reduced to one equation only (7).

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