HIGH FREQUENCY PARAMETRIC ANALYSIS OF DISCRETE COMPONENTS USING CURRENT DRIVEN RADIATION ALGORITHM

T.Pearson[1] and **M.Madheswaran**[2]
Center for Advanced Research, Dept of Electronics and Communication Engineering,
SMK Fomra Institute of Technoilogy[1], Chennai, Muthayammal Engineering College[2], Rasipuram, Tamil nadu, India
Tel: 94444081062, e-mail: pearsonin@gmail.com

Abstract:

There can be various EMC expert systems developed for analyzing the PCB. The algorithms used to predict possible radiated emissions problems from a printed circuit board have been presented. From accuracy point of view, the expert system approach is approximately equal to human EMC expert with a through knowledge of the board and a calculating aid. The algorithms also make assumptions and approximations about how the board will interact with the rest of the system.

Keywords: *EMC, EMS, Standards, Expert System.*

I. Introduction

Electromagnetic compatibility (EMC) often refers to one of the mysteries in the field of electrical and electronic engineering, as the EMC behavior of a product is unpredictable. In most cases, the EMC performance of the product cannot be found precisely with the highest level of simulation tools [1]. No single simulation software covers all the parameters and the rules governing the EMC design. Most of the engineers rely on measurement and testing methods after the prototype of the product is fabricated. In large-scale electrical and electronic projects, the end result may be catastrophic when there are critical EMC problems identified after the completion of infrastructure.

II. History

In the early days of electrical engineering in 1800s, all electrical systems were used for heating, lighting and machinery driving were controlled by simple on/off switches. EMC problems did not appear in these simple systems. A break through on the semiconductor technology in 1970s significantly increased the EMI problem. High frequency switching elements began to be widely applied in power, digital control and communication systems. Source of EMI was not only limited to simple switching but also to a wideband, high frequency and high power source. Furthermore, the digital control circuits were widely adopted, which were more vulnerable towards the noise. A switching power supply was a typical example of the EMI problem at this stage when it comprises both high power switching and digital control circuits. Engineers could no longer rely on the traditional techniques to solve EMI problems. New tactics were developed using shielding and filtering and using border team electromagnetic compatibility (EMC) between products was defined.

The EMI reduction techniques have evolved over three decades. They are used as general design rules instead of precise calculations. At the beginning of the 21st century, new EMC reduction techniques have been developed to direct towards the integration approach with full computer simulation technologies. Making use of computer simulation together with artificial intelligence optimized EMC solutions can be generated automatically. Before a full set of automatic EMC solution is available, research should focus on the solution of individual EMC parameters using the de-coupled method. Hopefully these solutions should be integrated into an ultimate solution in the future.

Although there are many computer modeling tools are available, those are rarely being used for analyzing the PCB's. Computer modeling can provide valuable insight to a board designer

as critical circuits are being placed and routed, but they are not good at identifying the unintentional emissions sources and coupling paths that result most EMC problems. Full wave modeling of printed circuit board is not a practical option considering the complexity of the latest technology. Even with infinite computational resources, the board designer would not have all the necessary information about the components, signals and software to do an accurate analysis. Further the EMI test procedures have repeatability issues that prevent their results from being accurately predicted by computer algorithms.

III. The Problem

Following rapid development of science and technology, human society has entered into a new era of information technology and communication in the 21st century. Today, the whole environment is surrounded by the significant levels of background electromagnetic noise emitted from mobile communication networks, computers, microprocessors, electrical appliances and so on. It is estimated that there is a 7% - 14% increase in the background.

The severe electromagnetic noise environment is hazardous towards electrical and electronic equipment, especially valuable electronic control system. The electromagnetic hazard is a cause for great concern around the world. A world-wide study and research are then initiated for electromagnetic noise reduction techniques. Recent research not only concentrates on electromagnetic noise reduction, but also on compatibility between equipment and environment in electromagnetic aspects. Therefore a broader term electromagnetic compatibility (EMC) is referred to, to cover the wider scope. This means that the electrical/electronic equipment is compatible with each others without any deterioration in their function within a defined time and space.

EMC refers to two aspects, electromagnetic interference (EMI) and electromagnetic susceptibility (EMS). EMI refers to the noise level generated by the equipment, which causes interference with others while EMS refers to the immunity of equipment against electromagnetic noise from the environment. Equipment with good electromagnetic compatibility emits minimum noise to the environment as well as being able to resist the noise from the environment.

The existence of electromagnetic compatibility requires three conditions:

a) Equipment to generate electromagnetic noise - (source)

b) Equipment to receive electromagnetic interference - (victim)

c) Media for the electromagnetic noise - (comply with)

Their relationship is illustrated in Figure 1.

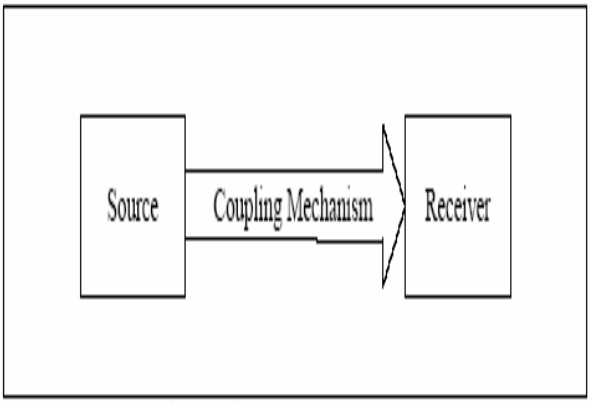

Fig. 1. Basic Elements in EMI Problems

The coupling path is the emission path of the electromagnetic noise. It is equivalent to the transmission of electromagnetic energy. Moreover, it is divided into conducted emission and radiated emission. Conducted emission requires certain transmission media but radiated emission does not require any. Radiated emission is classified into the near field and far field depending on the transmission distance d and the wavelength of the transmission wave λ. Generally, the transmission wave with $d < \lambda/2\pi$ refers to near field while $d < \lambda/2\pi$ refers to far field.

Near field interference can be further divided into electric field and magnetic field interference, which are commonly used as capacity interference and inductive interference respectively. Far field refers to the transmission of electromagnetic energy in free space, which is commonly used as radiation interference. The illustration in the Figure 2 shows a hierarchy of the coupling path of electromagnetic interference.

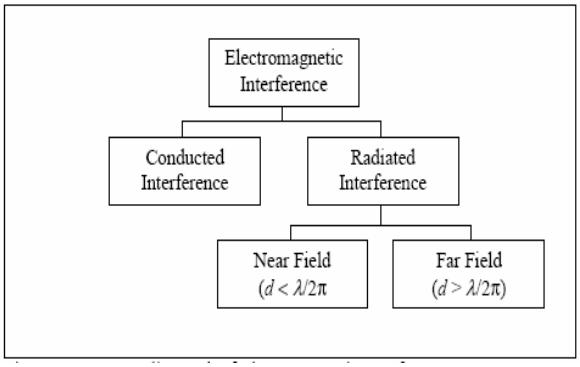

Fig. 2. Coupling Path of Electromagnetic Interference

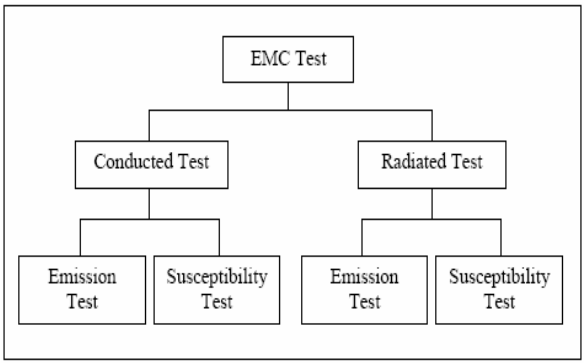

Fig. 3. EMC testing category

Electromagnetic interference relies on the following necessary elements, namely the source, comply path and victim. All suppression methods focus on either one of these factors such as suppressing the electromagnetic noise from the source, removing/reducing the coupling path and improving electromagnetic immunity of the victim.

IV.EMC Standards

In order to ensure a good electromagnetic environment and the compatibility between different electrical/electronic equipment, many countries and related international associations had defined a series of international standard for EMC, such as the US Federal Communications Commission (FCC), the International Electrotechnical Commission (IEC and CISPR), the European Committee for Electrotechnical Standardization (EN), the US Military Standard in EMC (MIL-STD-460), the Germany National Standard (VDE), and the French Standard (NFF) etc.

Any scientific measure on EMC of particular electrical/electronic equipment should rely on testing. This can verify the performance of the equipment in terms of EMC against international EMC standards. In accordance with the classifications of EMC, the tests are divided into emissions tests and susceptibility test. The emission test can be further divided into conducted emission test and a radiation emission test. Moreover, tests are developed in each stage of product design cycle i.e. research stage, breadboard stage, pre-fabrication stage, type-test stage, etc. The requirement for EMC testing equipment, testing method and the surrounding environment shall be deliberately defined before any tests are carried out. Figure 3 classifies the EMC testing.

V.Expert System

There can be various EMC expert systems developed for analyzing the PCB. One of the EMC expert system developed for PCB generally consists of four stages as listed below [2].

1. Input
2. Classification
3. Evaluation
4. Reporting

The board layout and component input data, the characteristics of all the net list and their signals are identified in the net classification stage. This information is passed to evaluate algorithms, which search for possible radiation or susceptibility problems. The basic structure of the PCB EMC expert system is shown in Figure 4.

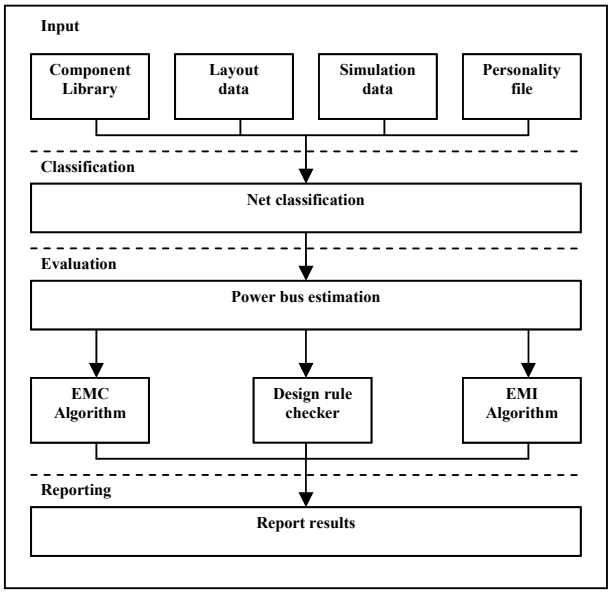

Fig. 4. Structure of the PCB EMC expert system

VI Current-Driven Radiation Algorithm

Considering the width of the printed circuit board to be finite, a portion of the magnetic field due to a signal current wraps around the board and there is an effective voltage drop across the return plane as shown in Figure 5. This voltage drop, in turn, can induce common mode currents that drive various EMI antennas on the printed circuit board[7]. These EMI antennas could be cables, heat sinks or other metallic structures.

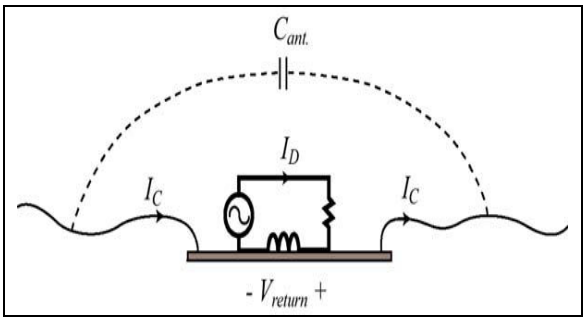

Fig 5. A simple configuration illustrating current-driven common mode configuration

The expert system estimates the voltage difference by approximating the branch inductance of the current return path as

$$L_p = (4 / \pi^2) \times [(\mu_o \, l \, h) / (dist1 + dist2)] \quad (1)$$

where

h - height of the trace over the return plane
dist1 & dist2 – two shortest distances between boundary of the board from midpoint of the segment
l - length of a segment
μo – permeability

The potential difference across the printed circuit board is calculated as

$$V_{ret} = \omega \, L_p \, I_{DM} \quad (2)$$

where

V_{ret} - return voltage
ω - angular frequency
L_p - branch inductance
I_{DM} – differential mode current

There can be three different possible EMI antennas are considered – cable to cable, cable to board and cable to heatsink.

(i) Cable-to-Cable Algorithm

This algorithm calculates the radiated field by a pair of cables connected to the board. For convenience, consider an isotropic radiator. Then, the relation between total radiated power and the voltage across the antenna port is,

$$P_{rad} = \oint \frac{1}{2} \frac{|E|^2}{\eta_o} ds = \frac{2\pi r^2 |E|^2}{\eta_o} = \frac{1}{2} I_C^2 \quad R_{rad} \quad (3)$$

where, $\eta_0 = 120\pi$. Considering the worst case, the maximum radiation occurs when the EM1 antenna resonates. At the resonance frequencies, the input impedance of the antenna is determined by the radiation resistance, R_{rad}, and the common mode current is,

$$I_C = \frac{V_{ret}}{R_{rad}} \quad (4)$$

The default radiation resistance, R_{rad}, used by this algorithm is 100 ohms, which corresponds to the input impedance of a typical worst-case resonant wire antenna. Since the radiated emissions are measured over a conducting plane, the field is multiplied by a factor of two. Finally, substituting in the equation and considering a typical measurement setup, the maximum E field is given by,

$$E \approx 2 \times \sqrt{\frac{30}{100}} \cdot \frac{V_{ret}}{3} = 0.365 \; V_{ret} \quad (5)$$

(ii) Cable-to-board algorithm

Even if only one cable is connected to the board, it may be driven relative to the board resulting in common-mode current. This algorithm is similar to the cable-to-cable algorithm, except that an effective capacitance, C, is defined between the cable and the board. The common-mode current is then given as

$$I_C = \frac{V_{ret}}{\sqrt{R_{rad}^2 + 1/(\omega \; C_B)^2}} \quad (6)$$

where the capacitance C_B, is approximated as the absolute capacitance of the board and estimated by the equation

$$C_B \approx \varepsilon_o \times \sqrt{Board\ Area} \quad (7)$$

By using the equations (6) and (7) and using the same approximations used in the cable-to-cable algorithm, the radiated emissions can be calculated as follows,

$$E \approx 0.365 \times \frac{100\ V_{rec}}{\sqrt{100^2 + 1/(\omega\ C_B)^2}} \quad (8)$$

(iii) Cable-to-heatsink algorithm

This algorithm calculates the radiated field due to common mode currents on an attached cable driven with respect to a heatsink. The approach is similar to that of cable-to-board algorithm but the effective capacitance of the heatsink is used instead of the board. The maximum field strength is given by

$$E = 0.365 \times \frac{100\ V_{rec}}{\sqrt{100^2 + 1/(\omega\ C_H)^2}} \quad (9)$$

VII. Expert system analysis of the test board

A multilayer test board is used to evaluate the expert system algorithms experimentally. This test board shown in figure 6 is developed for a study of the effects of layer spacing and dielectric materials on radiation algorithms.

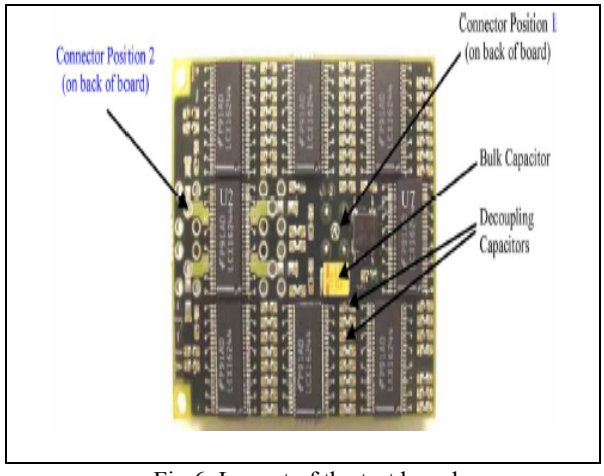

Fig.6. Layout of the test board.

The following diagram in the figure 7 illustrates layer stack up of the test board. The six-layer circuit board is of dimension 7.6cm x 5cm. In the test board Power and Ground planes are located on layer 3 and layer 4 with a spacing between them, 0.05 mm. Signals are routed on layer 2 and layer 5. The components consists of one 50-MHz oscillator, one bulk decoupling capacitor, eight octal clock buffers,

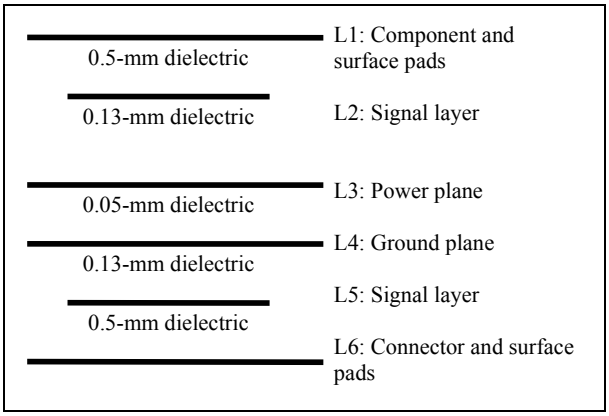

Fig 7. Layer stack up of the test board

28 load capacitors and 32 local decoupling capacitors. A 50-MHz oscillator drives the input pins of one of the octal clock buffers. The other buffers are driven by the first octal clock buffers. A subminiature type 'A' coaxial connector is used to connect to the power supply 3.3-V power to the printed circuit board. The 1-Ω resistors are connected in series with the four pins of one of the buffers, making it possible to measure the power currents to this buffer.

The test hoard is a 6-layer board using CMOS technology. The stack-up of the board is shown in Table I and the layout is shown in Figure 6. The large number of signal nets in this design makes it difficult to visually identify potential EMC problem.

Table – I Details of the stack-up of the Test Board

Layer	Material	Thickness	ε_r
Top	Metal Dielectric	1.2 mils 8.0 mils	1.0 4.5
GND	Metal Dielectric	1.2 mils 8.0 mils	1.0 4.5
VDD	Metal Dielectric	1.2 mils 8.0 mils	1.0 4.5
Bottom	Metal	1.2 mils	1.0

VIII. Board Analysis Using the Current-Driven Radiation Algorithm

The algorithm was first applied to the test board when the buffers were not loaded. For the board under analysis, there were no heatsinks, and there was only one cable attached to the board. Therefore, only the cable-to-board radiation was evaluated.

The parameters needed to calculate the radiation by the current-driven CM radiation algorithm and their values are listed in Table II.

Table II .Parameters needed for current driven algorithm

Parameter	Description	Value
L	Board length	7.6 cm
W	Board width	5.0 cm
h	Height of trace above plane	Depends on individual trace
l	Trace length	Depends on individual trace
ε_r	Dielectric permittivity	3.88
$dist1$	Shortest distance to one board edge	Depends on individual trace
$dist2$	Shortest distance to another board edge	Depends on individual trace
Δt	Current pulse width	3 ns
T	Period of the signal	20 ns
C_L	Load capacitance of the signal traces	16 x 7 pF

There were a total of seven signal traces on the second layer of the board contributing to the current-driven common mode radiation. One of the eight clock buffer ICs was driving the remaining seven clock buffer ICs. The signal current on each trace was approximated as a triangular pulse with a pulse width of Δt, a period of T, and a peak value of $I_p = C_L V_{CC}/\Delta t$. Figure 8 shows the envelope of the maximum estimated radiated emissions calculated using the current-driven CM radiation algorithm

At low frequencies (e.g., below 300 MHz), the radiation is limited primarily by the ability of the board-cable structure to form an efficient antenna. At higher frequencies, the radiation falls off in proportion to the amount of energy in the source current waveform as illustrated in the figure 8.

The high frequency parametric and structural analysis of the Current-Driven Radiation Algorithm for the test board is illustrated in the figure 9 and 10.

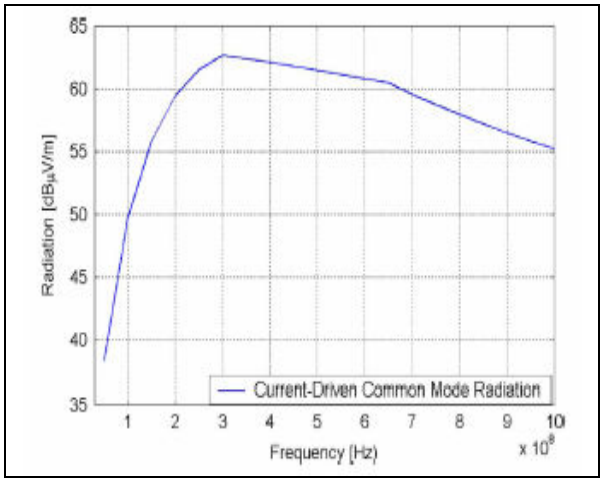

Fig. 8. Maximum emissions calculated using the current-driven common mode radiation algorithm.

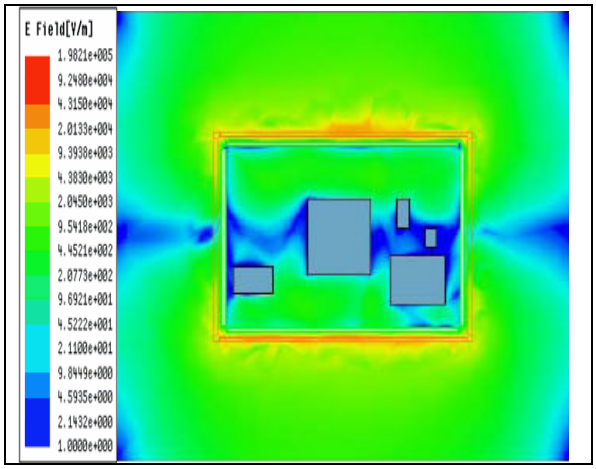

Fig. 9. High frequency parametric and structural analysis of the H-field in Current-Driven Radiation Algorithm

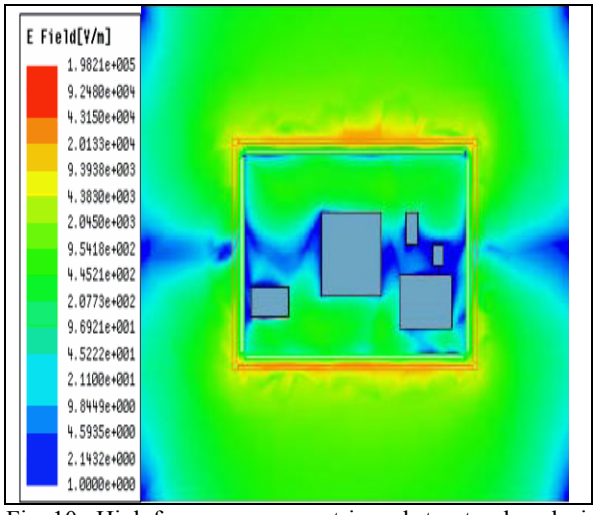

Fig. 10. High frequency parametric and structural analysis of the E-field in Current-Driven Radiation Algorithm

IX. Conclusion

Although both of the layout problems identified by the EMC expert software system might have been obvious to an EMC engineer who was familiar with the board and the signals on each of these nets, a lot of effort would have been required to initially locate these problems manually. If changes were made to the layout, this effort would have to be repeated to ensure that no new problems were created. The expert system algorithms are designed to help both experts and non-experts find major potential problems early in the design process without manually examining every net routed on the board.

For more than 40 years, researchers have been pursuing the development of measurement methods, prediction tools, and design techniques for improving the EMC performance of ICs. Looking to the future, there are many difficult challenges ahead, most without clear solutions. A set of issues was highlighted, regarding low-emission design techniques, high-immunity guidelines, extremely high-frequency measurement techniques, as well as efficient methodologies for reliable prediction of EMC performance prior to manufacture. The field of EMC at the component level has grown much beyond the expectations of one or two decades ago. EMC expertise has successfully weathered and, in fact, thrived on the IC technology scale-down. We expect component-level EMC to continue to be an active field of study in the future, as ICs become larger, denser, and operate at higher clock speeds and lower supply voltages. We hope this paper provides readers with a sense of the past and future trends in EM compliance of ICs, following the extraordinary advances of the microelectronics industry.

References

[1] H. Shim, T. Hubing, T. Van Doren, R. DuBroff, J. Drewniak, D. Pommerenke, and R. Kaires, "Expert system algorithms for identifying radiated emission problems in printed circuit boards," in Proc. IEEE Int. Symp. Electromagn. Compat., Santa Clara, CA, vol. 1, Aug. 9–13, 2004, pp. 57–62.

[2] H. Shim and T. Hubing, "Model for estimating radiated emissions from a printed circuit board with attached cables driven by voltage-driven sources," IEEE Trans. Electromagn. Compat., vol. 47, no. 4, pp. 899–907, Nov. 2005.

[3] H. Shim and T. Hubing, "Derivation of a closed-form approximate expression for the self-capacitance of a printed circuit board trace," IEEE Trans. Electromagn. Compat., vol. 47, no. 4, pp. 1004–1008, Nov. 2005.

[4] D. Hockanson, J. Drewniak, T. Hubing, F. Sha, and M. Wilhelm, "Investigation of fundamental EMI source mechanisms driving common-mode radiation from printed circuit boards with attached cables," IEEE Trans. Electromagn. Compat., vol. 38, no. 4, pp. 557–565, Nov. 1996.

[5] H. Shim, Y. Fu, and T. H. Hubing, "Radiated emissions from populated printed circuit boards due to power bus noise," in Proc. IEEE Int. Symp. Electromagn. Compat., Santa Clara, CA, vol. 2,Aug. 9–13, 2004, pp. 396– 400.

[6] H. Shim and T. Hubing, "A closed-form expression for estimating radiated emissions from the power planes in a populated printed circuit board," IEEE Trans. Electromagn. Compat., vol. 48, no. 1, pp. 74–81, Feb. 2006.

[7] F. Schnieder and W. Heinrich, "Model of thin-film microstrip line for circuit design," IEEE Trans.Microw. Theory Tech., vol. 49, no. 1, pp. 104– 110, Jan. 2001. [17] M. Leone, "The radiation of a rectangular power-bus structure at multiple cavity-mode resonances," IEEE Trans. Electromagn. Compat., vol. 45, no. 3, pp. 486–492, Aug. 2003.

[8] J. Fan, W. Cui, J. L. Drewniak, T. P. Van Doren, and J. L. Knighten, "Estimating the noise mitigation effect of local decoupling in printed circuit boards," IEEE Trans. Adv. Packag., vol. 25, no. 2, pp. 154–165, May 2002.

[9] Y. Fu, G. L. Burbui, and T. Hubing, "An improved model for representing current waveforms in CMOS circuits," Clemson Veh. Electron. Lab., Clemson, SC, Tech. Rep. CVEL-06-01, Sep. 2006.

[10] J. L. Levant, M. Ramdani, E. Tinlot, and R. Perdriau, "ICEM modeling of microcontroller current activity," Microelectron. J., vol. 35, no. 6, pp. 501–507, Jun. 2004.

[11] S. B. Dhia, M. Ramdani, and E. Sicard, Electromagnetic Compatibility of Integrated Circuits—Techniques for Low Emission and Susceptibility. New York: Springer-Verlag, 2006.

[12] C. Lochot, S. Calvet, S. B. Dhia, and E. Sicard, "Regina test masks: Research on EMC guidelines for integrated automotive circuits," Microelectron. J., vol. 35, no. 6, pp. 509–524, Jun. 2004.

[13] D. Panyasak, G. Sicard, and M. Renaudin, "A current shaping methodology for lowering EM disturbances in

asynchronous circuits," Microelectron. J., vol. 35, no. 6, pp. 531–540, Jun. 2004.

[14] J. Park, A. C.W. Lu, and K.M. Chua, "Double-stacked EBG structure for wideband suppression of simultaneous switching noise in LTCC-based SIP applications," IEEE Microw. Wireless Compon. Lett., vol. 16, no. 9, pp. 481–483, Sep. 2006.

[15] E. Lamoureux, "Etude de la susceptibilite des circuits integres numeriques aux agressions hyper-frequences" Ph.D. dissertation, Nat. Inst. Appl. Sci. (INSA), Toulouse, France, Jan. 2006.

[16] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system-on-package: Status and challenges," IEEE Trans. Adv. Packag., vol. 27, no. 2, pp. 286–300, May 2004.

[17] J. Park, H. Kim, Y. Jeong, J. Kim, J. S. Park, and D. G. Kam, "Modeling and measurement of simultaneous switching noise coupling through signal via transition," IEEE Trans. Adv. Packag., vol. 29, no. 3, pp. 548–559, Aug. 2006.

[18] K. Murano, F. Xiao, andY. Kami, "An immunity/susceptibility test method using electromagnetic wave of rotating polarization," IEEE Trans. Instrum. Meas., vol. 53, no. 4, pp. 1184–1191, Aug. 2004.

T.Pearson received B.E. and M.E. degrees in electronics engineering from Bharathiar University, Coimbatore, India. He is currently working towards Ph.D in electronics and communication engineering from Bharath University, Chennai, India.

He is currently a teaching faculty in SMK Fomra Institute of Technology. His research interests include the study of electromagnetic interference effects on CMOS digital circuits and digital circuits on VLSI systems particularly device modeling and circuit design.

Dr. M. Madheswaran has obtained his Ph.D. degree in Electronics Engineering from Institute of Technology, Banaras Hindu University, Varanasi in 1999. He obtained his M.E. degree in Microwave Engineering from Birla Institute of Technology, Ranchi, Bihar (Now Jarhand).

His field of interest includes semiconductor devices, microwave electronics, optoelectronics and signal as well as image processing. He is a member of IEEE, SPIE, IETE, ISTE, VLSI Society of India and Institution of Engineers (India).He is the Chairman, IEEE India Electron Devices Chapter for the year 2008 & 2009 and Vice Chairman IEEE India Solid State Circuits Chapter.