A Novel Compensator Based Four Switched Buck Converter

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Abstract: *Improving the efficiency and dynamics of power converters is a concerned tradeoff in power electronics. The increase of switching frequency can improve the dynamics of power converters, but the efficiency may be degraded. A double-frequency (DF) buck converter is proposed to address this concern. This converter is comprised of two buck cells: one works at high frequency, and another works at low frequency. It operates in a way that current in the high-frequency switch is diverted through the low-frequency switch. Thus, the converter can operate at very high frequency without adding extra control circuits. Moreover, the switching loss of the converter remains small. An ac small-signal model of the DF buck converter gives the dynamics of output voltage depends only on the high-frequency buck cell parameters, and is independent of the low-frequency buck cell parameters. Simulation results demonstrate that the proposed converter greatly improves the efficiency and exhibits nearly the same dynamics as the conventional high-frequency buck converter.*

Key words**:** *AC small-signal model, buck converter, efficiency, power conversion, switch inductor network.*

1. INTRODUCTION

The demand of high-performance power converter is increased dramatically with the broadening of power converter's application fields [1]. In order to improve the transient and steady state performance of power converters and to enhance power density, high switching frequency is an effective method. However, switching frequency rise causes higher switching losses and greater electromagnetic interference [2]. This, in turn, limits the increase of switching frequency and hinders the improvement of system performance. Active and passive soft-switching techniques have been introduced to reduce switching losses [3]-[6].Multi converter paralleling method, which employs low-power converters in parallel to enhance the power rating, has been proposed to enhance the power processing capability. However, parallel operation has interaction problem that causes circulating current [11], [12]. To avoid the circulating current, approaches such as isolation, high increase the control complexity. The interleaving operation employs N converters to operate in parallel with interleaved clocks, so the total dynamics can reach higher performance due to the fact that the equivalent frequency is N times the single converter frequency. Nevertheless, the circulating current phenomenon also exists.

A single-phase boost-type zero-voltage-transition (ZVT) pulse width-modulated converter proposed in [13] adopts an additional shunt resonant network to form an additional Boost cell to realize soft switching of the main switches. However, the auxiliary switches operate in hard switch and high frequency. A similar topology of single-phase rectifier is given in [14], where total harmonic distortion of the input line current is reduced and the efficiency improved. Its operation is different from the ZVT circuit. The boost-type topology, however, is not very effective to enhance the output voltage performance in that the capacitor ripple voltage is determined by the low frequency. Hence, this topology is not suitable for improvement of dc output transient and steady state performances. Moreover, the main Boost circuit and the added cell are coupled, and the added Boost cell has an effect on the inductor current input [15]. Splitting the filter inductor of buck converter into two parts with added auxiliary active switch and diode has been proposed to improve the output voltage response at load current step-down transient situation, but not at load current step-up transient situation [16]. Additional transformer and switches are needed to realize the improvement at step-up transient [17]. To make the circuits in [16] and [17] function as designed, it is required to detect the load transient event, then to trigger or shut down the auxiliary switch. This increases the complexity of the control circuit. Moreover, oscillations at the output voltage occur due to the frequent on and off operations at each transient event. On the other hand, high-frequency switching converter or linear power supply in parallel with low-frequency converter proposed in [18] and [19] enhances the output voltage response. Paralleling high-frequency converter approach also requires the load transient

information, while linear power supply method suffers from low efficiency. Moreover, the parallel structure brings about the circulating current problem. Additional current sharing control is needed to overcome this problem.

This paper proposes a novel converter topology to achieve high dynamic response and high efficiency of buck-type converters. This topology consists of a high-frequency buck cell and a low-frequency buck cell; and we call it the "double-frequency buck converter" (DF buck). The current flowing through the high-frequency cell is diverted by the low-frequency one, which also processes the majority of the converter power. This current decreases rapidly so that the high-frequency cell can work at very high frequency to improve the dynamic response. Furthermore, the efficiency is enhanced due to the low-current processing requirement of the high-frequency cell in the DF buck converter. Unlike the parallel structure, the proposed converter does not incur the circulating current problem [11], [12]. Moreover, it is not required to detect the load transient event for control. The circuit configuration and control strategy will be describe-ed in detail.

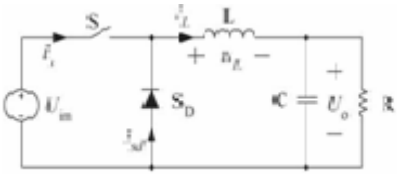


Fig1: schematic of buck converter

2. PROPOSED BUCK CONVERTER

The topology of a conventional buck converter is shown in Fig. 1. In the steady state, the input (U_{in}) and the output *(Uo*) of the converter are governed by

$$U_o = D.U_{in} \tag{1}$$

Where *D* is the duty ratio. If the buck converter works in the continuous conduction mode, then the inductor current i_L can be regarded as a current source. In each switching cycle, both the current flowing through the switch and the voltage across the diode is averaged. The converter excluding the added controlled current source (CCS) I_{La}, and its governing equations are

$$I_s = D.I_L \tag{2}$$

$$U_D = D.U_{in} \tag{3}$$

$$I_D = (1-D)I_L \tag{4}$$

In this paper, we propose to use a buck cell working at lower frequency to realize the CCS. The proposed converter is called the DF buck converter; because these buck cells work at two different frequencies. Schematic of this DF buck converter is shown in Fig. 3. The cell containing L, *S*, and S_D works at higher frequency, and is called the high-frequency buck cell. Another cell containi-

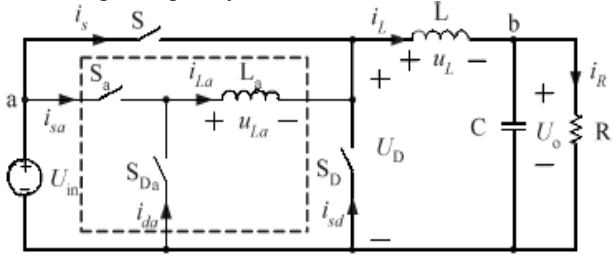


Fig 2. Schematic of the proposed DF buck converter

ng *La, Sa,* and SD*a* works at lower frequency, and is called the low-frequency buck cell. The high-frequency buck cell is used to enhance the output performance, and the low-frequency buck cell to improve the converter efficiency. An active switch, instead of a diode as in the conventional unidirectional buck converter, is employed to realize S_D in the high-frequency buck cell. This active switch transfers the energy stored in the low-frequency cell to the source during the transient stage of load step-down. It works complementarily with high-frequency cell switch *S*, and improves the transient response.

The switch *S* is controlled to operate at the high frequency f_h, and the corresponding switching period is T_{sh}. On the other hand, the switch S_a is controlled to work at a low frequency fi, and the corresponding switching period is T_{sl}. Assume that the high frequency is an integer multiples of the low frequency, i.e.,

$$f_h = M.f_l \tag{5}$$

At each low-frequency cycle, four switching states exist. Table I lists the switching states according to the status of switches *S* and *Sa*.

The state *a* denotes that both switches *S* and S_a are on. The equivalent circuit is shown in Fig. 3(a). In a similar manner, the equivalent circuits of states *b, c,* and *d* are shown in Fig. 3(b)-(d), respectively.

$$u_L = U_{in} - U_o \tag{6}$$

$$\frac{di_L}{dt} = \frac{u_L}{L} = \frac{U_{in} - U_o}{L} \tag{7}$$

$$u_{La} = 0 \tag{8}$$

$$\frac{di_{La}}{dt} = \frac{u_{La}}{L_a} = 0 \tag{9}$$

In this state, the voltage U_L across the inductor L is positive, and the voltage u_{La} across L_a is zero. Hence, the current i_L flowing through L rises, and the current i_{La} flowing through L_a does not change.

The governing equations of state *b* can be described by

$$u_L = -U_o \tag{10}$$

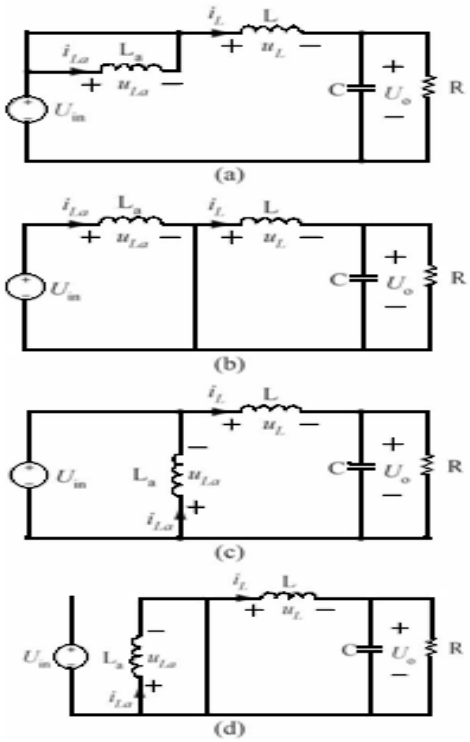
$$\frac{di_L}{dt} = \frac{u_L}{L} = \frac{-U_o}{L} \tag{11}$$

$$u_{La} = U_{in} \tag{12}$$

$$\frac{di_{La}}{dt} = \frac{u_{La}}{L_a} = \frac{U_{in}}{L_a} \tag{13}$$

TABLE I
SWITCHING STATES

State	Active Switches			
	S	S_a	S_D	S_{Da}
a	ON	ON	OFF	OFF
b	OFF	ON	ON	OFF
c	ON	OFF	OFF	ON
d	OFF	OFF	ON	ON



At this state, the voltage U_L across L is negative, so the current i_L decreases. The voltage U_{La} across La is positive, and the current i_{La} flowing through L_a rises.

In state c, the equivalent circuit equations are derived as

$$u_L = U_{in} - U_o \tag{14}$$

$$\frac{di_L}{dt} = \frac{u_L}{L} = \frac{U_{in} - U_o}{L} \tag{15}$$

$$u_{La} = -U_{in} \tag{16}$$

$$\frac{di_{La}}{dt} = \frac{u_{La}}{L_a} = -\frac{U_{in}}{L_a} \tag{17}$$

The voltage U_L across L is positive, so the current i_L rises. Since the voltage U_{La} across La is negative, the current i_{La} through La decreases.

Finally, the equations of state *d* are

$$u_L = -U_o \tag{18}$$

$$\frac{di_L}{dt} = \frac{u_L}{L} = \frac{-U_o}{L} \tag{19}$$

$$u_{La} = 0 \tag{20}$$

$$\frac{di_{La}}{dt} = \frac{u_{La}}{L_a} = 0 \tag{21}$$

The voltage U_L across L is negative, so the current i_L flowing through L decreases. The voltage U_{La} across La is zero, and the current i_{La} flowing through L_a remains the same.

From equivalent circuits, we find that the low-frequency buck cell does not affect the output inductor voltage, which has the same waveform and value as that of the conventional buck converter. That is, the voltage across the output inductor is $U_{in} — U_o$ when the switch is on, and is $—U_o$ when the switch is off. The voltage and current waveforms of DF buck in one low-frequency cycle T_{sl} are shown in Fig. 5, where $M = 4$. In the conduction mode of low-frequency switch, the voltage across the low-frequency inductor La alternates between zero and Uin . Thus, the equivalent slope of the current i_{La} is positive. At the switch-off interval, U_{La} varies from zero to $—U_{in}$, the equivalent slope of i_{La} becomes negative. As a result, if we employ proper control method, the low-frequency inductor can be controlled to follow the output inductor current.

3. Performance evaluation

The voltage mode control (VMC) circuit used to control the proposed DF buck converter is shown fig:4.in the control diagram ,the output voltage is fed back and compared with *Uref.* The output is continuously monitored and a corrective action is performed in the case the output voltage shifts from its intended value. The end result of the corrective action is a change in the duty cycle of the signal driving the switches. The challenge in the designing such a system is to make the control loop stab-

le. The transfer function of the error amplifier should be such that the whole system is unconditionally stable.

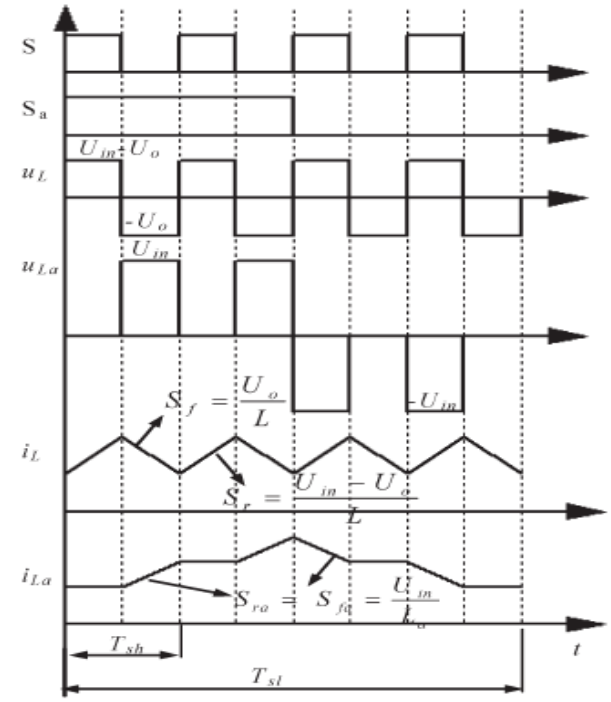


Fig4: voltage and current waveforms in one switching period.

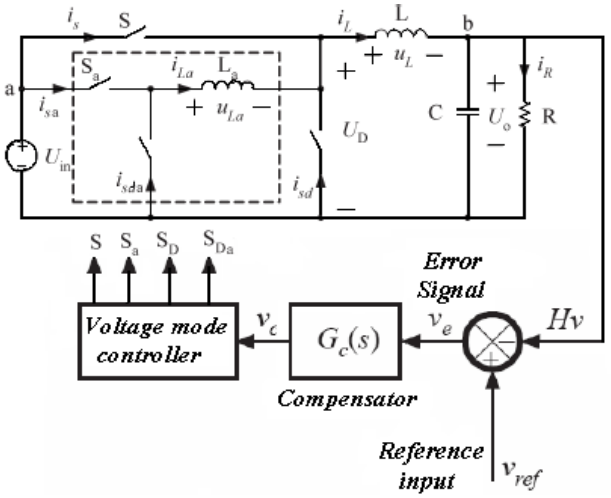


Fig.5.voltage mode control diagram.

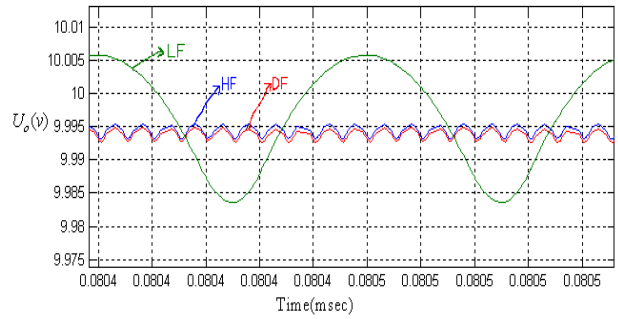


Fig.6 output voltage waveform comparison in steady state

A. Steady-state performance.

Performance of the DF buck converter is evaluated by looking at the steady-state response of three circuits: a DF buck, a single high-frequency buck converter whose switching frequency is the same as the higher frequency of DF buck, and a single lo-frequency buck converter whose switching frequency is equal to the lower frequency of DF buck. Parameters used in the simulation are

Uin=48v, Uo=10v, C=470μF

DF buck: L=100μH, La=1mH, f_l=10 kHz

f_h = 100 kHz

High-frequency buck: L=100μH, f=100 kHz

Low-frequency buck: La=1mH, f=10 kHz

The output voltage waveforms of the various buck converters are shown Fig: .it can be seen that the steady state performance of the DF buck and that of single high-frequency buck converter are almost the same.

B. Efficiency Analysis

In order to analyze the efficiency improvement of the proposed DF buck converter, the efficiency expression is analyzed in the section. The analysis is also applied to the single high frequency buck and low-frequency buck converters. Various loss estimation methods have been proposed in the literature based on different assumptions [20]–[23]. A simple loss model is adopted here [23] in that we just want to show the efficiency relationship between the DF buck and single high-frequency buck, not to develop a new loss model.

In the analysis, we have the following assumptions.

1) The conduction losses of active switch and diode are estimated, respectively, according to their conduction voltages U_{on} and U_F.

2) The switching transient processes are assumed to satisfy the linear current and voltage waveforms. Moreover, the turn-on time t_{on} is the same for all switches and diodes, so is the turn-off time t_{off}.

3) Since the switching loss usually dominates the total loss, losses of the output capacitor and output inductor are not calculated here

In a single-frequency buck converter, the total loss P_{SF} comes from four parts, the conduction loss P_{scon} and switching loss P_{ss} of the active switch S, and the conduction loss P_{dcon} and switching loss P_{sd} of the diode. When the input voltage is U_{in}, duty ratio is D, the inductor average current is I_L, and the switching frequency is f_s, the losses can be estimated according to the following equations [23]:

$$P_{scon} = D.U_{on}I_L \quad (22)$$

$$P_{dcon} = (1-D).U_F.I_L \quad (23)$$

$$P_{ss} = \frac{1}{2} f_s.U_{in}I_L(t_{on}+t_{off}) \quad (24)$$

$$P_{sd} = \frac{1}{2} f_s.U_{in}I_L(t_{on}+t_{off}) \quad (25)$$

For single-frequency buck converter, the conduction losses are the same; the difference is on the switching frequencies f_h and f_l. For DF buck, the losses consist of two portions: high frequency cell losses and low-frequency cell losses. The current chopped by the high-frequency cell is the difference between high-frequency inductor current i_L and low-frequency inductor current i_{La}. This difference is roughly equal to 0.5 I_{Lapk}, where I_{Lapk} is the peak–peak low-frequency inductor current ripple, because the inductor current ripple of the high-frequency cell is small compared with that of the low-frequency cell. Moreover, the average current in low-frequency inductor is $I_L - 0.5\ I_{Lapk}$ with the peak current control. The loss break down can be expressed as follows:

The losses in the high-frequency cell are

$$P_{sconH} = 0.5D.U_{on}I_{Lapk} \quad (26)$$

$$P_{dconH} = 0.5(1-D).U_F.I_{Lapk} \quad (27)$$

$$P_{ssH} = \frac{1}{4} f_h.U_{in}I_{Lapk}(t_{on}+t_{off}) \quad (28)$$

$$P_{sdH} = \frac{1}{4} f_h.U_{in}I_{Lapk}(t_{on}+t_{off}) \quad (29)$$

The losses in the low-frequency cell include

$$P_{sconL} = D.U_{on}(I_L - 0.5I_{Lapk}) \quad (30)$$

$$P_{dconL} = (1-D).U_F(I_L - 0.5I_{Lapk}) \quad (31)$$

$$P_{ssL} = \frac{1}{2} f_l.U_{in}(I_L - 0.5I_{Lapk})(t_{on}+t_{off}) \quad (32)$$

$$P_{sdL} = \frac{1}{2} f_l.U_{in}(I_L - 0.5I_{Lapk})(t_{on}+t_{off}) \quad (33)$$

Then, from (22)–(33), the total conduction loss P_{conDF} in the DF buck is approximately the same as that in the single-frequency buck converter

$$P_{conDF} \approx P_{scon} + P_{dcon} \quad (34)$$

In the case the low-frequency inductor current is small with reference to the inductor average current, the total switching loss P_{sDF} can be approximated as

$$P_{sDF} \approx f_l.U_{in}I_L(t_{on}+t_{off}) \quad (35)$$

It follows from (26)–(35) that the total conduction loss of DF buck converter is the same as the single-frequency buck conductor. This result also can be reasoned from the fact that the total currents flowing through the DF buck switches and diodes are the same as that through a single-frequency buck. On the other hand, the total switching loss is nearly the same as the single low-frequency buck, and is much smaller than that of the single high-frequency buck. Hence, the DF buck converter improves the efficiency by current diversion to the low-frequency cell. Although assumptions and approximations are made in the aforementioned analysis, it reveals the efficiency mechanism of the DF buck converter.

4. Experimental results

SIMULINK is used for simulation of power electronic converter fed electric drives with fixed or time varying loads. In addition to simulating the Power electronic circuits using components drawn from SimPowerSyst-ems Block set, it is possible to simulate the behavior of these circuits by using various blocks in the Simulink block set. The blocks can be suitably selected and defined to represent the mathematical equations that define the system being simulated. This is an added feature of software MATLAB/ SIMULINK.

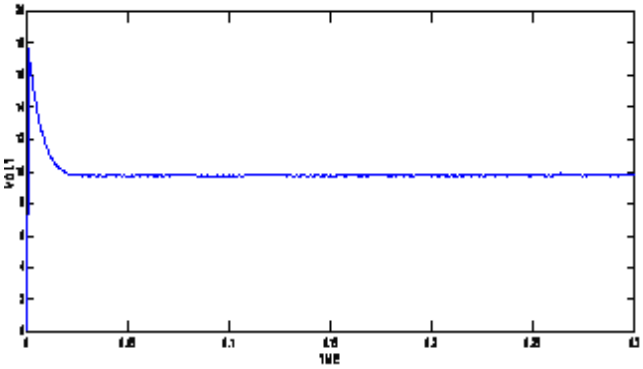


Fig.7.closed loop output voltage waveform

Three types of buck converters, which are low-frequency, high-frequency, DF buck converters whose output voltage compared with respect to the different frequencies. The switching losses in the DF buck converter are ten times lesser than the single frequency buck converter. If the switching losses is reduces the efficiency of the converter also increases. It is observed that the voltage ripple of magnitude of the high frequency buck and DF buck converter is same. The efficiency was calculated from the input power and the output power. Observe that the efficiency of DF buck is very close to that of the low-frequency buck converter, and both produce efficiency higher than the high-frequency one as shown in fig 8.

This means that DF buck can reach the dynamics of a high-frequency buck converter, and the efficiency is also improved at the same time. Thus, the proposed DF buck converter can be applied in high-performance high-efficiency application field of power converters.

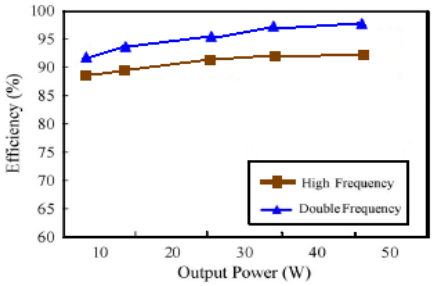


Fig. 8. Efficiency comparison

6. Conclusion

The four switched double frequency buck converter based compensator with voltage mode control technique is described in this paper. In particular this converter has efficiency and reduced switching losses ten times lesser as compared to conventional buck converter.

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