A NOVEL SIX-LEVEL INVERTER SYSTEM FOR DUAL-FED INDUCTION MOTOR DRIVE

G.SAMBASIVA RAO, Dr.K.CHANDRA SEKHAR
Dept. of Electrical Engg, R.V.R & J.C College of Engg, Chowdavaram, Guntur -522 019(India)
E-Mail:sambasiva.gudapati@gmail.com, cskoritala@gmail.com

Abstract: *In this paper, a new six-level inverter system for dual-fed induction motor drive is described. The dual-fed structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The six-level inversion is obtained by feeding the dual-fed induction motor with an asymmetrical 3-level inverter from one end and a symmetrical 3-level inverter from other end. This inverter scheme does not experience neutral point fluctuations and uses a lesser number of DC sources compared to the series H-bridge topology. A multilevel carrier based Sinusoidal Pulse Width Modulation is implemented for the proposed drive where a progressive discrete DC bias depending upon the speed range is given to the reference wave to reduce the inverter switchings.*

Key words: *Dual-fed induction motor, six-level inverter, carrier based SPWM, triangular carrier signal, reference sinusoidal signal.*

1. Introduction

Multilevel inverters are increasingly gaining importance for industrial and utility applications due to their numerous inherent beneficial features [1-5]. In particular, multilevel inverters allow the operation at higher dc voltages using semiconductor switches connected in series and produce voltage waveforms with better harmonic profile than conventional two-level inverters. There are three main topologies of multilevel inverters relevant for large induction motor drive applications: the extended neutral-point clamped inverters, series-connected H-bridge inverters and dual-fed induction motor drives.

The extended neutral-point clamped inverters experience neutral-point fluctuations as the DC link capacitors have to carry the load current [3]. The series-connected H-bridge topology of multilevel inverters has been suggested for induction motor drives and it requires separate DC supply for all three phases, which increases the power circuit complexity [4].

Feeding the dual-fed induction motor from both ends also results in a multilevel structure [5, 6]. In [5], a phase-shifted sine–triangle PWM is used for the multilevel voltage generation for the dual-fed induction motor drive, and in [6] a space-vector-based PWM approach is explained for three-level voltage-space vector generation for the dual-fed induction motor drive. The dual-fed structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The dual-fed induction motor is then fed by two inverters from the two ends of the winding. This technique has been used to implement a four-level inverter using two two-level inverters with asymmetric DC links [7]. A multilevel system that is capable of realizing a PWM waveform ranging from 2-level to 5-level is described in [10]. In the topology described in [10] an asymmetrical 3-level inverter and a 2-level inverter feed dual-fed induction motor. In the topology described in [11] capable of realizing a PWM waveform ranging from 2-level to 6-level is described. A multilevel system that is capable of realizing a PWM waveform ranging from 2-level to 8-level is described in [12]. In [12] two 3- level inverters feed dual-fed induction motor from both ends. The asymmetrical three-level inverter in [8, 12] is constituted by the cascade connection of two two-level inverters with unequal DC link voltage. In [14], two symmetrical three-level inverters feed the dual-fed induction motor to obtain the PWM waveforms ranging from two level to five level. In [15-17], different topologies of multilevel inverters, control strategies and applications are described.

In this paper, a new inverter topology to produce a multilevel PWM waveform ranging from 2-level to 6-level for the motor phase voltage for the dual-fed induction motor drive is proposed. In the proposed scheme, the dual-fed induction motor is fed with an asymmetrical 3-level inverter from one end and a symmetrical 3-level inverter from other end, asymmetrical three-level inversion is obtained by connecting two 2-level inverters with unequal DC link voltage in cascade and symmetrical three-level inversion is obtained by connecting two 2-level inverters with equal DC link voltage in cascade. This six-level inverter does not experience neutral point fluctuations and uses a lesser number of DC sources compared to the series H-bridge topology. In the multi level carrier based Sinusoidal Pulse Width Modulation used for the proposed drive, a progressive discrete DC bias depending upon the speed range is given to the reference wave. This results in a reduction of the switching ripple in the motor phase voltage waveform. This multilevel carrier based SPWM eliminates the use of look-up table approach to switch the appropriate space vector combination as in [11-13]. Dead times are present in the proposed multilevel carrier based Pulse Width Modulation and their effects on the voltage waveform are negligible.

2. Six-level inverter scheme for the dual-fed induction motor

The power circuit of the proposed drive is shown in Fig.1. An asymmetrical three-level inverter, Inverter-A and a symmetrical three-level inverter, Inverter-B feed the dual-fed induction motor. The inverter-A is composed of two conventional two-level inverters INV-1 and INV-2 in cascade. The Inverter-B is composed of two conventional two-level inverters INV-3 and INV-4 in cascade. The DC link voltages of INV-1, INV-2, INV-3 and INV-4 are (2/5)Edc, (1/5)Edc, (1/5)Edc and (1/5)Edc respectively, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive.

The leg voltage E_{A2n} of phase-A attains a voltage of (1/5)Edc if (i)The top switch S_{21} of INV-2 is turned on (Fig.1) and (ii) The bottom switch S_{14} of INV-1 is turned on. The leg voltage E_{A2n} of phase-A attains a voltage of (3/5)Edc if (i) the top switch S_{21} of INV-2 is turned on and (ii) The top switch S_{11} of INV-1 is turned on. The leg voltage E_{A2n} of phase-A attains a voltage of zero volts if the bottom switch S_{24} of the INV-2 is turned on. Thus the leg voltage E_{A2n} attains three voltages of 0, (1/5)Edc and (3/5)Edc, which is basic characteristic of a 3-level inverter. Similarly the leg voltages E_{B2n} and E_{C2n} of phase-B and phase-C attain the three voltages of 0, (1/5)Edc and (3/5)Edc.

The leg voltage $E_{A4n'}$ of phase-A attains a voltage of (1/5)Edc if (i)The top switch S_{41} of INV-4 is turned on and (ii) The bottom switch S_{34} of INV-3 is turned on . The leg voltage $E_{A4n'}$ of phase-A attains a voltage of (2/5)Edc if (i) The top switch S_{41} of INV-4 is turned on and (ii) The top switch S_{31} of INV-3 is turned on. The leg voltage $E_{A4n'}$ of phase-A attains a voltage of zero volts if the bottom switch S_{44} of the INV-4 is turned on. Thus the leg voltage $E_{A4n'}$ attains three voltages of 0, (1/5)Edc and (2/5)Edc, which is basic characteristic of a 3-level inverter. Similarly the leg voltages $E_{B4n'}$ and $E_{C4n'}$ of phase-B and phase-C attain the three voltages of 0, (1/5)Edc and (2/5)Edc.

Thus, one end of dual-fed induction motor may be connected to a DC link voltage of either zero or (1/5)Edc or (3/5)Edc and other end may be connected to a DC link voltage of either zero or (1/5)Edc or (2/5)Edc. When both the inverters Inverter-A and Inverter-B drive the induction motor from both ends, six different levels are attained by each phase of the induction motor. If we assume that the points n and n' are connected, the six levels generated for phase-A are shown in Table 1. In this topology only ripple currents are flowing through the capacitors C1, C2, C3 and C4. As the load current is not flowing through the capacitors, the proposed topology eliminates the neutral point fluctuations occurred in the conventional neutral-point clamped (NPC) topology. Also the fast recovery neutral clamping diodes are excluded in this topology i.e. the number of power devices is less than NPC topology.

Table 1
The six levels realized in the phase-A winding

Leg-voltage of phase A E_{A2n}	Leg-voltage of phase A $E_{A4n'}$	Motor phase voltage $E_{A2A4} = E_{A2n} - E_{A4n'}$	Level
0	(2/5) Edc	-(2/5) Edc	Level 1
0	(1/5)Edc	-(1/5)Edc	Level 2
0	0	0	Level 3
(1/5)Edc	0	(1/5)Edc	Level 4
(3/5)Edc	(1/5)Edc	(2/5)Edc	Level 5
(3/5)Edc	0	(3/5)Edc	Level 6

3. Voltage space vectors of proposed scheme

At any instant, the combined effect of 120^0 phase shifted three voltages in the three windings of the induction motor could be represented by an equivalent space vector. This space vector Es, for the proposed scheme is given by

$$Es = E_{A2A4} + E_{B2B4} . e^{j(2\pi/3)} + E_{C2C4} . e^{j(4\pi/3)}. \quad (1)$$

By substituting expressions for the equivalent phase voltages in (1),

$$Es = (E_{A2n} - E_{A4n'}) + (E_{B2n} - E_{B4n'}). e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'}). e^{j(4\pi/3)} \quad (2)$$

This equivalent space vector Es can be determined by resolving the three phase voltages along mutually perpendicular axes, d-q axes of which d-axis is along the A-phase (Fig.2). Then the space vector is given by

$$Es = Es(d) + jEs(q) \quad (3)$$

Where Es(d) is the sum of all voltage components of E_{A2A4}, E_{B2B4} and E_{C2C4} along the d- axis and Es(q) is the sum of the voltage components of E_{A2A4}, E_{B2B4} and E_{C2C4} along the q-axis. The voltage components Es(d) and Es(q) can be thus expressed by the following transformation,

$$E_S(d) = E_{A2A4}(d) + E_{B2B4}(d) + E_{C2C4}(d) \quad (4)$$

$$E_S(q) = E_{B2B4}(q) + E_{C2C4}(q) \quad (5)$$

$$\begin{bmatrix} Es(d) \\ Es(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A2A4} \\ E_{B2B4} \\ E_{C2C4} \end{bmatrix} \quad (6)$$

By substituting expressions for the equivalent phase voltages in (6),

$$\begin{bmatrix} Es(d) \\ Es(q) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} E_{A2n} - E_{A4n'} \\ E_{B2n} - E_{B4n'} \\ E_{C2n} - E_{C4n'} \end{bmatrix} \quad (7)$$

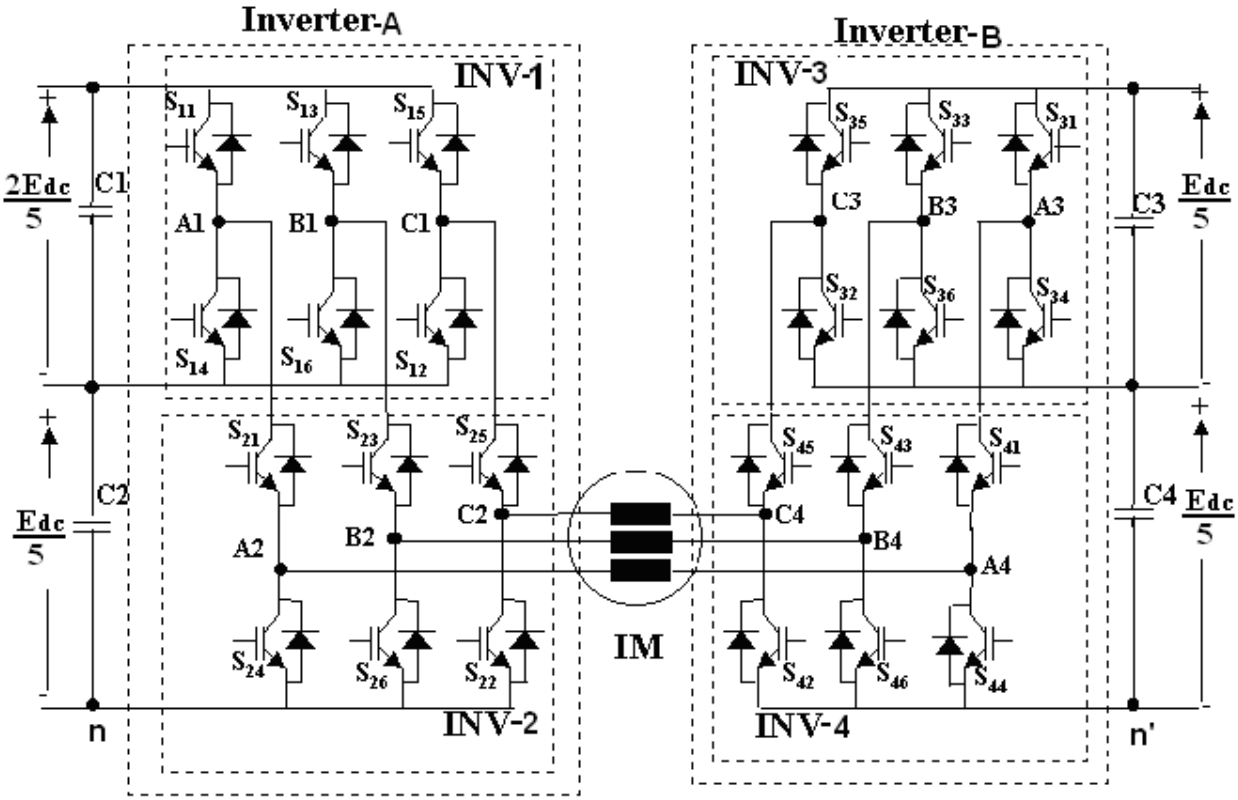

Fig.1 Schematic circuit diagram of the proposed 6- level inverter drive scheme.

The inverters can generate different levels of voltage vectors in the three phases of induction motor depending upon the condition of the switchings of inverter and for each of the different combinations of leg voltages, E_{A2n}, E_{B2n} and E_{C2n} for the inverter-A and $E_{A4n'}$, $E_{B4n'}$ and $E_{C4n'}$ for the inverter-B. The different equivalent voltage space vectors can be determined using (3) and (7). The possible combinations of space vectors will occupy different locations as shown in Fig.3. There are in total 91 locations forming 150 sectors in the space vector point of view. These space vector levels are identical to those of a conventional 6-level inverter.

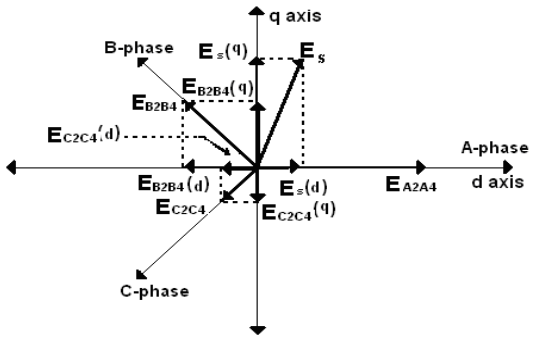

Fig.2 Determination of equivalent space vector from phase voltages

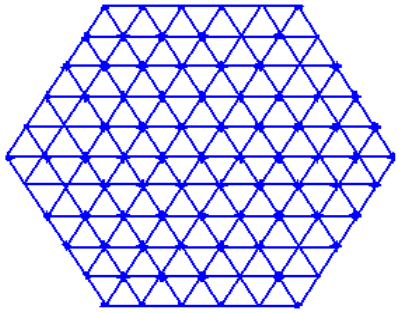

Fig.3 The voltage space vector locations for the proposed drive

4. Effect of Common-Mode Voltage in space vector locations

In the above analysis to generate the different levels and the space vector locations, the points n and n' are assumed to be connected. When the points n and n' are not connected (as in the proposed topology Fig.1), the actual motor phase voltages are

$$E_{A2A4} = E_{A2n} - E_{A4n'} - E_{n'n} \quad (8)$$

$$E_{B2B4} = E_{B2n} - E_{B4n'} - E_{n'n} \quad (9)$$

$$E_{C2C4} = E_{C2n} - E_{C4n'} - E_{n'n} \quad (10)$$

$E_{n'n}$ is the common-mode voltage and is given by

$$E_{n'n} = \frac{1}{3}(E_{A2n} + E_{B2n} + E_{C2n}) - \frac{1}{3}(E_{A4n'} + E_{B4n'} + E_{C4n'}) \quad (11)$$

Substituting these expressions in (1)

$$E_S = (E_{A2n} - E_{A4n'} - E_{n'n}) + (E_{B2n} - E_{B4n'} - E_{n'n}).\ e^{j(2\pi/3)} + (E_{C2n} - E_{C4n'} - E_{n'n}).\ e^{j(4\pi/3)}$$

$$= (E_{A2n} - E_{A4n'}) + (E_{B2n} - E_{B4n'}).\ e^{j(2\pi/3)} + (E_{C2n} -$$

$E_{C4n'}$). $e^{j(4\pi/3)}$ - ($E_{n'n}$ + $E_{n'n}$. $e^{j(2\pi/3)}$ + $E_{n'n}$. $e^{j(4\pi/3)}$)

In this equation
($E_{n'n}$ + $E_{n'n}$. $e^{j(2\pi/3)}$ + $E_{n'n}$. $e^{j(4\pi/3)}$) = $E_{n'n}$ - ½ $E_{n'n}$ – ½ $E_{n'n}$ = 0

and the equation then reduces to
Es = (E_{A2n} – $E_{A4n'}$) + (E_{B2n} – $E_{B4n'}$). $e^{j(2\pi/3)}$ + (E_{C2n} – $E_{C4n'}$). $e^{j(4\pi/3)}$

This expression of Es is the same as (2), where the points n and n' are assumed to be connected. The above analysis depicts that the common-mode voltage present between the points n and n' does not effect the space vector locations. This common-mode voltage will effect only in the diversity of space vectors in different locations.

5. Modulation scheme for the proposed inverter

Multilevel carrier based Sinusoidal Pulse Width Modulation is used for the proposed inverter scheme. In the multilevel carrier based Sinusoidal Pulse Width Modulation, for an N-level inverter a set of (N-1) adjacent level shifted triangular carrier signals are used [8]. If the sinusoidal reference signal has peak amplitude E_m^* and frequency f_m, the modulation index is defined with reference to a triangular carrier signal of peak to peak amplitude of Ec (N-1) as

$$M_a = 2E_m^* / E_C (N-1). \quad (12)$$

For the six-level inverter drive structure, 5 triangular carrier signals T1 to T5, with peak to peak amplitude of E_C are used, as shown in Fig.4a. The peak to peak amplitude of each carrier is $E_C = (1/5)E_{max}$, where E_{max} is the maximum value possible for the modulating signal. These five triangular carriers divide the entire range of modulating signal to six regions S1 to S6, S1 being the region below the lowest carrier signal T1, S2 is the region between T1 and T2, S3 between T2 and T3, S4 between T3 and T4, S5 between T4 and T5 and S6 above T5. When the modulating signal is in a particular region a corresponding voltage level is applied across the motor phase winding as assigned below:

S1 => -(2/5) Edc; S2 => -(1/5) Edc;
S3 => 0 ; S4 => (1/5) Edc;
S5 => (2/5) Edc; S6 => (3/5) Edc (13)

Three 120^0 phase shifted sinusoidal signals with 20% third order harmonic components are used as the reference signals for the proposed carrier based Sinusoidal Pulse Width Modulation. The addition of third order harmonic components increases the maximum fundamental component voltage amplitude that can be generated using the Sinusoidal Pulse Width Modulation scheme [9]. These reference sinusoidal signals are continuously compared with the triangular carrier signals set to determine the region (S1, S2…S6) in which the instantaneous value of the reference sinusoidal signal exists. All the three phases are compared simultaneously. Gating signals for the two inverters (i.e. Inverter-A & Inverter-B) then can be generated such that the appropriate switching devices are switched to realize the particular level in a particular phase depending upon the region. As the modulation index M_a increases, the proposed inverter can give the two-level operation and progressively move to the three-level, four-level, five-level and to the six-level operation. For low modulation index such that $E_m^* \leq E_C/2$ where E_m^* is the peak value of the modulating signal, if the reference sinusoidal signal is placed at the middle of the lowest triangular carrier T1 as Fig.4b, the modulating signal exists only in two regions S1 or S2 and it will result in only two levels, Level 1 (-2Edc/5) and Level 2 (-Edc/5). In this case the switching losses are only due to two level inverter, INV-3. When the modulating index is increased such that $Ec/2 \leq Em^* \leq Ec$, an additional DC bias of Ec/2 is given to the reference signal such that it is at the middle of the two lower triangular carriers T1 and T2 and results in 3-level operation (Fig.4c). A similar progressive DC shift in steps of Ec/2 is given such that the inverter progressively moves through the Level 3, Level 4, Level 5 and to Level 6 (Fig.4d, Fig.4e and Fig.4f) operation. When the E/f control is used, these five ranges of voltage amplitudes correspond to five ranges in frequency. Therefore the range (denoted by x = 1, 2, 3…5) in which the frequency command falls can be used to determine the DC shift to be given to the reference sinusoidal signals and the reference sinusoidal signals can be represented by,

$Ea^* = Em \sin wt + 0.2\ Em \sin 3wt + x\ Ec/2$, (14)

$Eb^* = Em \sin(wt - 2\pi/3) + 0.2\ Em \sin 3wt + x\ Ec/2$, (15)

$Ec^* = Em \sin(wt - 4\pi/3) + 0.2\ Em \sin 3wt + x\ Ec/2$. (16)

6. Simulation results and discussion

The proposed inverter topology is simulated using MATLAB environment with open loop E/f control using multilevel carrier based Sinusoidal Pulse Width Modulation technique. The respective DC link voltages are (2/5)Edc, (1/5) Edc, (1/5) Edc and (1/5) Edc for the INV-1, INV-2, INV-3 and INV-4, where Edc is the DC link voltage of an equivalent conventional single two-level inverter drive. The speed reference is translated to the frequency and voltage commands maintaining E/f. Depending upon the frequency range, reference sinusoidal signals are generated according to (14), (15) and (16). The three reference sinusoidal signals are simultaneously compared with the triangular carrier set and the level at which the instantaneous value of the reference sinusoidal signal exists is determined. A DC link voltage (Edc) of 500 volts is assumed for simulation studies. Fig.5a shows the motor phase voltage (E_{A2A4}) in the lowest speed range where the inverter is operating in the two-level mode. In this case, Inverter-B is operating in the two-level mode, switching between 2Edc/5 (200V) and Edc/5 (100V) and Inverter-A is not operated, switched

to zero. In this range the switching losses only due to INV-3. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig.5b and Fig.5c respectively. Fig.6a shows the motor phase voltage in the next speed range and Inverter-B is now operated in the three-level mode, switching between 0, Edc/5 (100V) and 2Edc/5 (200V) whereas Inverter-A is still not operated. In this range the switching losses only due to INV-3 and INV-4. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig.6b and Fig.6c respectively. Fig.7a shows the motor phase voltage in next speed range in four-level operation , the Inverter-A is operating in the two-level mode, switching between 0 and Edc/5 (100V) and Inverter-B is operating in the three-level mode. During this range of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig.7b and Fig.7c respectively. Fig.8a and Fig.9a show the motor phase voltage in five-level operation and six-level operation as Inverter-A is operating in the three-level mode, switching between 0, Edc/5 (100V) and 3Edc/5 (300V) and Inverter-B is operating in the three-level mode. During these ranges of operation, motor phase current and normalized harmonic spectrum of motor phase voltage are shown in Fig.8b, Fig.8c, Fig.9b and Fig.9c respectively. The ratio of triangular carrier signal frequency to reference sinusoidal signal frequency is 48 for all ranges of operation. It can be observed that the motor phase voltage during 6-level operation is very smooth and close to the sinusoid with lower harmonics. Fig.10 shows the decrease of percentage of total harmonic distortion (%THD) in the motor phase voltage as the number of levels increased.

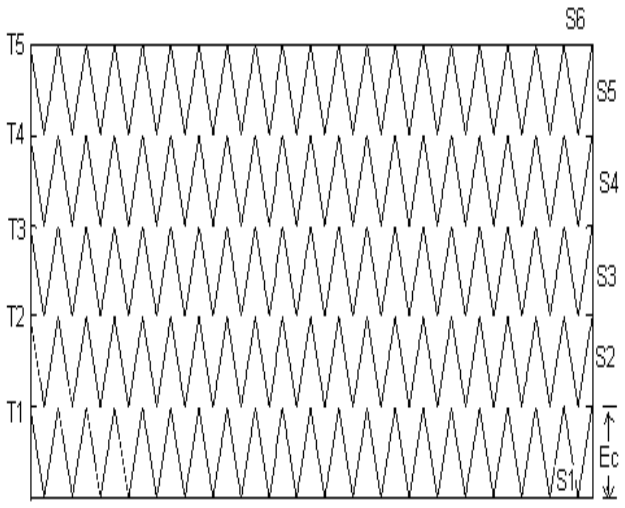

Fig.4a. Triangular carrier signals and the different regions in the multi carrier SPWM

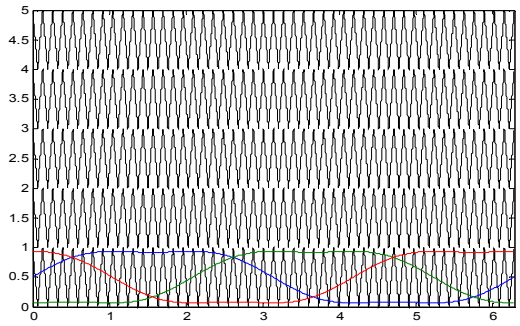

Fig.4b. Reference sinusoidal signal set for 2-level operation in the proposed SPWM

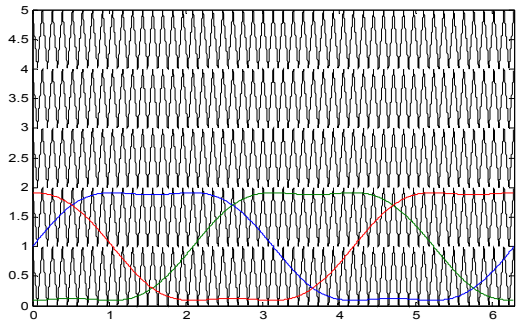

Fig.4c Reference sinusoidal signal set for 3-level operation in the proposed SPWM

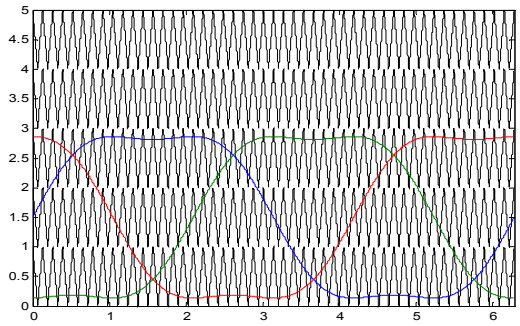

Fig.4d. Reference sinusoidal signal set for 4-level operation in the proposed SPWM

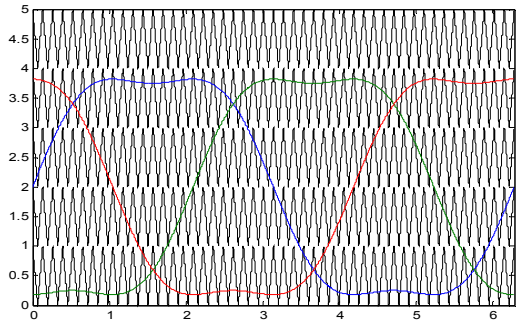

Fig.4e. Reference sinusoidal signal set for 5-level operation in the proposed SPWM

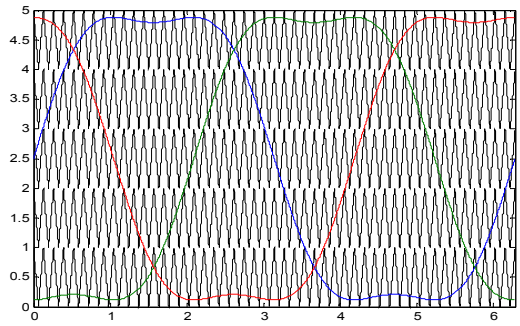

Fig.4f. Reference sinusoidal signal set for 6-level operation in the proposed SPWM

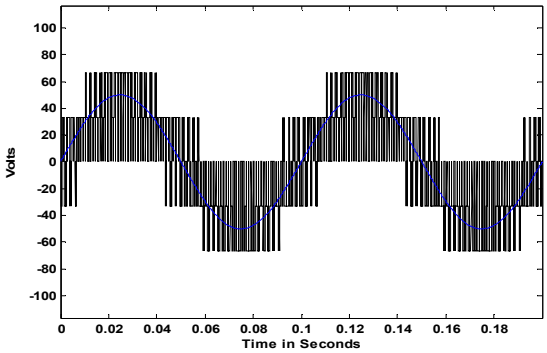

Fig.5a. Motor phase voltage during 2-level operation

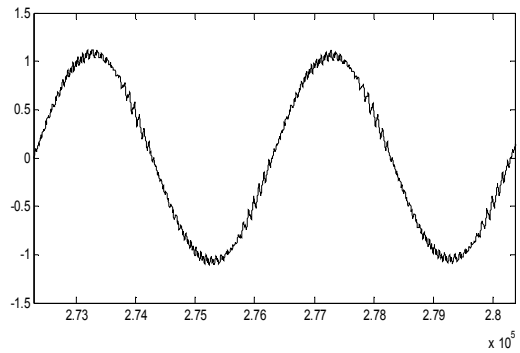

Fig.5b.Motor phase current during 2-level operation

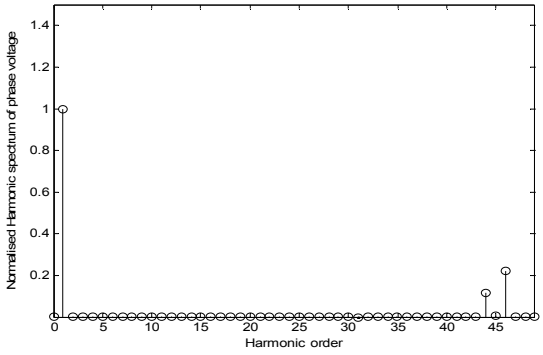

Fig.5c.Normalized harmonic spectrum of the motor phase voltage during 2-level operation

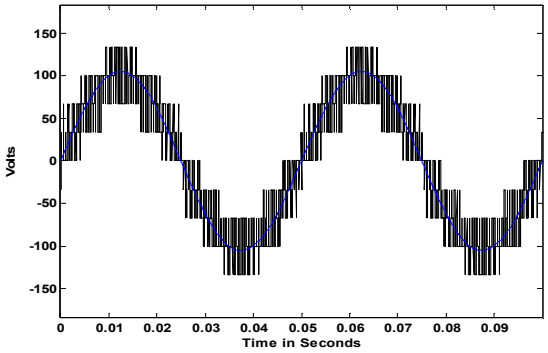

Fig.6a. Motor phase voltage during 3-level operation

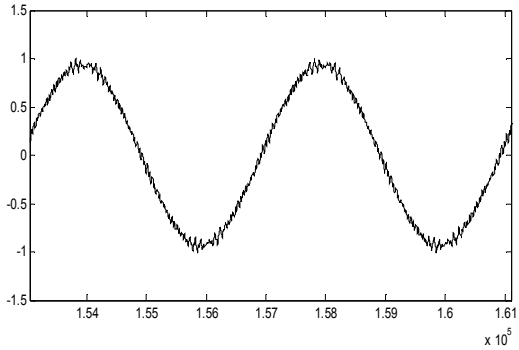

Fig.6b.Motor phase current during 3-level operation

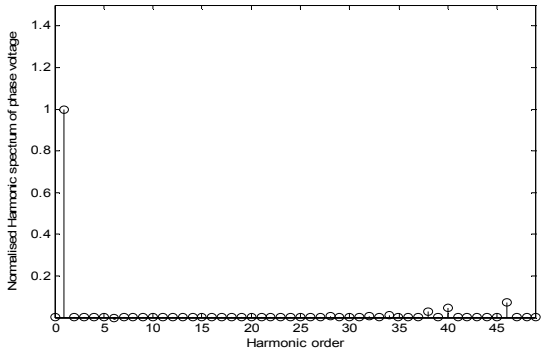

Fig.6c.Normalized harmonic spectrum of the motor phase voltage during 3-level operation

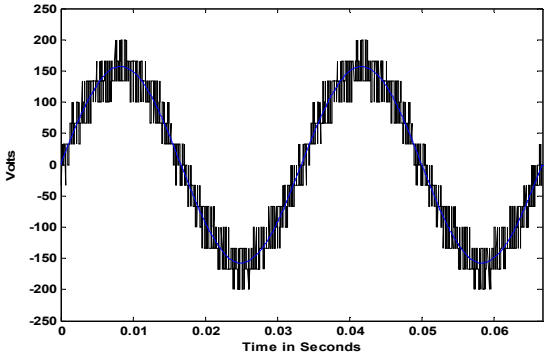

Fig.7a. Motor phase voltage during 4-level operation

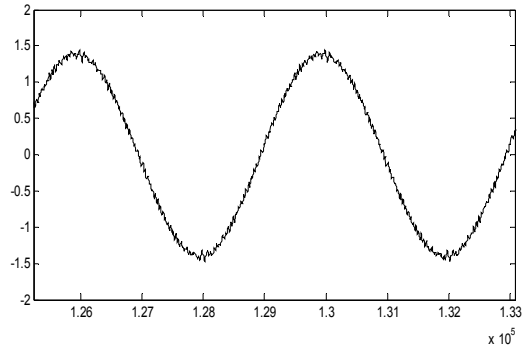

Fig.7b.Motor phase current during 4-level operation

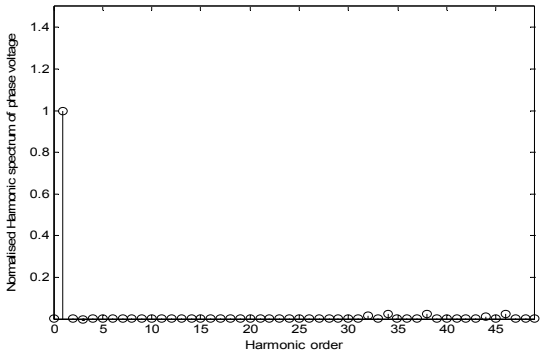

Fig.7c.Normalized harmonic spectrum of the motor phase voltage during 4-level operation

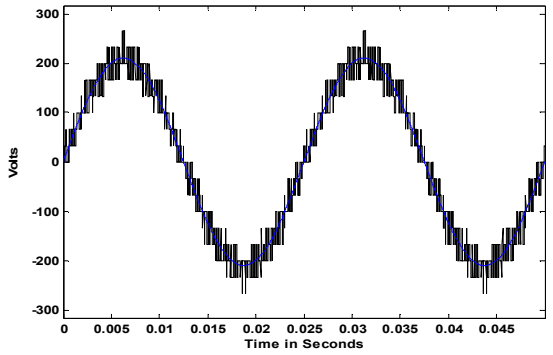

Fig.8a. Motor phase voltage during 5-level operation

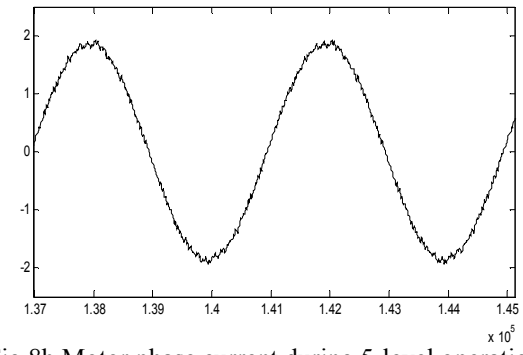

Fig.8b.Motor phase current during 5-level operation

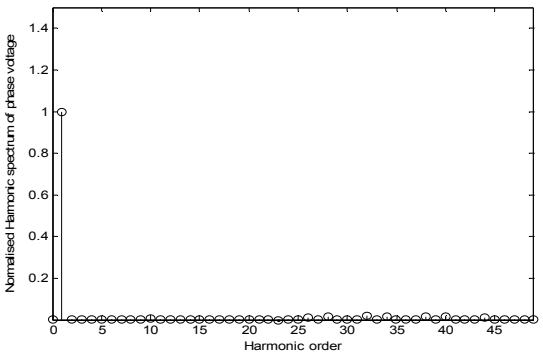

Fig.8c.Normalized harmonic spectrum of the motor phase voltage during 5-level operation

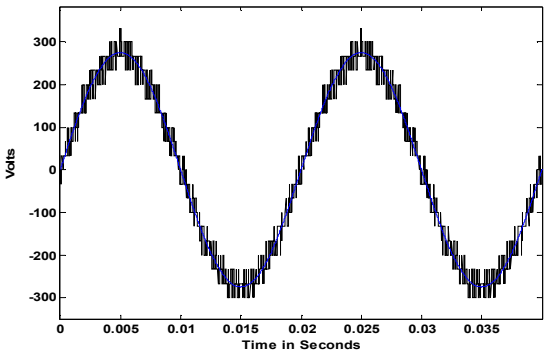

Fig.9a. Motor phase voltage during 6-level operation

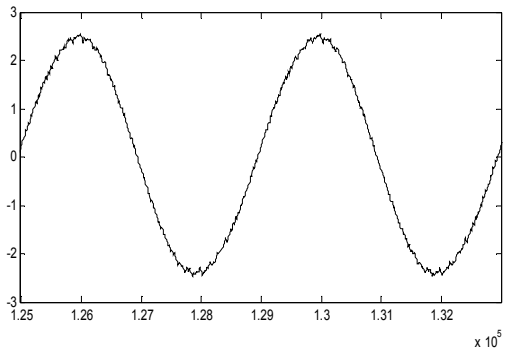

Fig.9b.Motor phase current during 6-level operation

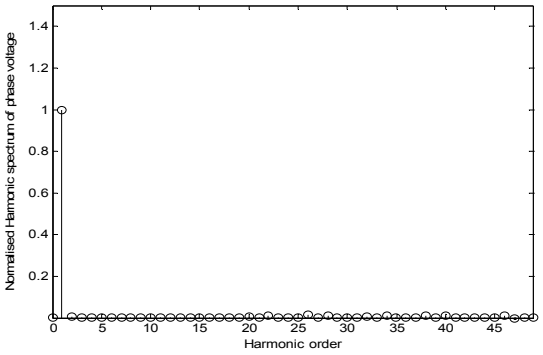

Fig.9c.Normalized harmonic spectrum of the motor phase voltage during 6-level operation

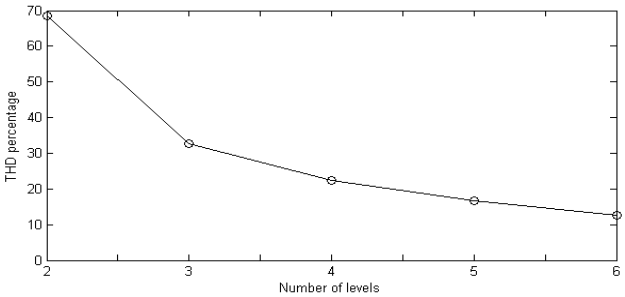

Fig.10. Total harmonic distortion (%THD) as the number of levels increased

7. Conclusion

A dual-fed induction motor drive, where the induction motor is fed by an asymmetrical three-level inverter from one end and a symmetrical three-level inverter from other end, generates voltage space vectors identical to a conventional six-level inverter. The asymmetrical three-level inverter used is composed of two conventional two-level inverters with unequal DC link voltage in cascade and the symmetrical three-level inverter used is composed of two conventional two-level inverters with equal DC link voltage in cascade. Comparing with conventional series H-bridge topology, the present topology needs a less number of power supplies. The proposed inverter does not experience neutral-point fluctuations and the DC link capacitors carry only the ripple current. Multilevel carrier based SPWM, where a progressive discrete DC shift is added to reference wave depending on the speed range, allowing operation in all levels (2-level to 6-level) is employed for the proposed work. This multilevel carrier based SPWM eliminates the use of look-up table approach to switch the appropriate space vector combination as in Space Vector Modulation scheme. In the lower speed ranges, one of the inverters is operating while the other inverter is not operated. The phase voltage of six-level operation contains lower harmonics when compared to that of two-level to five-level operation. As the number of levels increased the %THD in the motor phase voltage decreased. This results in smooth running of motor and the performance of the motor can be improved.

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