Recent Advances in Silicon Carbide Device Based Power MOSFETs

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Abstract: *Silicon Carbide (SiC) has revolutionized the semiconductor power devices. It is a wide band gap semiconductor with an energy gap wider than 2eV and possesses extremely high power high voltage switching characteristics, high thermal, chemical and mechanical stability. The SiC wafers are available in 6H, 4H, 2H and 3C polytypes. Because of its wide band gap, the leakage current of SiC is many orders of magnitude lower than in Silicon. Also forward resistance of SiC power devices is approximately 200 times lower than conventional silicon devices. The breakdown voltage of SiC is 8-10 times higher than that of Silicon. In this paper DIMOSFET, UMOSFET and Lateral Power MOSFET are discussed along with their characteristics and applications. Different Crystal structures used for SiC are also highlighted in this paper.*

Key words: *Silicon Carbide, DIMOSFET, UMOSFET and Lateral MOSFET.*

1. Introduction

Silicon Carbide (SiC) has been recently given renewed attention as a potential material for the high power and high frequency applications requiring high temperature operations. Some of the possible applications of SiC as a material of power electronic devices are for advanced turbine engines, propulsion systems, automotive and aerospace electronics and applications requiring large radiation damage resistance. Properties such as large break down electric field strength and large saturated electron drift velocity, small dielectric constant, reasonably high electron mobility, and high thermal conductivity to make a SiC attractive for fabrication of power devices with reduced power losses and die sizes. High thermal conductivity and breakdown electric field also suggest that integration of devices made from SiC make possible higher packing densities and there by improvement in the current handling capability of these devices can be achieved. In spite of these advantages, research pertaining to SiC power devices and their practical application has been hampered by lack of reproducible techniques to grow semiconductor quality single crystal and epilayers. However, recent developments in the growth of mono crystalline thin films of SiC by chemical vapor deposition and significant advancement in the growth of 6H-SiC single crystal boules, has stimulated a renewed interest in the SiC devices for a wide gamut of high temperature and high power device applications. Developments in the areas of the growth of the large area SiC bulk single crystal of 6H-SiC, improvement in the quality of SiC epilayers on Si and 6H-SiC substrates, high temperature ion implantation and doping of p and n types dopant, thermal oxidation reactive ion etching, discovery of ohmic contact materials, study of the electrical properties of grown and the doped films and their dependence on the temperature and advancements in the characterization techniques of the CVD-grown SiC films have made fabrication of high voltage SiC power devices a realistic possibility in the near future.

Table1 gives the comparison of the electrical properties of SiC with other semiconductors viz. Si, GaN and GaAs. Thermal oxidation of SiC produces a layer of SiO_2 on the surface while the carbon atoms from the SiC form CO, which escapes as gas. Thus, it is possible to make all devices found in silicon IC technology in SiC, including high quality, stable MOS transistors and MOS integrated circuits. The examples of WBG semiconductors are: Gallium Nitride (GaN, E_G=3.4eV), Aluminum Nitride (AlN, E_G =6.2eV) and Silicon Carbide (SiC, E_G between 2.2 to 3.25 eV depending on the polytype used). It is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature. Finally, SiC is the only compound semiconductor, which can be thermally oxidized to form a high quality native oxide (SiO_2). Although Silicon Carbide offers substantial advantages over Silicon, it is still immature as a semiconductor material. The main limitations of the technology are in the area of crystal growth

The SiC lattice consists of alternating planes of silicon and carbon items, and the stacking sequence of these planes defines different polytypes of the material identified by the repeat distance of the stacking sequence (e.g. 3C,4H & 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electric electrical properties such as

band gap energy, electron mobility and critical field differ significantly between the polytypes [1-5].

There are a large number of possible crystal structures. These are 2H, 3C, 4H and 6H. But, the most important are 3C, 4H and 6H. These structures differ by band gap energy, carrier mobility and breakdown field. For example, the Energy Gaps are 2.2, 3.26 and 3.0 eV for 3C, 4H and 6H-SiC respectively.

In this paper Silicon Carbide Based Power MOSFET viz DIMOSFET, UMOSFET and Lateral Power MOSFET are discussed along with their characteristics, uses, structures and applications. Table2 give the performance details of commercially available silicon carbide based devices which are developed by Purdue Group, Cree Group, Rutgers/USCI and Denso Group.

2. Power MOSFET

Power switches can be considered as the heart of all power electronic systems. The increased power capabilities, ease of control and reduced costs of power switches have made power electronic systems affordable in large number of applications. The first power switches were thyristors and bipolar transistors. Thyristors were used in higher power systems because their ratings were scaled at faster pace than bipolar transistors. Bipolar transistors were favored for low and medium power applications because of their faster switching capability. The rating of these devices grew steadily until the late 1970s, the year in which the first power MOSFETs introduced. Since the introduction of the first power MOSFETs, Si power MOSFETs has been immensely improved and have become the dominant device technology since 1980s for many applications for many reasons. First, MOSFET has very high input impedance due to its MOS gate structure. Hence, it provides the simplest gate drive requirements. The creation of either inversion layers or accumulation layers under the MOS channel can be controlled using integrated circuits because small gate current that is required to charge and discharge the high input gate capacitance. Second, The MOSFET is majority carrier device hence there is no minority charge storage involved in its operation. This results in faster switching operation. Third, compared to bipolar transistors the MOSFETs has superior ruggedness and forward biased safe operating area which allows the elimination of snubber circuits for protection of the switch during operation in typical hard-switching applications. Fourth, as the majority carriers in silicon exhibits increasing resistivity with temperature, the thermal runaway behaviour is avoided in MOSFETs. MOSFET devices are formed as parallel combinations of many thousands of individual MOSFET cells to take advantage of thermal behaviour. Any device carry excess current will heat up and become more resistive, diverting current into parallel paths. Excessive loss still produces thermal failure in MOSFET, but there is no unstable runaway effect if the parasitic BJT does not act. Due to these excellent characteristics, it would be desirable to utilize power MOSFETs for high voltage/power electronic applications. However, the blocking voltage capability of the MOSFET is based upon the ratings of the reverse body diode of the drift region. This blocking voltage is determined in part by the distance from source to drain. High blocking voltage capability implies high resistance because of geometry, so there is trade off between low drift region resistance and diode voltage capability.

Comparison of the figure of merits of Si and SiC polytypes determined by various scientists is given in Table3. On the basis of Keyes' and Johnson's figures of merit, SiC has superior properties as compared to Si. They derived the figure of merit for high speed switches and high power discrete amplifiers. Figure of merit emphasizes the electrical and thermal properties of various semiconducting materials to evaluate their power handling capability. Baliga derived the two figures of merits. One figure of merit is for low frequency and other one is for high frequency as well as high-power unipolar switches. Silicon carbide based MOSFET can be used in high power application and hence MOSFETs require high breakdown voltage. The one – step field plate termination can enhance the breakdown voltage to 910Volts, embedded mesa termination can increase it to 1350Volts and the embedded mesa with step field plating can give a breakdown voltage of 1100Volts [6], however, 6H-SiC DIMOSFET's in practice have attained a maximum blocking voltage of 760Volts [7]. The specific on resistance of the drift region of the MOSFET can be significantly reduced by enhancing the inversion channel mobility using Pyrogenic Re-Oxidation Annealing [8] thereby reducing the power dissipation.

Power MOSFET can be classified under following heads: (i) Double Implanted or DIMOSFET (ii) UMOSFET (iii) Lateral or LDMOSFET

2.1 Double Implanted MOSFET

Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only by using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC. Here we will discuss double implanted MOS (DMOS) as shown in Figure 3.

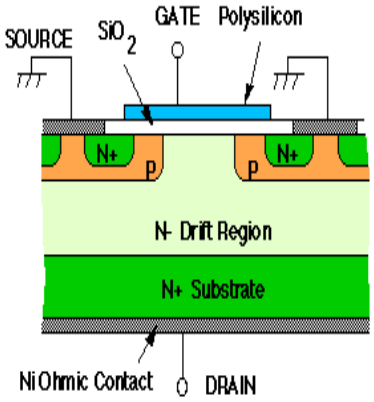

Fig.1. Double implanted MOSFET
(After J. N. Shenoy et al., Ref. 10)

DMOS transistors are common in silicon power device technology where the p-base and n^+ source regions are formed by diffusion of impurities through a common mask opening [9]. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n^+ source [9-13]. The implanted DMOSFET requires that separate masks be used to define the p-base and the n^+ source. The construction is a vertical structure with a drift layer built on a highly conductive n^+ layer. The n-drift region is designed to give the forward blocking capabilities. The forward blocking capability is achieved by the pn junction between p-base region and n-drift region. During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n^+- source region. By short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides. However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region. On applying the positive bias to the gate electrode, the conductive path between the n^+-source region and the n-drift region is formed. The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components. The total specific on-resistance [14] is determined as

$$R_{on\text{-}sp} = Rn^+ + R_C + R_A + R_J + R_D + R_S \qquad (1)$$

where $R_{on\text{-}sp}$ is the specific on-resistance, Rn^+ is the contribution from the n^+ -source, R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base regions by virtue of the JFET pinchoff action, R_D is the drift region resistance and R_S is the substrate resistance. In a power MOSFET, the blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n^+-source, the n-channel, the accumulation region and the n^+-substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating $R_{on\text{-}sp}$. However, at higher break down voltages, R_D is significantly higher than other resistances and Ron-sp can be approximated by R_D. The drift region analysis for an ideal DIMOSFET structure can be performed by taking the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor. The doping level N_B (cm^{-3}) required to support a given breakdown voltage V_B and the depletion width W (cm) [15] can be given by

$$N_B = \frac{\varepsilon E_C^2}{2qV_B} \qquad (1)$$

$$W = \frac{2V_B}{E_C} \qquad (2)$$

The specific on-resistance associated with the drift layer to support V_B [16] is given by

$$R_{on-sp} = \frac{W}{qN_B\mu_n} \qquad (3)$$

Substituting (1) and (2) in (3), we get

$$R_{on-sp} = \frac{4V_B^2}{\varepsilon E_C^3 \mu} \qquad (4)$$

where ε is the permittivity in F/cm, E_C is the breakdown field in V/cm, q is the electronic charge in C and μ_n is the electron mobility in cm^2/V-sec [17]. From the equations, it has been confirmed that both the mobility μ_n and breakdown field E_C depend on N_B.

The V-I characteristics of DIMOSFET are shown in Fig.2. SiC DIMOSFETs have been fabricated with the blocking voltage of 760V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength. By adjusting all

these parameters we propose to get the blocking voltage greater than 760V. The safe operating area of MOSFET is divided into three regions: (i) maximum permissible drain current, (ii) maximum power dissipation limit, and (iii) maximum drain source voltage limit. The safe operating area of MOSFET does not contain any second breakdown as seen in the BJT. This is because of the majority carriers present in the MOSFET.

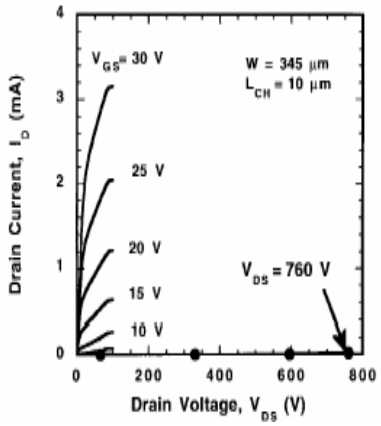

Fig.2. V-I characteristics of DIMOSFET
(After M. Bhatnagar and B. J. Baliga, Ref. 14)

2.2 UMOSFET

The UMOSFET is formed by reactive ion etching, the electrical fields at the bottom corners being lower than that at the tip of the V- groove MOSFET. The substrate acts as the drain electrode. It is lightly doped and thick, constituting the lightly doped drain to ensure a high blocking voltage. The p-type base layer is grown by epitaxy and is grounded. As shown in Fig.3, the UMOS forms the pn junction and the MOS channel. In the blocking state the gate is grounded, which turns the MOS channel off. The large drain voltage is supported by the reverse-biased junction and the MOS capacitor. The electric fields in the pn junction and the MOS capacitor are shown to the right of the figure. It has been observed that the electric field in the oxide at the trench bottom is 2.5 times higher than the peak field in the semiconductor. Such high fields may lead to the damage of the oxide before the pn junction breaks down. The field at the trench corners is even higher due to two-dimensional effects. Hence, in UMOSFETs the maximum blocking voltage depends on oxide breakdown and not on the semiconductor breakdown [18]. The maximum breakdown voltage provided by the device is 260V.

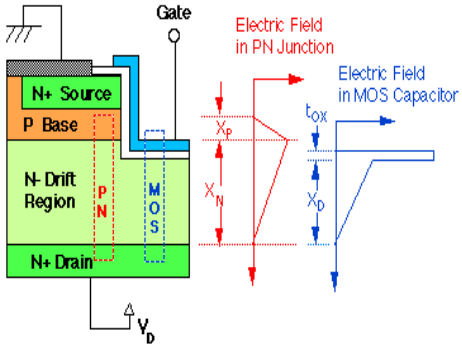

Fig. 3. Cross section of 4H-SiC UMOSFET
(After J.Tan et al., Ref. 18)

In order to overcome the limitation of the device a new UMOSFET with integral oxide protection has been developed, which limits the electric fields in the trench which simultaneously reduces the on-resistance. The structure is shown in Fig.4 with electric fields in the blocking state. A new p-region is formed at the bottom of the trench by ion-implantation and reduces the electric field at the oxide/semiconductor interface to zero. A new n-type layer (known as current spreading layer) grown epitaxilly between the n-drift region and the p-type base layer prevents the pinch-off of the conducting channel in the on state. The layer also facilitates lateral current flow into the drift region. Fig.5 shows V-I characteristics of IOP-UMOSFET. The features of IOP-UMOSFET are as follows: (a) The blocking voltage of the device is 1.4kV (b) The breakdown is nondestructive and the oxide failure does not occur (c) The specific on-resistance is 15.7 $m\Omega cm^2$ (d) The figure-of-merit V_B^2/R_{on-sp} is 125 MW/cm^2, the highest value ever reported for a power MOSFET in any material system and 25 times higher than the theoretical limit for silicon power MOSFETs.

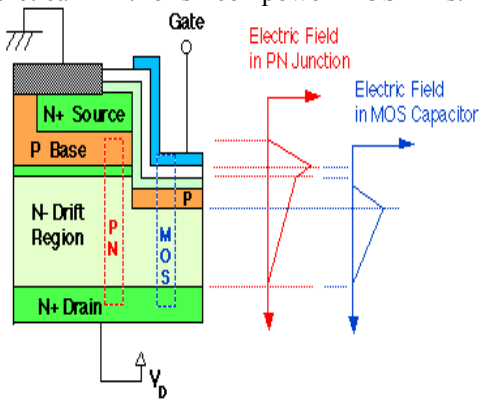

Fig.4 Cross section of 4H-SiC IOP-UMOSFET
(After J. Tan et al., Ref. 18)

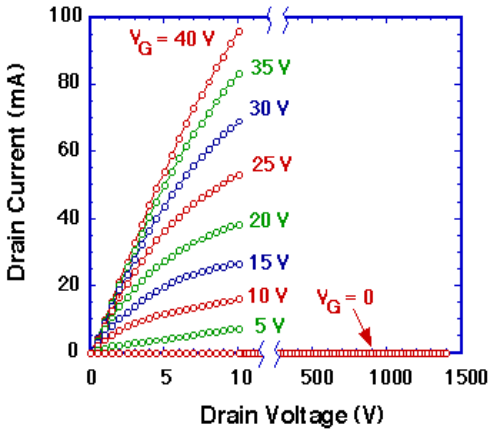

Fig.5 V-I Characteristics of IOP-UMOSFET
(After J. Tan et al., Ref. 18)

2.3 Lateral MOSFET

Before the advent of power devices of SiC, MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was blocked by a reverse-biased pn junction. In order to achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. In order to overcome the limitations of vertical-type MOSFETs we use the lateral-type MOSFET. The structure of lateral DMOSFET is as shown in Fig.6. From the figure it can been observed that the insulating substrate is of SiC [19]. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer. Fig.7 shows the current voltage characteristics of lateral DMOSFET. From the characteristics, it is observed that the device withstands a maximum drain voltage of 2.6 kV.

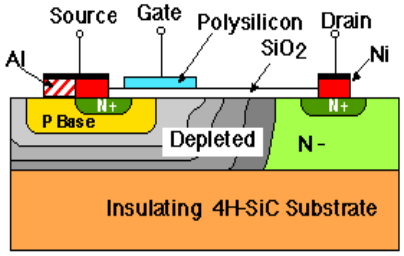

Fig.6 Cross section of lateral MOSFET
(After J. Spitz et al., Ref. 19)

From the above discussion we can say that the device should be implemented laterally rather than vertically because there is no necessity for an increase of surface area required for the device.

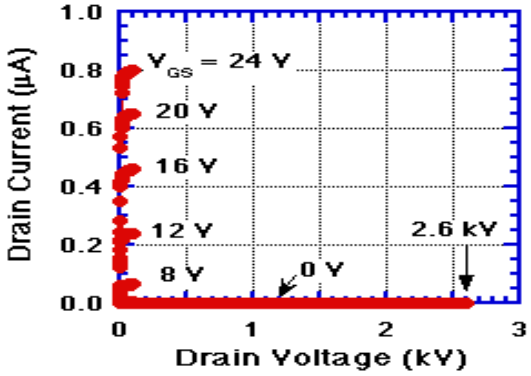

Fig.7 V-I Characteristics of lateral DMOSFET at room temperature (After J. Spitz et al., Ref. 19)

3. Status & Issues Regarding the Analysis Development of SiC Based MOSFETs:

In late 1980s, it was observed that power silicon devices were approaching their theoretical limits and that these limits could be significantly extended by fabricating power devices in the materials with higher breakdown electric fields, such as silicon carbide [20]. For vertically oriented majority carrier devices, the theoretical minimum value of the resistance-area product under punch- through condition is:

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_s E_C^3} \qquad (5)$$

where $R_{on\text{-}sp}$ is the specific on-resistance in Ωcm^2, μ_n is the electron mobility perpendicular to the surface, ϵ_s is the permittivity of the semiconductor, E_c is the critical field for avalanche breakdown perpendicular to the surface, and V_B is the designed blocking voltage of the drift region. Although it varies with doping, the critical field E_c in SiC is almost an order of magnitude higher than in silicon. Even allowing for the lower electron mobility, the specific resistance in SiC at a given blocking voltage is about 400 times than that in silicon.

In 1994 Silicon Carbide MOS characteristics had been explained. This paper produces data which for the first time characterizes the SiC/SiO2 interface and explains one of the previously unexplained abnormalities observed in the characteristics of SiC

MOSFETs. The outstanding distinction between the MOS characteristics on p and n type SiC wafers obviously indicates that the difference is probably caused by the fact that the p type wafers are Al doped and the n type wafers are N doped. The redistribution of impurities that occur during the thermal oxidation of SiC and Si, behaves in a similar fashion. N type dopants are rejected by the oxide during growth whereas p type dopants are incorporated into the oxide. Hence, the Al dopant in the oxide is likely to be the causes of the p type SiO_2/SiC interface characteristics [21].

The first MOSFETs in SiC were reported in late 1980s and the first power MOSFETs in 1994. The power devices were the vertical Trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs have been reported to have two serious problems: (a) A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage (b) The low inversion layer mobility along the trench sidewalls results in high specific on resistance which nullifies the advantage of low drift region in SiC. By 1995, UMOSFETs were fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

In 1996, the advantages and limitations of 4H-SiC Power UMOSFET Structure demonstrated by US Air Force (WPAFB, Dayton Ohio) and Office of Naval Research, Arlington, Virginia. In this paper, the use of p^+ polysilicon gate leads to higher breakdown voltage as the Fowler Nordheim injection from the gate electrode is reduced [22]. It is also concluded that the insulator reliability is the limiting factor and therefore the high temperature operation of these devices may not be practical.

In 1997, Denso Corporation Japan introduced UMOSFET. This UMOSFET produced the blocking voltage of 450V, specific resistance of 10.9 $m\Omega cm^2$ and $V_B^2/R_{on\text{-}sp}$ of 18.6 MW/cm^2 [23].

In 1997, Northrop Grumman Science and Technology Centre introduced and fabricated the 4H-SiC UMOSFETs at the blocking voltages of 1.1kV and 1.4 kV [23-24], as well as the 4H-SiC DIMOSFETs at a blocking voltage of 900V [25].

In 1998, Purdue University reported a SiC accumulation-channel UMOSFET with new structural features that shield the trench oxide from high electric fields in the blocking state . The new features consisted of p-type region formed in the trench bottom by self-aligned ion implantation and a thin n-type epilayer incorporated between the n-drift region and the p-type base [26-27].

A way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar implanted DMOSFETs. Since impurity diffusion is impractical in SiC, the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for the n^+ source. Because p-type implants are conducted at temperatures between1600 and 1700^{o}C, the self-aligned implant process using polysilicon gates is not practical in SiC. Hence, the realignment tolerances must be allowed between two sources and gate. This should also alter the alignment of the underlying base material. Due to these disadvantages, the elimination of the trench corners resulted in a threefold improvement in the device blocking voltage to 760V. This blocking voltage is achieved using 6H-SiC.

In 1998, the 4H-SiC UMOSFET was fabricated with a breakdown voltage of 1.4 kV and a specific on-resistance of 311 $m\Omega cm^2$ by the CREE Research Inc. The fabricated device required the impurity concentration of the drift region of $1x10^{15}/cm^3$ and required n^- thickness of 15µm. For the prototype module, three kinds of 2.0 kV UMOSFETs with different chip areas (0.7x0.7, 1.5x1.5, and 3.0x3.0 mm^2) were designed. All were fabricated in CREE Research Inc by using 4H-SiC wafers. In this report the relationship between the breakdown voltage and the specific on-resistance was presented by various groups which were involved in the fabrication of silicon carbide based power devices [27].

In 1999, the usefulness of silicon carbide for the device application was explained [28].

In 1999, the theoretical and numerical analysis of SiC JFET and MOSFET at 6.5 kV was presented.
To improve the on-state/breakdown performance of the JFET, buried layers in conjunction with a highly doped buffer layer have been used. Trench technology has been employed for the MOSFET. The devices are simulated and optimised using MEDICI simulator. In order to obtain a 6.5 kV breakdown voltage, the n-drift region length is 60µm long with a doping concentration of $2x10^{15}$ cm^{-3}. The distance between the

gate and the source diffusions is 0.6 μm. For a trench MOSFET, the p-well doping is $5x10^{17}$ cm^{-3} and its length is equal to 3.8 μm. The doping concentration of the n-drift region has to be decreased to $1.7x10^{15}$ cm^{-3}. In order to obtain the proposed breakdown voltage, the n-drift layer length is 60μm long. The gate oxide thickness for the simulated structure is 0.2μm [29].

In 1999, high-voltage lateral MOSFETs on 6H and 4H SiC wafers were fabricated with 400-475 V breakdown voltage using the RESURF principle. An MOS electron inversion layer mobility of about 50 Ω cm^2/V-sec was obtained on 6H-SiC wafers. This mobility is high enough such that the specific on-resistance of the 6H-SiC MOSFETs is limited by the resistance of the drift layer. The measured FET specific on-resistance R_{on-sp} ranges from 0.25 to 0.7750 Ωcm^2 depending on the device structure. However, this resistance is much higher than predicted because the sheet resistance of the drift layer is an order of magnitude higher than expected for the implant doses used. This paper also concluded that by redesigning the devices with appropriate drain edge terminations and by reducing gate overlap over the drift region, a substantial increase in breakdown voltage is expected [30].

In 2000, the characterisation of SiC epitaxial channel MOSFETs was demonstrated. Silicon carbide epitaxial channel MOSFETs were fabricated on 6H SiC substrates with N+ epitaxial source and drain electrodes. The electrical characteristics were modelled in the sub-pinch off depletion and accumulation modes of operation. A buried channel mobility of 230 cm^2/V-sec and an accumulation-mode surface mobility of 45 cm^2/V-sec were extracted at room temperature under a 50% activation of channel donor impurities [31].

In 2001, high-voltage lateral RESURF metal oxide semiconductor field effect transistors in 4H–SiC were experimentally demonstrated with a breakdown voltage of 900 V and a specific on-resistance of 0.5 Ωcm^2. Lighter RESURF doses and/or thicker gate oxides were required in SiC lateral MOSFETs to achieve highest breakdown voltage capability. In this paper, lateral RESURF MOSFETs were fabricated on p/p^+ 4H–SiC substrates with epitaxial thickness and doping of 10μm and $4\text{-}5x10^{15}$ cm^{-3} respectively. The source/drain regions were implanted with phosphorus to create a box profile of junction depth of 0.5μm and total dose of $5x10^{15}$ cm^2. The RESURF region was also realised with a box profile implant of the same junction depth with nitrogen as the dopant. The implants were activated at 1200 ^{0}C in argon ambient [32].

In 2001, a new 800V lateral MOSFET with dual conduction paths was presented and demonstrated. The feature of this new device was a buried P-type layer that divides the N-type drift region into two parallel conduction paths. The dual conduction paths provide an on-state resistance reduction of 33% as compared to a state-of-the-art double RESURF MOSFET. Charge balance is maintained among the layers to ensure high blocking voltage capability. The manufacturing process was relatively simple and provided excellent control of the charge in each layer by using ion implantation steps rather than epitaxial layers. A new BiCMOS Power IC process featuring this novel device was used to manufacture the cost-effective integrated power supply chips [33].

In 2001, a 4H-SiC RF power MOSFET was fabricated and characterised for the first time. The improved performance of this device was facilitated by a two-metal-layer process which optimises the conflicting requirements of the acceptable inversion-layer mobility and the low contact resistance. The cut-off frequency of the device with 1μm gate length was in excess of 7 GHz. The breakdown voltage of the newly fabricated MOSFET was found to scale with the drift length. A breakdown voltage of 950 V was achieved in MOSFETs with specific on-resistance of 24 Ωmm^2. The parasitic resistances were reasonably small due to dopant activation and post metallisation anneals. The sheet resistances of the N source/drain and N drift regions were measured to be 300 Ω/sq and 3400 Ω/sq respectively. The resistivity of the ohmic contact was $1.5x10^{-5}$ Ωcm^2 [34].

In 2002, a novel analytical model of a SiC MOSFET was presented. In this paper, by using known experimental results, a semi empirical relation for carrier mobility (μ) dependence on electric field intensity, dopant concentration and temperature was formulated. Based on this relation, appropriate analytical mathematical-physical model for simulation of current-voltage characteristics, transconductance and conductance of MOSFET were developed. All models were formulated taking into account, among other effects, the dependence of threshold voltage on temperature and impurity concentration in the channel, as well as the effect of the channel narrowing. Using the proposed model a simulation algorithm was designed and a simulation of the MOSFET's performance was performed [35].

In 2002, a 10 A, 2.4 kV power DIMOSFET in 4H-SiC was reported and the characteristics of large area (3.3x3.3 mm^2), high-voltage 4H-SiC DiMOSFETs

were demonstrated. The MOSFETs showed a peak MOS channel mobility of 22 cm^2/V-sec and a threshold voltage of 8.5V at room temperature. The DIMOSFETs exhibited an on-resistance of 42 $m\Omega cm^2$ at room temperature and 85 $m\Omega cm^2$ at 200 ºC. Stable avalanche characteristics at approximately 2.4 kV were observed. An on-current of 10 A was measured on a 0.103cm^2 device. High switching speed was also demonstrated. In this paper, the MOS channel length defined by the p-well and n implants was 1.5µm. Electrons flowed laterally from the n source through a MOS channel on the implanted p-well, then flowed vertically through the JFET region formed by two adjacent p-well regions and then through the lightly doped n drift region into the drain. The cell pitch was 16 µm and the packing density of the gate periphery was 1250 cm/cm^2. A 20-µm thick drift layer with a doping concentration of $2.5x10^{15}$ cm^{-3} was chosen for a 2000 V blocking voltage design. This paper also suggested that the devices are capable of high-voltage, high-frequency and low-loss switching applications [36].

In 2002, a two-zone, lateral RESURF field 6H-SiC MOSFET with a breakdown voltage as high as 1300 V and a specific on-resistance of 160 m Ωcm^2 was fabricated. These MOSFETs exhibited stable and reversible breakdown indicating an avalanche breakdown in SiC that had not been reported in earlier lateral SiC MOSFETs. In this paper, the device was fabricated on p/p^+ 6H-SiC wafers with epitaxial thickness and doping of 10µm and $7x10^{15}$ cm^{-3} respectively. The specific on-resistance of the MOSFET is lower than any lateral MOSFET reported in silicon or SiC with similar breakdown voltage [37].

In 2003 and 2004, numerical device simulations on a 4H –SiC vertical MOSFET were presented. The simulations mainly focused on reverse blocking voltage, threshold voltage and on-state resistance. The simulated gate MOSFET had a gate oxide thickness of 50nm, a source depth of 0.2 micron and a p-well depth of 1 micron. The channel length was of 1micron [38-39].

In 2004, a comparison of modern SiC power devices was demonstrated. In this paper an analysis of the static and dynamic behaviour of a 2 kV SiC MOSFET and IGBT was presented. By comparing the circuit performances it was observed that IGBT is two times faster than MOSFET [40].

In 2005, a design and fabrication of a 1600V 4H-SiC UMOSFET with a dual buffer layer structure was demonstrated. The fabricated device exhibited 50$m\Omega cm^2$ of specific on-resistance with ~1µm of the channel length that could be further reduced to <1µm. In this paper, the n-type drift layer was ~25µm thick with $3\text{-}5x10^{15}$ cm^{-3} of doping concentration. Two n-type buffer layers were grown on top of the drift layer. The first buffer layer was ~3µm thick and $1\text{-}2x10^{16}$ cm^{-3} doped with nitrogen. The second layer was ~0.5µm thick, $0.5\text{-}1x10^{17}$ cm^{-3} doped with nitrogen followed by the final p-type, ~2µm thick base layer with $0.8\text{-}1x10^{17}$ cm^{-3} doped with aluminum. The N^+ layer was formed by high energy up to 700 KeV nitrogen implantations to obtain ~1µm channel length. UMOSFET trench gates were perpendicular to the primary flat of the SiC wafers to achieve high inversion channel mobility [41].

In 2005, an on-state performance of trench oxide-protected SiC UMOSFETs on 115µ m-thick n-type 4H-SiC epilayers designed for blocking voltages up to 14 kV was demonstrated. In this paper, a current density of 137A/cm^2 and a specific on-resistance of 228 $m\Omega cm^2$ were achieved at a gate bias of 40 V. The effect of current spreading on the specific on-resistance for finite-dimension devices was investigated. A 115µm-thick, $7.5x10^{14}$ cm^{-3} n-type epilayer was first grown on n^+ 4H-SiC substrate, cut 8^o off axis and followed by a 0.4 µm, $2x10^{17}$ cm^{-3} n-type current spreading epilayer and a 1.5 µm, $2x10^{17}$ cm^{-3} p-type epilayer to form the base region of the UMOSFET. Source contacts were formed by implanting $4x10^{15}$ cm^{-2} nitrogen at 650 ºC using a Ti-Au mask. Gate trenches approximately 2 µm deep were formed by reactive ion etching using a Ni mask. Sacrificial oxidations were performed to smooth the trench sidewalls. The active area of the device was .018cm^2 and required a current 2.5 A. The device required a current density of 137A/cm^2. The blocking layers of doping and the thickness used here were theoretically capable of blocking 14 kV and had actually been demonstrated to block 10 kV. However, problems with the edge terminations in the devices limited the blocking voltage to just over 5 kV [42].

In 2005, a 1330 V, 67$m\Omega cm^2$ 4H-SiC RESURF lateral MOSFET was investigated. The figure of merit of the presented device was 26 MW/cm^2. This figure of the merit was the best among the reported lateral MOSFETs [43].

In 2006, 4H-SiC DMOSFETs of breakdown voltages of 1.2 kV and 1.8 kV were fabricated [61]. For 1.2 kV, an epilayer with a doping concentration of $6x10^{15}$ cm^{-3} and a thickness of 12 µm could be used. For 1.8 kV 4H SiC DMOSFET the device had a gate oxide of 500Å. The gate oxide electric field was limited to approximately 3 MV/cm. The active area of

this device was 0.0936 cm^2. An on-resistance of 85 mΩ (R_{on-sp} = 8 mΩcm^2) and a drain current of 50 A (534 A/cm^2) at a forward drop of 5.7 V were measured at room temperature [44].

In 2006, silicon carbide as energy efficient wide band gap devices was discussed. For RF applications, GaN HEMTs allowed the use of highly efficient Class E circuit topologies demonstrating a high power of 63 W at 2 GHz with 75% power added efficiency. SiC Schottky diodes were allowing up to a 25% reduction in losses in power supplies for computers and servers when used in the power factor correction circuit. Even higher efficiencies could be obtained when the SiC Schottkys were combined with a SiC MOSFET as the switch, resulting in yet another 22% reduction in losses. For motor control, SiC Schottky allowed a >35% reduction in losses as demonstrated for a 3 HP motor drive [45].

In 2007, a compact circuit simulator model was developed and used to describe the performance of a 2kV 4H SiC power DIMOSFET. This model [46] also made a comparison with the widely used 400V, 5A Si power MOSFET. The model's channel current expressions are unique in that they include the channel regions at the corners of square and hexagonal cells that turn on at lower gate voltages and the enhanced linear region transconductance. This model also actively describes the static and dynamic performance of both the Si and SiC devices. In this paper the detailed device comparisons show that both the on-state performance and switching performance at 25 °C are similar between the 400V Si and 2kV SiC MOSFETs with a difference that the SiC device requires twice the gate drive voltage. The main difference between the devices is that the SiC has a five times higher voltage rating without an increase in the specific on-resistance.

In 2008,it has been analyzed the device structure of a 6H-SiC vertical double-implanted MOSFET (DIMOSFET) in order to provide a high breakdown voltage of about 10 kV and a low power dissipation for a rise in device temperature of 600 ˚C. Analysis of 800 W power dissipation for stable device operation corresponding to this temperature rise shows optimum doping levels of the drift region lying between $5*10^{13}$ cm^{-3} and $5*10^{15}$ cm^{-3} for a breakdown voltage of 10 kV [47].

4. Conclusion

At present SiC devices appear to compete in the semiconductor market as high voltage high power switching devices. In this paper we estimate that SiC can be used as a power device for the large breakdown voltages, low specific on resistance and optimal value of power dissipation. It can also be used in the development of the nonvolatile memories. It has also been examined that SiC devices can be used as static induction transistor that can be operated at microwave frequencies. However, in order to become economically feasible, several critical materials and processing issues still need to be solved.

Table 1 Comparison of electronic properties of SiC with Si, GaAs and GaN

	Si	**GaAs**	**GaN**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field @ $10^{17}cm^{-3}$(MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron mobility @$10^{16}cm^{-3}$ (cm^2/V-sec)	1100	6000	1000	370	800	750
Hole mobility @$10^{16}cm^{-3}$ (cm^2/V-sec)	420	320	200	90	115	40
Saturated electron drift velocity (cm/sec)	10^7	10^7	$2.5x10^7$	$2x10^7$	$2x10^7$	$2.x10^7$
Intrinsic concentration, n_i (cm^{-3})	$1.5x10^{10}$	$1.9x\ 10^{-10}$	$2.1x10^6$	$2.3x\ 10^{-6}$	$8.2x\ 10^{-9}$	6.9
Thermal conductivity	1.5	0.55	1.3	4.9	4.9	5

(After R. Y. Lakhshman, MS Thesis, Mississippi State University, 2001, Ref. 8)

Table 2 The best-reported SiC based power MOSFETS fabricated and tested by different groups

MOSFETs					
Sr. No.	**Fabricated Device**	**Blocking Voltage (KV)**	**Specific on resistance $m\Omega cm^2$**	**Figure of merit (MW/cm^2)**	**Device Fabricated By**
1	DMOSFET (6H)	.760	125	4.62	Purdue Group (1996)
2	DMOSFET	.350	18	6.81	NCSU (1997)
3	DMOSFET (4H)	2.4	42	137	Cree, Inc.
4	UMOSFET	1.41	275	7.2	Cree Group (1997)
5	IOP-UMOSFET (4H)	1.4	15.7	125	Purdue Group (1998)
6	UMOSAFET	.45	10.9	18.6	Denso Group (1997)

Table3 Comparison of figures of merits SiC with Si

Figure of Merits	**Si**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Johnson's FOM	1	400	400	280
Keyes' FOM	1	5.1	5.1	5.8
Baliga FOM (Low Frequency)	1	240	560	140
Baliga FOM (High Frequency)	1	29	69	25

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