COMPARATIVE ANALYSIS OF POWER BY INCORPORATING FLIPFLOPS IN PID CONTROLLER

Er. V.P. Krishnammal[1] **Dr. V. Vijaya Kumari[2]** **Dr. M.C. Jobin Christ[3]**

[1]Department of Biomedical Engineering, Adhiyamaan College of Engineering, Hosur, India.
[2]Department of Electronics and Communication Engineering, Er.Perumal Manimekalai College of Engineering, Hosur, India
[3]Department of Biomedical Engineering, Rajalakshmi Engineering College, Chennai, India
krishnavelappan@gmail.com[1] , ebinviji@rediffmail.com[2] & jobinchrist.mc@rajalakshmi.edu.in[3]

Abstract: *Proportional-Integral-Derivative (PID) control is widely used in industries such as chemical, petrochemical, robotics etc, since this control algorithm has been universally accepted in most of the industrial control. There are many factors that makes PID controller most popular, such as its low cost, easy maintenance and its robustness in a large range of operating condition. Razor flip-flops are incorporated to improvise the PID's performance, by detecting and correcting the timing errors on critical path. A novelty has been introduced in the proposed methodology, which involves a Flip Flop called Razor Clock Gated Flip Flop (RCGFF) by using Pulse-Triggered Flip-Flop. This proposed outlook reduces the timing error and improves the integrated sequential circuits' robustness. RCGFF has been used to achieve high-precision, high-speed, power reduction in static and average power consumption in PID controller. This procedure is appropriate for low power and data communication in PID controller. The proposed RCGFF is associated with preceding work such as Semi-Dynamic Flip-Flop (SDFF), Dynamic Data Flip-Flop (DDFF), Hybrid Latch Flip-Flop (HLFF) and Clocked CMOS Flip-Flop (CCMOS) in terms of attributes like power consumption, Power Delay Product (PDP), time delay and area. Results are authenticated by simulations, the proposed method achieves 74% of power reduction comparing to conventional existing design, by means of IBM 130 nm with 1.8 supply voltage.*

Keywords: *Flip Flops, Proportional-Integral-Derivative (PID) controller, Pulse-Triggered Flip-Flop, Razor, Timing error.*

1. Introduction

In the process control industries, PIDs are most often used controllers [1]. The main reason for PID being used is its extraordinary efficiency, comparatively justifiable structure and simplicity of execution in training by process and control engineers [2]. For the last two decades, many efficient blocks like Operational Transconductance Amplifiers (OTAs) [3-4], Current Feedback op-Amp (CFAs) [5-6], second generation Current Conveyors (CCIIs) [7], second generation Current Controlled Current Conveyors (CCCIIs), and Current Differencing Buffered Amplifiers (CDBAs) [8], are the various high performance active building scenario of PIDs, which makes PIDs to have a significant attention in various industries.

The PID controller is a type of feedback controller that is the possibly the most widely-used controller [9]. PID stands for Proportional-Integral Derivative, denoting to the three terms functioning on the error signal to yield a control signal. By making an alteration in the three parameters of PID controller algorithm, the controller can afford control action intended for precise process entities. The reaction of the controller to an error, the degree to which the controller overreaches the set point, and the degree of system fluctuation determines the response of the controller. To obtain the output by ADC, the system process which is an analog signal is used. In this, both ADC and DAC are acquainted with the error, delay, and data loss. The unnecessary delays in the program execution has been caused by the timing error. There are many factors that cause timing error, such as scaling in CMOS technology, rise of process variations, minimization of power supply and modern ICs complexity. Among various error detection and correction techniques, razor flip-flops-based error detection scheme is an effective method for detecting timing errors. In this system, timing-error detecting flip-flop is introduced to critical paths across the design, and these are later used to sense the on-set of timing errors while ascending supply voltage.

Figure 1 illustrates the closed-loop control outline predictably used for Razor Dynamic Voltage Scaling (DVS). A Single error bit has been generated while detecting late transitions at the end points of the critical path by Razor flip-flops (RFFs). A global error bit flag,

$e[n]$ has been obtained by combining the foresaid error bit with a wide OR gate. A counter is used to assimilate $e[n]$ over N cycles and results in an error rate, $e'[n]$, which is related with the target error rate set point, r $[n]$, before adjusting the supply voltage using the supply voltage control variable, $u[n]$, which signifies the new supply voltage request. To generate a scalable supply voltage, a power management unit, which can either be a separate IC or integrated on chip has been used. Thus, Razor Clock gated Flip Flop (R- CGFF) has been used in the proposed system to reduce the timing error in every bit and maximises the power reduction in the controller system incorporating PID.

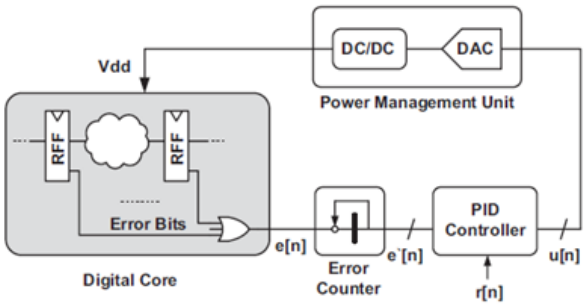

Figure 1: Timing-error rate feedback incorporated in Closed-loop DVS

2. Razor based flip flop design

Razor flip-flop is mostly used to detect and correct the timing errors on critical path and to deliberately operate the circuit at sub-critical voltage and adjust the operating voltage by considering the error rate [13]. This removes the necessity for conservative voltage margins. It comprises of main flip-flop and shadow flip-flop which is under the control of delayed clock, as depicted in Figure 2. Timing errors can be perceived by associating the data from the main flip-flop with shadow flip-flop [14-15]. If an error is sensed, it is revised by reinstating the data from the shadow latch to the main flip-flop. It permits the timing guard band to be disregarded or to be abridged. Timing errors are noticed and modified by on-chip circuits when they arise. All the flip-flops must be replaced by RFFs, if any flip-flop in a stage attains a signal with critical path delay. In the applications of high-speed operations, razor Pulse-triggered FF (P-FF) has been considered as a widespread substitute to the conventional master-slave- based FF. In Razor FF, P-FF design has been classified into implicit (pulse generated are built in the latch) or explicit (pulse generated externally to latch). The power efficiency of the implicit type is comparatively higher. Thus, the Razor FF uses conventional Implicit-Type P-FF. Flip Flops like SDFF (Semi-Dynamic Flip-Flop), HLFF (Hybrid Latch Flip-Flop), DDFF (Dynamic data Flip-flop) and CCMOS (Clocked CMOS Flip-Flop) are mainly used.

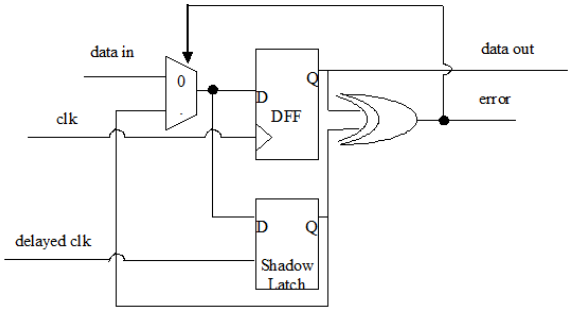

Figure 2: Design of a Razor Flip-flop

2.1 Semi-Dynamic Flip-Flop (SDFF)

Semi-Dynamic Flip-Flops (SDFF) have many unique characterises like small delay, logic embedding feature and simple topology thus; these FFs are used in high performance applications[16]. It is called semi-dynamic because it is constructed with dynamic input stage with static operation. The operation of the circuit is well-defined with pre-charge and the evaluation section. The flip-flop enters the pre-charge phase, when the edge of the clock falls. The flip-flop enters the evaluation phase, when the edge of the clock rises.

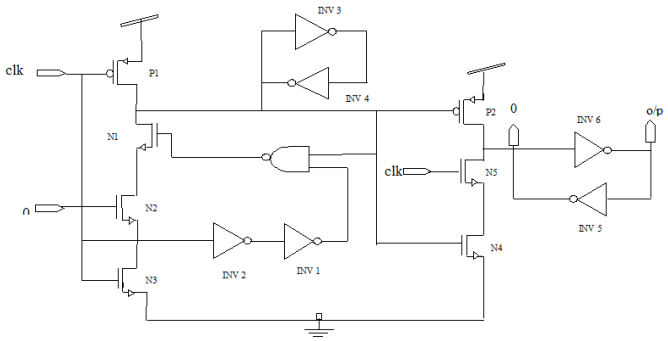

Figure 3: Design of Semi-Dynamic Flip-Flops (SDFF)

As depicted in Figure 3, CLK signal acts as an input to P1, N3 and INV2. Thus, INV1 and INV2 generate the pulse delay, which is fed as an input to the conational NAND gate. N3 will be turned ON when clock edge rises. When data remains low, N3 node will be discharged and the switching activity of transistor leads to more power dissipation.

2.2 Hybrid Latch Flip-Flop (HLFF)

HLFF samples the data on one edge of the Clock and removes the delay of data flow on the reverse edge[17]. The latch latency and clock load are reduced by

incorporating HLFF in a system. The basic operation of HLFF involves, delivering soft clock edge which permits for the stack passing and diminishing the effects of clock skew on cycle time, thus its operation is like a latch operation. This cycle time is determined by an integrated one-shot consequent from the clock edge.

As depicted in the Figure 4, Delay clock signal is originated by inverters INV1-INV3. With respect to the pull-up transistor (P3- with the gated input clock signal), the flip-flop output signal Q is sustained high. During the data transition ("0" to "1"), Q node is not pre-discharged. Discharging capability has been enhanced by using larger transistors N1 and N4.

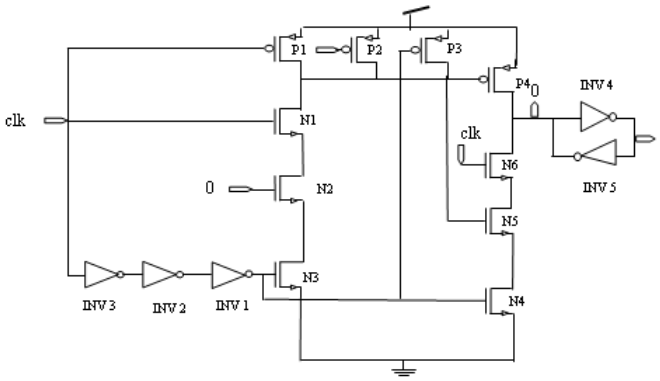

Figure 4: Design of Hybrid Latch Flip-Flop (HLFF)

2.3 Dynamic Data Flip-Flop (DDFF)

Figure 5 depicts the design of DDFF by Keeper logic method. The feedback inverter is weak pull up in PMOS2 and NMOS 2 are associated to the load capacitance to keeper logic gate, thus there is no voltage swing discharge and no properly pull-down. The foresaid scenario ensures the need of extra circuitry.

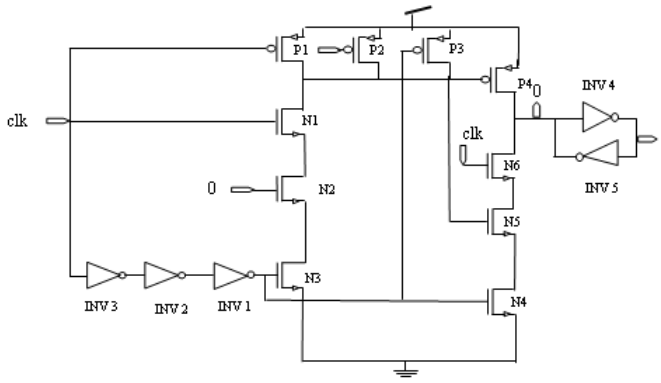

Figure 5: Design of Dynamic Data Flip-Flop (DDFF)

2.4 Clocked CMOS Flip-Flop (CCMOS)

Clocked CMOS was proposed to overcome the downside of the data float in keeper logic at node INV1 and INV2. The pull-up and pull-down networks' data input controls the voltage scaling of CCMOS. The data path voltage is controlled by clock and clock bar inputs. In the drain node of PMOS2 and NMOS2 the strong pull-down and pull up network has been feed backed. In the pull-down network, NMOS6 and PMOS5 has voltage swing, which are controlled with respect to the I1. With respect to clock and clock bar, swing voltage are pull down in the transistors NMOS9 and PMOS5. The foresaid scenario implies the durable discharging in load capacitance at the drain node of N9 and P5. To ensure datapath in a pull up network, proper voltage scaling has been controlled by P1 and N4 with respect to gated input I1. The clock controls the P4 and N1 and it confirms the powerful pull-down, with respect to the widening of I2 and I3 inverters. Thus extended delay from I1 to I3 pulse width are appropriately discharges in load capacitance.

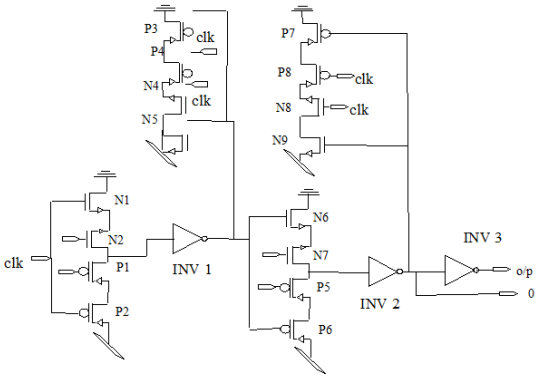

Figure 6: Circuitry of Clocked CMOS Flip-Flop (CCMOS)

Clocked CMOS circuits, which implement progressively rising and falling power-clock, which results in a significant energy saving. The circuit design is tedious because the demand that the output signal should pathway the power-clock's progressively rising and falling behaviour throughout charging and discharging.

3. Novel Razor CGFF with PID controller

The novelty introduced in the proposed work is the implementation of Razor Clock Gated Flip Flop (RCGFF) by using Pulse-Triggered Flip-Flop. Thus, the foresaid scenario reduces the PID controller's timing error.

3.1 Error detection and correction

To detect the error signal in circuit level, the delay clock signal is prearranged to shadow flip-flop. If the combinational logic encounters the setup time of the main flip-flop, then the main and delayed flip-flops will latch the similar value. Thus, the error signal retains its level as low. If the setup time is not met by the main flip-flop, then it will latch a value that is diverse from the shadow flip-flop. To assurance that the shadow flip-flop continuously latches the input data properly, the input voltage is controlled such that under the worst-case scenario, the logic delay does not overdo the setup time of shadow flip-flop. RCGFF has enormous pull down in each stage of data compared to DDFF. Thus the node expulsion in RCGFF has enormous pull down in each stage of data,

this preserves the low switching movement of transistor and low noise capacitance discharge.

In pipeline stage, well-organized error detection and correction miscarries in critical path delay. Shadow Flip-flop meets the main flip-flop at rising or falling edge thus, it meets the foresaid clock delay, finally the data remains the same in both flip-flops. If XOR gate fan out is low, then error signal occurs, and it is altered by shadow flip-flop until XOR gate fan out are high, as depicted in figure 7.

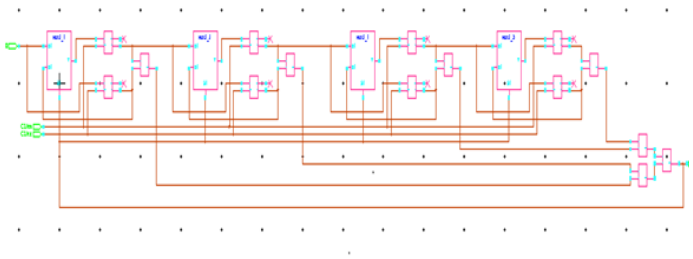

Figure 7: Novelty in the Proposed Razor CGFF

The timing error is corrected by implementing the PID controller with Razor system. Design of Proportional Integral Derivative (PID) controllers has established a great deal of consideration in the fields of control systems. The main advantage of PID is that; it is simple, cheap and ease in parameters tuning. The design of PID controller using Current Conveyor Transconductance Amplifier (CCTA) consists of capacitors and resistors to match the input voltage as shown in figure 8. Based on Ib1, Ib2 and Ib3 bias current it may work as P, PI, PD and PID as shown in table 1.

Table. 1 PID Programming

Ib1	Ib2	Ib3	controller
1	0	0	P
0	1	0	I
0	0	1	D
1	1	0	PI
1	0	1	PD
0	1	1	ID
1	1	1	PID

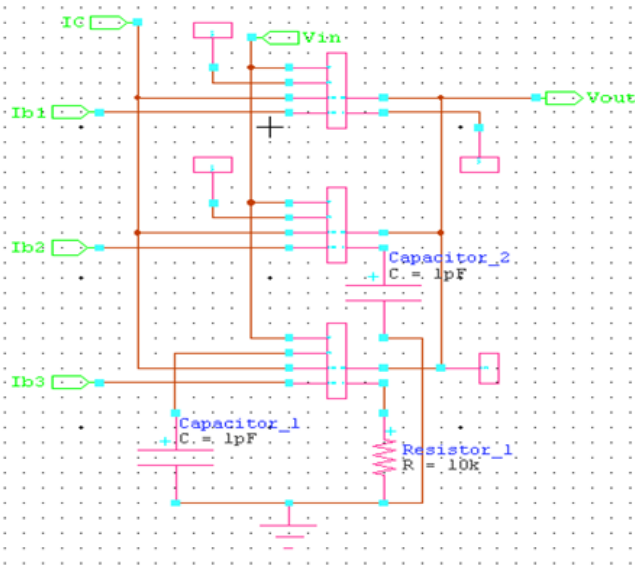

Figure 8: Design of PID controller

Razor implementation in PID as depicted in figure 9. It comprises of DVS, Razor FF and PID. To obtain data loss system, functioning of Razor relates the data in M-FF and S-FF with reference to the clock signals Clkm (main FF clock) and Clks (shadow FF clock). Delay signal given to razor flipflop is Clks. In Razor, both flip-flops attains the same value. Consecutively data is conceded to the PID controller. If the value is different then, shadow FF will precise the value, with respect to clock delay signal. Based on Ib1, Ib2, Ib3 and VIN PID will produce the signal, which manages the feedback to the DAC. Feedback signal fed to the DAC is a nonlinear signal. Input voltage scaling down in DVS will be again looped back to razor. This process will be repeated until feedback becomes linear. The schematic diagram of Razor implementation in PID controller is depicted in figure 9.

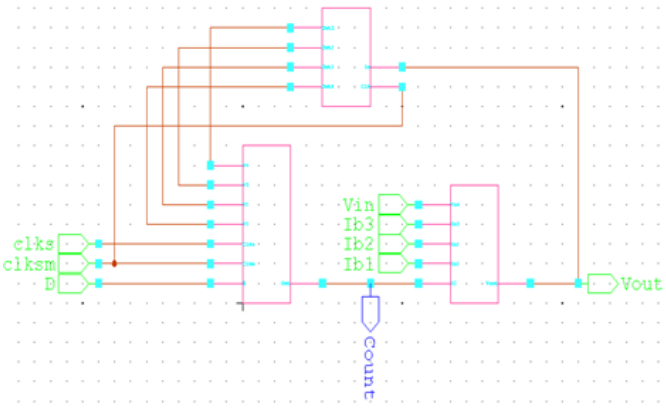

Figure 9: Schematic diagram of Razor implementation in PID controller

4. Experimental Results

Tanner EDA tool using 130nm CMOS parameters has been used for the simulations. The proposed RCGFF has been compared with preceding work such as SDFF,

HLFF and Clocked CMOS with respect to varies parameters, such as power consumption, Power Delay Product (PDP), time delay and area. Both convention and proposed Flip-flop designs are tested in data driving and clock drive. Estimation of the data power has been done with respect to the load. Total power is well-defined as the summation of data driving power, the clock driving power and internal power. The simulation parameters are signified in table 2.

Table 2: Simulation Parameters

Device Technology	130nm CMOS technology
C1 , C2	100 pF
VDD	1.2 V
-VSS	1.2 V
Ib1	55 µA
Ib2	24 µA
Ib3	30 µA
KP	1
TI	0.43u10-6 s
TD	1u10-6 s

The simulated frequency responses of PI controller have been analysed under two circumstance such as, when the digital signals were Ib1= 1, Ib2 = 1, Ib3 = 0 and PD controller have been analysed under when the digital signals were Ib1 = 1, Ib2 = 0, Ib3 = 1.

The simulated frequency and phase responses of the proposed PID controller have also been analysed when the digital signals were Ib1 = 1, Ib2 = 1, Ib3 =1.

For logic 1, CCTA used 20 µA for Ib1, Ib2 and Ib3. For logic 0, CCTA used 0A for Ib1, Ib2 and Ib3.
Table 3 depicts the comparison of conventional Flip flops and CCMOS design.

Table 3 .Comparison of Flip-flops in Pulse mode

Parameter	Data Driving (mw)		
	With load	Without load	Data power
SDFF	1.5239	1.0531	0.4708
HLFF	0.12897	0.0000584	0.1289116
DDFF	0.665337	0.22518	0.440157
C^{2}MOS	0.893957	0.87077	0.023187
Parameter	**Clock Driving (mw)**		
	With load	**Without load**	**Data power**
SDFF	1.5239	0.7589	0.765
HLFF	0.12897	0.00001316	0.1289568
DDFF	0.665337	0.559771	0.105566
C^{2}MOS	0.893957	0.87077	0.023187

Parameter	Internal power (mw)	Total Power (mw)
SDFF	3.811	5.6291
HLFF	4.6	4.72901524
DDFF	3.523	3.853746
C^{2}MOS	0.87515	1.769107

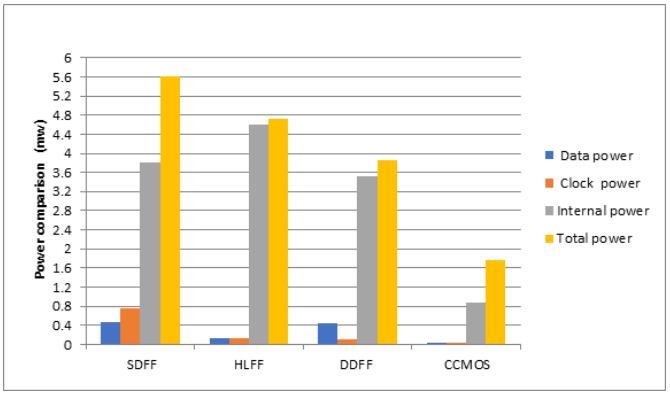

Figure10: Graphical representation of power comparison for Flip-flops in Pulse mode

Table 4 depicts the comparison of convention Flip flops and proposed Clock gating RCGFF design.

Table 4 .Comparison of Flip-flops in Pulse mode with Razor

Razor					
Parameter	**SDFF**	**HLFF**	**DDFF**	**CCMOS**	**RCGFF**
Avg power (mw)	15	8.5	7.9	6.4	1.62
Static power (mw)	47.3	11.7	10.3	22.12	3.43
Static current (mA)	26.2778	6.5	5.72	12.28	1.90
PDP (ns)	473	58	51	442	123
Time Delay	6.59 ns	41.9 ns	4.85us	2.45us	4.04ns
operating frequency	100 MHz	100 MHz	100 MHz	100 MHz	100 MHz
No of Transistor (area)	295	292	290	294	274

Table 4 shows that, Comparing to SDFF, HLFF,and Clocked CMOS, the proposed RCGFF achieves better power consumption, PDP, time delay and area consumption. The deigned RCGFF is integrated with PID controller to achieve the capability of timing error detection. Table 5 depicts the comparison of Razor in PID.

Table 5. Comparison of Razor in PID

Razor in PID controller					
Parameter	**SDFF**	**HLFF**	**DDFF**	**CCMOS**	**RCGFF**
Avg power (mw)	12	9.23	8.07	4.25	4.00
Static power (mw)	50.8	18.5	8.78	12.44	6.48
Static current (mA)	28.26	10.27	4.87	6.91	3.60
PDP (ns)	254.423	240.666	131.7	311	298.5
Time Delay	10	2.202	21.9	10	10
operating frequency	100 MHz	100 MHz	100 MHz	100 MHz	100 MHz
No of Transistor (area)	414	350	348	390	370

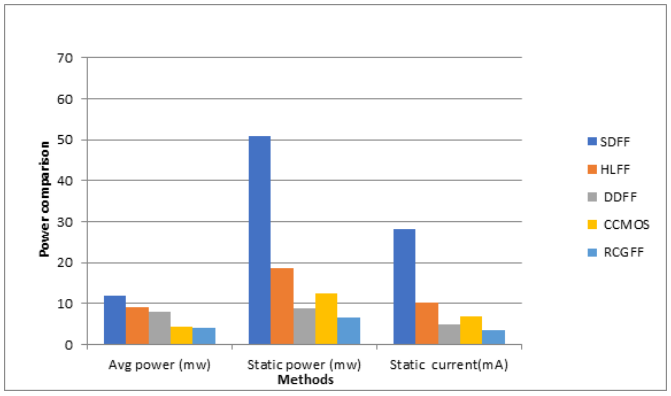

Figure 11: Graphical representation of power comparison for Razor in PID

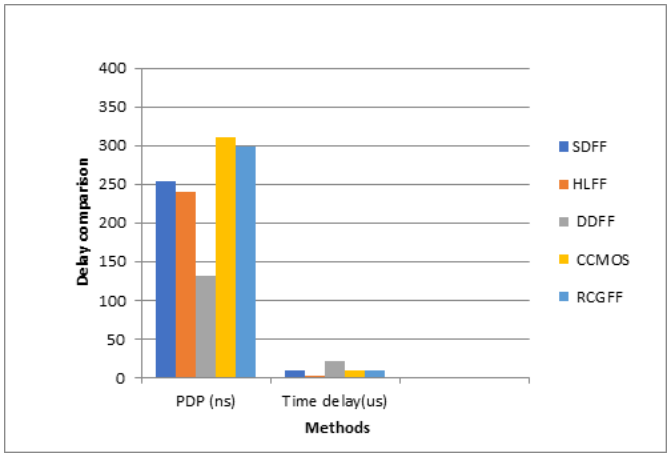

Figure 12: Graphical representation of delay comparison for Razor in PID

The proposed RCGFF achieves minimum average power and static power compared to the existing SDFF, HLFF,DDFF and Clocked CMOS, which is shown in Figure 11 and 12.

5. Conclusion

A novelty has been introduced by designing PID controller with Razor clock gated flip-flop. This technique is appropriate for application incorporating low power and scenarios with data communication in PID controller. The main advantages of this design are low power, low leakage current, and low Timing error. Tanner EDA tool using 130nm CMOS has been used to analysis varies parameters like power consumption, Power Delay Product (PDP), time delay and area for the proposed design against the existing Semi-Dynamic Flip-Flop (SDFF), Dynamic Data Flip-Flop (DDFF), Hybrid Latch Flip-Flop (HLFF) and Clocked CMOS Flip-Flop (CCMOS).From the simulation it has been proved that the proposed design is suitable for higher-precision, higher-speed, reduction in static power and average power consumption in a PID controller. It attains 74% of power reduction comparing to conventional existing design. Future work can be done on tuning PID controller with Glowworm Swarm Optimization (GSO) and type of fuzzy cascade controller

References

1. Bassi, S.J., Mishra, M.K. and Omizegba, E.E., 2011. Automatic tuning of proportional- integral-derivative (PID) controller using particle swarm optimization (PSO) algorithm. International Journal of Artificial Intelligence & Applications, 2(4), p.25.
2. Skoczowski, S., Domek, S., Pietrusewicz, K. and Broel-Plater, B., 2005. A method for improving the robustness of PID control. IEEE Transactions on Industrial Electronics, 52(6), pp.1669-1676.
3. C. Edral, A. Toker and C. Acar, "OTA-C Based Proportional-Integral-Derivative (PID) Controller and

Calculating Optimum Parameter Tolerances," Turkish Journal of Electrical Engineering and Computer Sciences, Vol. 9, No. 2, 2001, pp. 189-198.

4. Srisakultiew, S. and Siripruchyanun, M., 2013. A synthesis of electronically controllable current-mode PI, PD and PID controllers employing CCCDBAs. Circuits and Systems, 4(03), p.287.
5. E. Cevat, "A New Current-Feedback-Amplif Based Proportional-Integral-Derivative (PID) Controller Realization and Calculating Optimum Parameter Tolerances," Pakistan Journal of Applied Sciences, Vol. 2, No. 1, 2002, pp. 56-59. doi:10.3923/jas.2002.56.59
6. Srisakultiew, S., Lawanwisut, S. and Siripruchyanun, M., 2013, February. A synthesis of current-mode PI PD and PID controllers employing CFAs. In The Proceeding of 51th Kasetsart University Annual Conference, Bangkok (pp. 144-151).
7. S. Minaei, E. Yuce, S. Tokat and O. Cicekoglu, "Simple Realization of Current-Mode and Voltage-Mode PID, PI and PD Controllers," Proceedings of the IEEE International Symposium on Industrial Electronics, Dubrovnik, 20-23 June 2005, pp. 195-198.
8. V. Srikul, S. Srisakultiew and M. Siripruchyanun, "A Synthesis of Current-Mode PI, PD and PID Controllers Employing CCIIs," proceeding of electrical engineering Network 2012 of Rajamangala University of Technology, Nong Khai, April 2012, pp. 513-516
9. Ghosh, A., Krishnan, T.R. and Subudhi, B., 2012. Robust proportional–integral–derivative compensation of an inverted cart–pendulum system: an experimental study. IET control theory & applications, 6(8), pp.1145-1152.
10. Hill, E.L., Lipasti, M.H. and Saluja, K.K., 2008, June. An accurate flip-flop selection technique for reducing logic SER. In *Dependable Systems and Networks With FTCS and DCC, 2008. DSN 2008. IEEE International Conference on* (pp. 128-136). IEEE.
11. Valadimas, S., Tsiatouhas, Y. and Arapoyanni, A., 2012, May. Cost and power efficient timing error tolerance in flip-flop based microprocessor cores. In *Test Symposium (ETS), 2012 17th IEEE European* (pp. 1-6). IEEE.
12. Sartori, J. and Kumar, R., 2009. Characterizing the voltage scaling limitations of razor-based designs. *Urbana*, *51*, p.61801.
13. Nejat, M., Alizadeh, B. and Afzali-Kusha, A., 2015. Dynamic flip-flop conversion: A time- borrowing method for performance improvement of low-power digital circuits prone to variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(11), pp.2724-2727.
14. Valadimas, S., Tsiatouhas, Y., Arapoyanni, A. and Xarchakos, P., 2013. Effective timing error tolerance in flip-flop based core designs. *Journal of Electronic Testing*, *29*(6), pp.795-804.
15. Roberts, D., Austin, T., Blauww, D., Mudge, T. and Flautner, K., 2005, March. Error analysis for the support of robust voltage scaling. In *Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on* (pp. 65-70). IEEE.
16. Panahifar,E.,&Hassanzadeh,A.2017.A Modified signal Feed-Through Pulsed Flip-Flop for Low power Applications,International journal of Electronics and Telecommunications,63(3),pp.241-246.
17. Adapur,R.S.,& Kumar,S.S .2018. A SEU Hardened Dual dynamic Node Pulse Hybrid Flip-Flop with an Embedded Logic Module .In International Conference on soft Computing systems, pp, 62-68.