FPGA BASED RIPPLE FREE ON TIME NON LINEAR DIGITAL PSM CONTROLLER FOR A SMPS

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Abstract – **This paper shows how to improve the efficiency of the digital pulse skipping modulation (DPSM) controller. The controller controls MOSFET switch of Switched mode power supply circuit (SMPS) with high switching frequency ranges from 50 kHz to 1MHz. The improved DPSM controller design exhibited in MATLAB Simulink and tested for the output stability. The Simulink model for digital PSM controller circuit is converted to VHDL coding and downloaded in Xilinx FPGA 3S250E/144 and is interfaced with the driver circuits to control the buck converter. Hardware of step down buck SMPS circuit is rated with 2A, 120W Maximum power. A closed loop model is tested in discontinuous mode. The converter is tested for two different loads such as inductive load and resistive load. Comparative analysis is done for two case studies.**

Index terms- Switched mode power supply, DC-DC Converter, Digital Pulse skip modulation (DPSM),Field programmable gate array, Digital pulse width modulation(DPWM), Zero order hold(ZOH), Proportional integral differential controller

I. INTRODUCTION

An increasing demand for electronic gadgets with increased power saving time with reduced loss is highly trending now a days. The power loss has been partially reduced by correct selection of number of skipping cycles. PSM depends on DPWM controller to produce the pulse width input, to charge a capacitor and it observed by switching of PWM [2]. It converts the input voltage to various levels of output voltage based on duty ratio. Wide range of applications of DC-DC converter like high performance regulated power supplies, Battery chargers, computers, photocopiers, televisions, timers, medical instrumentation, utility systems like very low frequency(VLF) transmitters, wireless communication power supplies.

Power management technique is important for all electronic applications for light load. It could be achieved by digital controller techniques instead of analog controllers. Digital controllers play vital role in power electronic systems. It produces both very low and very high switching frequency. If high switching frequency is achieved, and then the size of the filter components likes inductor (L), capacitor (C) is reduced, and hence the total size of the DC-DC converter is also reduced. Then the entire circuit can be used for portable electronic gadgets. Each and every electronic gadget, requires different voltage levels for different driver circuit.

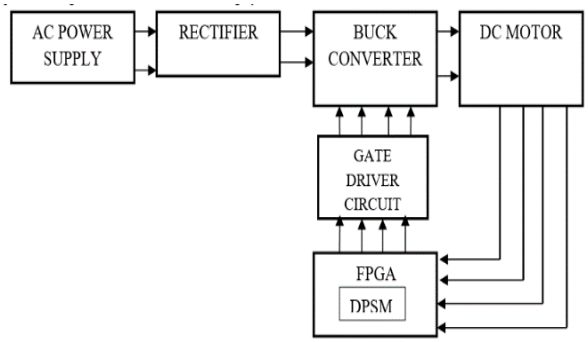

Fig.1, Block diagram of ripple free DPSM controlled Converter with DC Motor load

In DC-DC converter freewheel diode interval causes small duty cycle, it increases primary side conduction losses, switching losses MOSFET, inductor ripple current loss. These losses are overcome by PFM-SBC [4], which acts by varying the voltage across the capacitor in the output side.

In trimode chopper load sensor, optimum time controller achieves high efficiency among large load range. It is helpful for system on chip applications without using PWM and PFM mode. PSM technique achieves high efficiency for small load current [5].

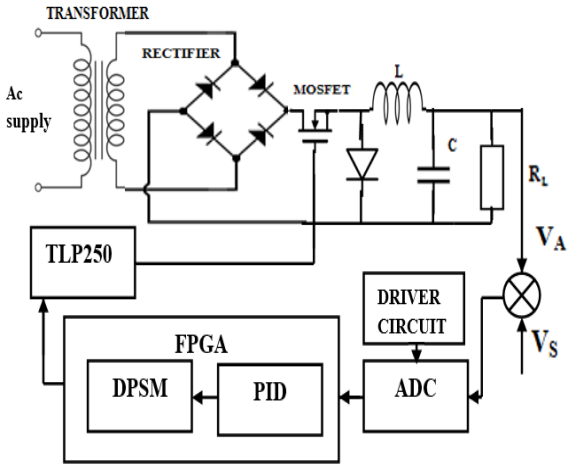

Fig.2, Block diagram of ripple free DPSM controlled Converter with R_L load

In trimode chopper load sensor, optimum time controller achieves high efficiency over a large load range. It is helpful for system on chip applications without using PWM and PFM mode. PSM technique achieves high efficiency for small load current [5].

Multimode digital controller using regular off time PWM gives stable DC gain. It rejects the limit cycle fluctuation when the duty ratio is high [6]. The peak ripple current both input and outputs during all operating conditions are minimized over large load variations [7]. Existing PWM or PFM types are based on first order linearization methods. The PFM controlled DC-DC involves two comparator and flip-flops presented. Frequency modulated control system is developed. The sample and hold block involves a pole at the right half plane as a result of which linearized block is obtained [10].

If on time and off time is varied then the power band undergo non monotonic variation. Voltage controlled PSM achieves monotonic change in the periodicity if on time and off time varied. It retains the originality of the PSM and gives the flexibility to change the width of the duty ratio. It uses feedback and feed forward techniques[8]. Improved PSM technique involves adopted two kinds of duty ratio. The two duty ratios are larger duty cycle and smaller duty cycle. These two duty cycle regulates the output voltage gives improved stability response in speed [9].

Fuzzy PSM includes fuzzy rules and simulation .It attains high efficiency and quick response comparing with basic PSM without losing the originality of DC-DC converter it reduces the ripple of the output voltage with audible noise interference [11].

The two phase DC-DC converter is controlled by the digital controller. The small and large signal models are analyzed. The lag compensator included in the feedback loop to obtain desired performance [12]. The high frequency controller controls DC-DC converter based on the synchronous binary counter with DSP system. The switching frequency of 4MHz is obtained due to which the number of logic devices in a single IC can be reduced. It permits multiple operations in single IC .PWM control logic is implemented in CPLD IC's [13].

Mixed signal simulation is used to design the digital controller for chopper. The controller model is implemented in ASIC. The digital controller increases the flexibility and lowers the sensitivity thereby reducing passive components [14]. The discrete time modeling control is applied to the PSM scheme. The discrete analysis achieved for four regions. Stable periodic behavior and non-monotonic variation in periodicity is achieved [15].

PWM controller for small power step down converter modeled and implemented. The delay line based PWM, comparing the reference value and the ramp value. The delay of delay line controlled by total buffers are starved the current is limited by a MOSFET device in linear region the threshold voltage limited to 0.8V [16].

Frequency adaptive repetitive control scheme applied to the power converter. Taylor series is used for delay line filter design. The structure containing M+1 sub filters. Lagrange interpolation applied for sub filters. Increasing the M order in the Taylor series results the increased bandwidth. To find the frequency integer part (Ni) and fractional part (P) are calculated in on line this design gives the variable frequency signal without redesigning the RC filter [17].

Direct Current (DC) motors are widely used in several industrial and home applications. Further DC motors are controlled with any digital systems so that the speed can be controlled by a digital controller for best performance. Drawback of DC motor is higher torque ripple and the drive circuit produces unwanted harmonics which reduces the power quality and causes unwanted electromagnetic interference [18].

The goal of this paper is to obtain the stable output with reduced harmonics. It can be achieved by implementing DPSM controller in standalone FPGA by combining with ADC I^2C bus successive approximation technique involved with SDA and SCK busses. This digital controller controls

the SMPS. The design values L=0.2X10^{-6} and C=0.3X10^{-3}F are soldered in outside FPGA. Different power stages are applied in the hardware, for FPGA circuit, voltage level is 12V and for MOSFET driver circuit, voltage level is 7V. The experimental results of DPSM are shown in the last session in this paper.

II.MATHEMATICAL MODELLING

Meticulously obtaining stability for power electronic converter to obtain nominal value for nonlinear model based on the linearization method (with small deviation from ideal operation). Considering the actual voltage, input voltage and duty ratio the equation becomes,

$$\frac{V_a}{V_i} = \frac{D}{D+\Delta} \quad (1)$$

Where V_a is the actual voltage and V_i is the input voltage D is the duty cycle of the converter. We can rewrite the equation to get Δ. It is named as equation (2)

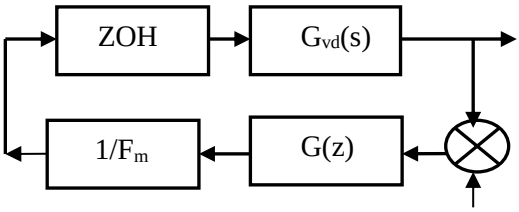

Fig.3 Discrete time modeling of PSM Controller

$$\Delta = D\left(\frac{V_i}{V_a} - 1\right) \quad (2)$$

$$\overline{I_0} = \frac{V_i T_i}{2L} D\Delta \quad (3)$$

Now substitute equation (2) in (3)

$$\overline{I_0} = \frac{V_i T_i}{2L} D\left(D\frac{V_i}{V_0} - 1\right)$$

Taking small signal values for D to d and I_0 to i_0

$$\overline{I_0} = \frac{V_i T_i}{2L} D^2\left(\frac{V_i}{V_a^2} - 1\right) \quad (4)$$

$$\widehat{\iota_0} = \frac{\partial \overline{I_a}}{\partial D}\hat{d} + \frac{\partial \overline{I_a}}{\partial V_a}\widehat{v_a}$$

$$\cong \frac{V_i T_i}{2L} 2D\left(\frac{V_i}{V_0} - 1\right)\hat{d} + \frac{V_s T_S}{2L} D^2\left(-\frac{V_i}{V_a^2}\right)\widehat{V_a} \quad (5)$$

$$\widehat{\iota_0} \cong \frac{2I_0}{D}\hat{d} - \frac{D+\Delta}{R}\widehat{v_0} \quad (6)$$

A. Design of converter

When the switching frequency is increased heat may be produced in the inductor which is due to saturation, residual flux and hysteresis is imbalanced. Hence the proposed DPSM controller produces more heat because of nonlinear pulse width in the controller output. This can be overcome by properly selecting the coil with increased air gap for certain limit.

The value of inductance L_I can be derived as follows

$$V_{LI} = L_I \frac{di}{dt} = L_I\left(\frac{\Delta I_{LI}}{(1-D)T}\right) \quad (7)$$

$$L_I = \frac{V_{OUT}(1-D)}{f_{SW} \cdot \Delta I_{LI}} \quad (8)$$

Where f_{sw} is the switching frequency of the converter. Assuming 30% of ripple value allowed

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

Where Δ is the 30% of allowed ripple value.

I_{pk}=100A

Inductor must sustain the peak current up to 100A.

B. Capacitor selection

The output capacitor filters inductor current ripples and delivers the stable output voltage

$$\Delta I_{Cout} = \left(\frac{V_{out}}{n.f_{SW}}\right)\left(1 - \frac{D}{L}\right) \quad (10)$$

$$C_{out} = \frac{(1-D)\,V_{out}}{\Delta V_{Cout} \cdot 8L\,.n.f_{sw}} \quad (11)$$

III.PROPOSED DPSM CONTROLLER

The converter output less than the reference value the pulses are generated and applied to MOSFET switch .If the converter output greater than the reference value the pulses are skipped. Hence output maintained close to the reference value. When MOSFET switch is on the inductor current rises and MOSFET switches off condition then the inductor current go to lower value, during this condition the pulses are skipped the inductor current go to very low value. Alternatively applying the pulses and skipping the pulses in the equal time period (Pa + Qs) of each duration of the period. Based on the inductor charging and discharging the pulses are skipped and applied to the converter circuit. The basic PSM controller shown in fig.4.The basic PSM controller output applied to the MOSFET but the output is not stable.

Where, Pa-Pulses applied , Qs-Pulses skipped

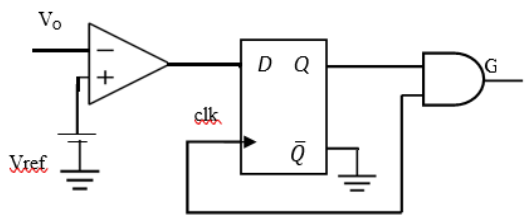

Fig.4 Basic PSM controller

If the controller to be stable all the poles present in right half side should be placed in the left side of the plane. For that the controller should be designed based on the closed loop transfer function. If the closed loop transfers function is first order it is easy to tune the controller because all the poles are in the right side but since the controller is second order transfer function so tune the controller is difficult. The proposed controller is designed to tune for achieving stable operating point for all higher frequency ranges. The principle of error deduction at the output side by comparing with reference. At every sampling point controllers compute exact values [m_1, m_2, $m3_{\ldots}m_n$]Where, V_{set} is the set voltage, V_{actual} is the actual voltage from the DC-DC converter.

$$m_1 = \sqrt{(V_{set1})^2 - (V_{actual1} + E_{h1})^2} \quad (12)$$

$$m_2 = \sqrt{(V_{set2})^2 - (V_{actual2} + E_{h2})^2} \quad (13)$$

Controller can find the errors up to n times

$$M_n = \sqrt{(V_{setn})^2 - (V_{actualn} + E_{hn})^2} \quad (14)$$

When the set voltage greater than the actual voltage, the comparator output voltage is maximum. Now, all Flip-flop outputs are high hence the output of AND gate is high and finally it sets delay flip flop. Now pulses are applied to the MOSFET switch. This period is known as inductor rising edge period. Similarly set voltage lower than the actual voltage comparator gives the minimum value. The output logic AND gates is low and it resets the all D flip flops regardless of the clock pulses, at this time clock pulses are skipped. This is known as falling edge period of inductor. Now converter output voltage is low value, and the MATLAB simulations results also showed in the figure.9, which are obtained from the MATLAB. The pulses are applied to the gate of the MOSFET switch. And also pulses are skipped in the case when actual voltage exceeds the reference voltage.

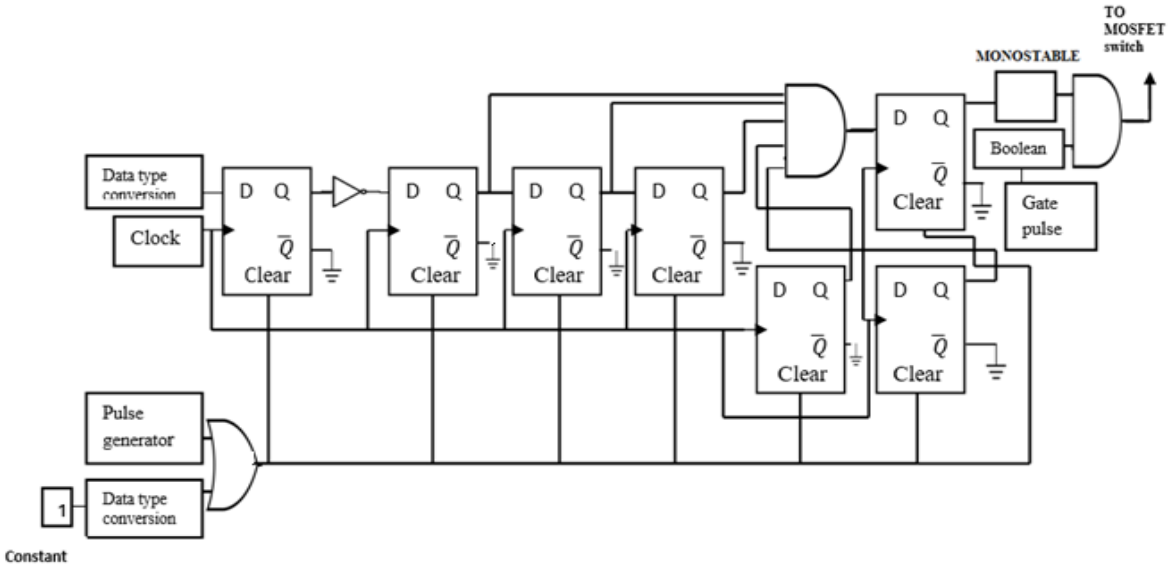

Fig.5 Proposed ripple free DPSM controller

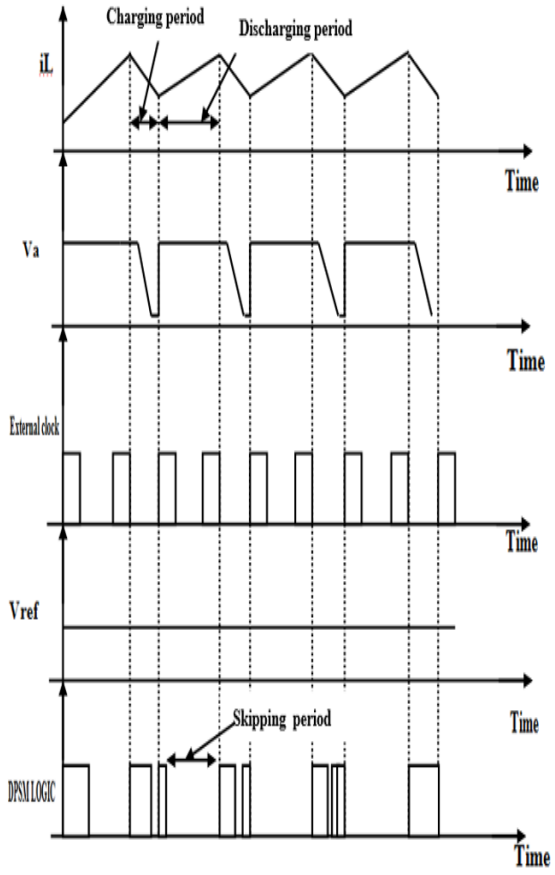

Fig.6 Waveforms of Proposed ripple free DPSM controller

IV MODELLING AND ANALYSIS OF DPSM CONTROLLER

A. Basic PWM DC-DC Converter

Pulse skipping provides increased efficiency at lower load currents. The DPSM feedback circuit consists of data type conversion block Based on Simulink we can observe values of linear model output and also nonlinear block output. To analyze ripples of inductor current, output voltage error, we can design the modeling of controller of practical system. Step down converter is controlled by pulse skipping modulations. it provide the delay using delay flip flop circuit. Comparator compares actual voltage V_a with set voltage V_{set} and its output is logic AND ed with CLK.

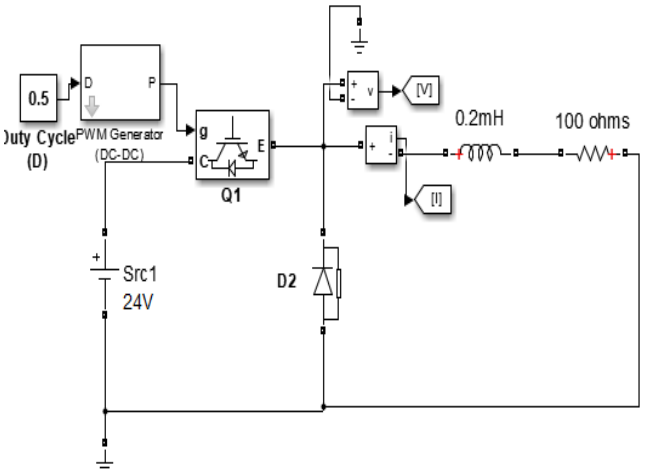

Fig.7 Simulink modeling of Buck DC-DC converter

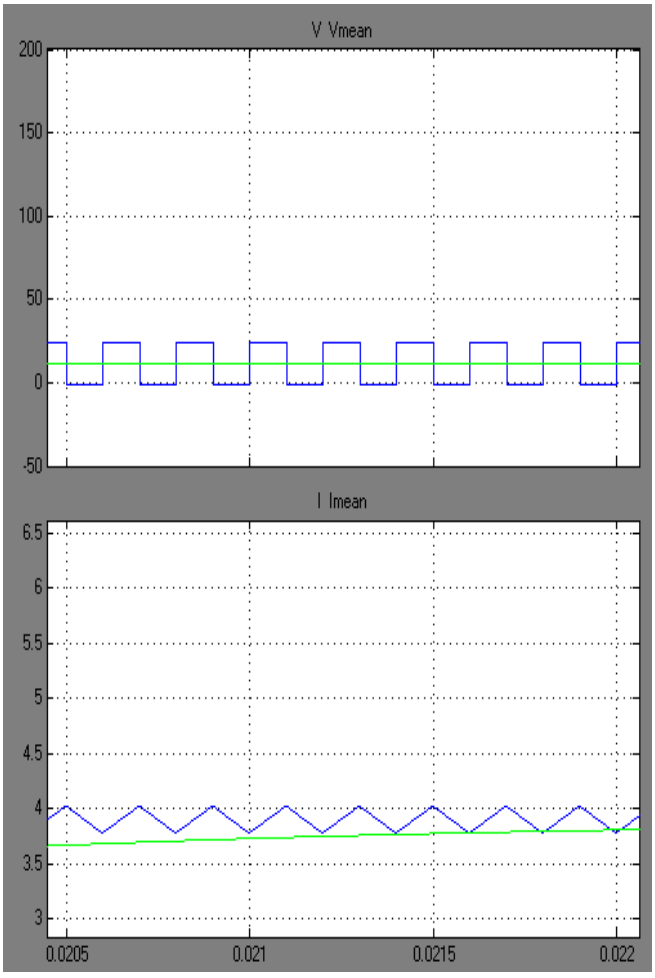

Fig.8 Output voltage and current of Buck DC-DC converter

B. DPSM controlled DC-DC Converter

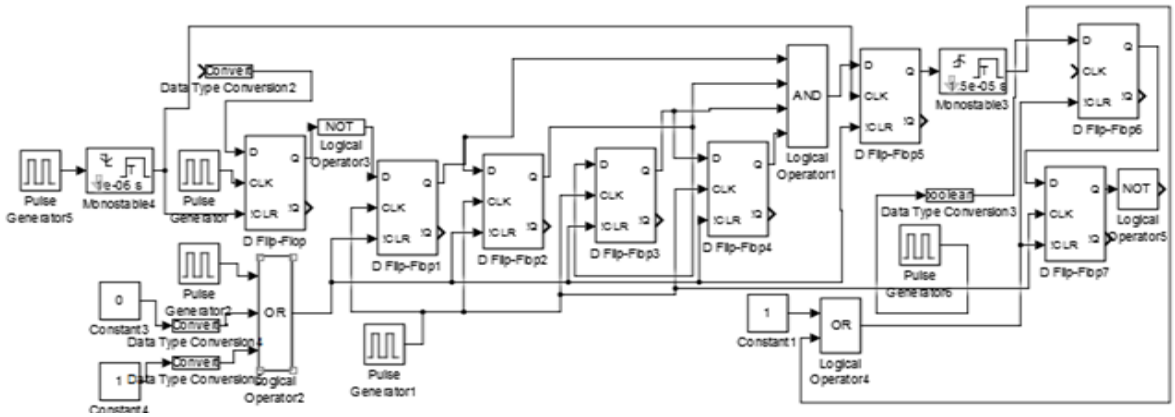

Fig.9 Proposed DPSM controller in MATLAB Simulink model

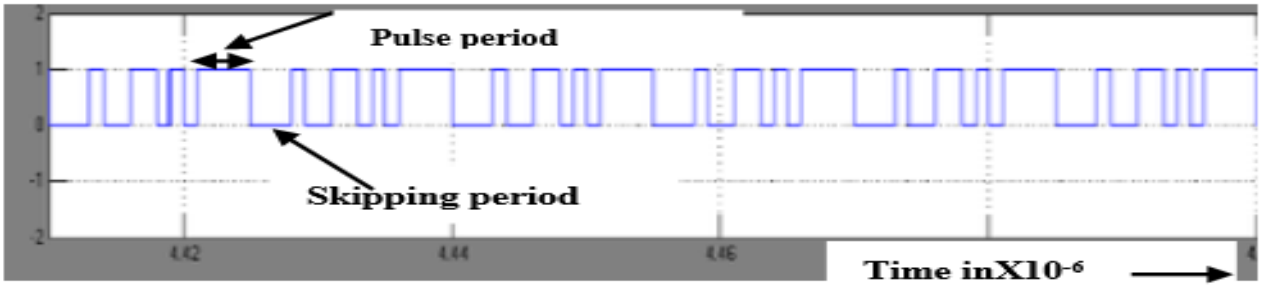

Fig.10 Output waveform of Proposed DPSM controller in MATLAB Simulink

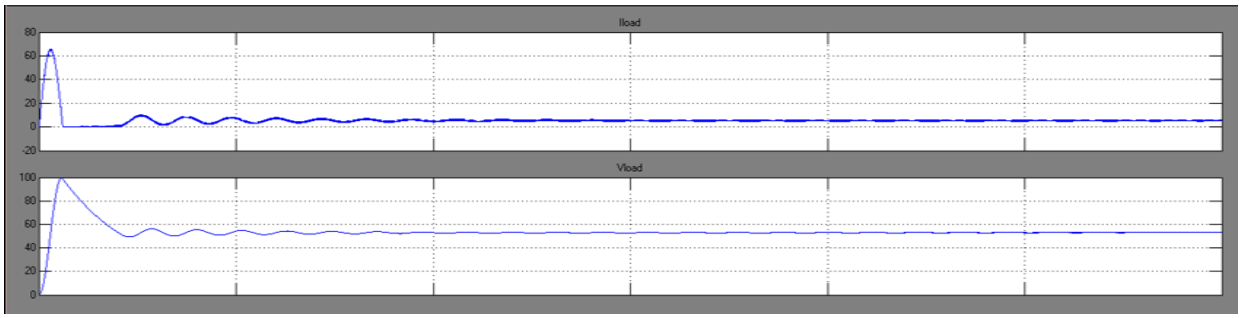

Fig.11 Output waveform of Proposed DPSM controller in MATLAB Simulink

V DESIGN SPECIFICATIONS OF CONVERTER

TABLE I

Parameters	Values
Input voltage	24V
Output voltage	(6V to 20V)
Load resistance	50ohm to 500ohm(2A rating)
Inductive load (DC motor)	1000 rpm-1500rpm
Inductance	$0.2X10^{-6}$ H (Ripple current up to 30%)
Capacitance	$0.3X10^{-3}$F
Output ripple voltage	$100X10^{-3}$V
Inductance peak current	100mA
Frequency range	15KHz to 50KHz
Maximum Power	120W

V.HARDWARE IMPLEMENTATION ON FPGA AND EXPERIMENTAL RESULTS

A step down converter hardware is designed and the DPSM controller is implemented in the SPARTAN FPGA board. The input voltage fixed as 24V, F_{SW} = 25 KHz, L = $0.2X10^{-6}$H, C = $0.3X10^{-3}$F, ripple current 30% allowed, I_{LR} = 100A, ΔV_{COUT} =100mv, R_L=500Ω, BYQ28E Diode, PCF8591 ADC IC is used with (I^2C) protocol .The hardware tested for various inductive and resistive load. The various load ranges of load comparisons are done.

BYQ28E Diode: This special diode used for high switching frequency SMPS. It has low voltage drop forward biased condition with less surge capability. High thermal cycling performance.

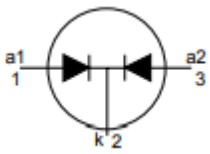

Fig.12 special diode symbol

PCF8591 ADC IC: It is a single IC, uses successive approximation type principle .During A/D conversion high gain comparator and D/A converter are used for the conversion. The conversion cycle starts when sending a read address to ADC IC device .This device triggered at trailing edge of clock pulse of and executed while transmitting the result of previous conversion.

Xilinx FPGA 3S250E/144: The Spartan 3E family reduces the cost per logic cell. Improves the performance of the system and 90nm technology used. It permits user design upgrades without changing the hardware replacement.

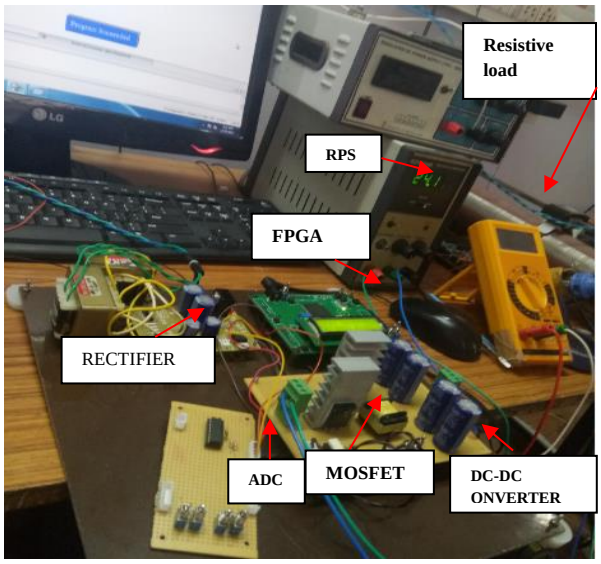

Fig. 13 Hardware set up of closed loop DPSM controller for SMPS with Resistive load

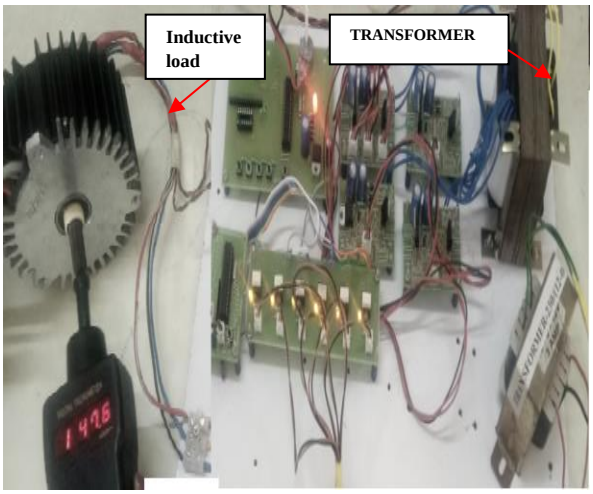

Fig. 14 Hardware set up of closed loop DPSM controller for SMPS with inductive load

The proposed ripple free DPSM controller controls the threshold voltage nMOSFET .respectively. Design components values of DC-DC converter are showed in table. Initially the 240V AC reduced to 24V by using step down transformer with frequency 50Hz. Fig.13 shows the transformer output with reduced third harmonics .This step

down voltage rectified to DC voltage by using bridge rectifier circuit. Outputs are shown in figure 14.

DC voltage applied to DC-DC converter. The proposed controller output shown in Fig.15.The pulses are skipped during the output voltage greater than the reference voltage. It gives the pulses when the reference voltage and output voltage are equal.

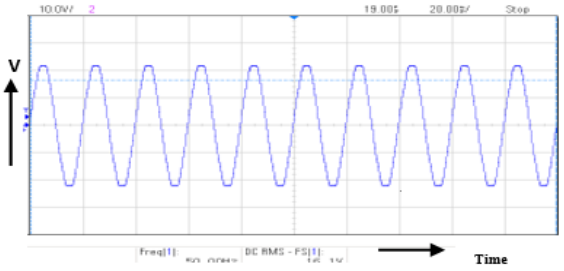

Fig. 14 Transformer output

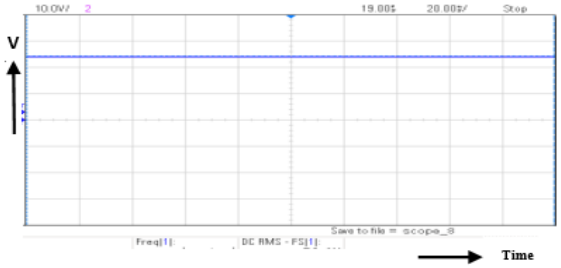

Fig.15 Rectifier output waveform

Then MOSFET gate is operated by driver circuit. Input for the driver circuit is given by DPSM controller with reduced harmonics.

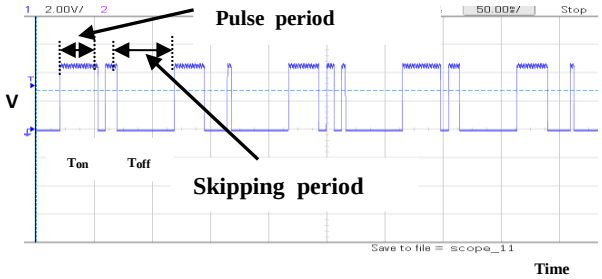

Fig.16 DPSM output waveform

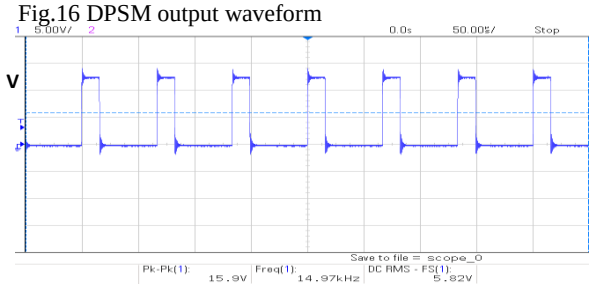

Fig.17 ADC output waveform

The input for DPSM is coming from PID block with error rectification done by comparator with ADC. Then discrete time harmonic compensator directly modeled in the VHDL programming with standard approaches followed by time domain specifications (4). In this document a digital PID is considered with K_P=50, K_I=0.1and, K_D=0.001. In time domain, gain and phase margins are 40 dB, 42^o respectively.

The final outputs of the DPSM controlled converter with variable frequencies are shown in fig.17 and fig. 18

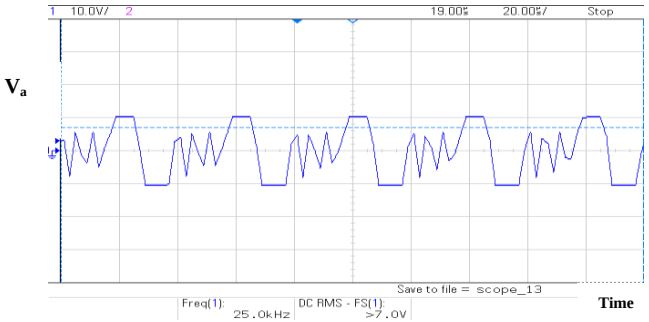

Fig.18 Converter output waveform with 25kHz

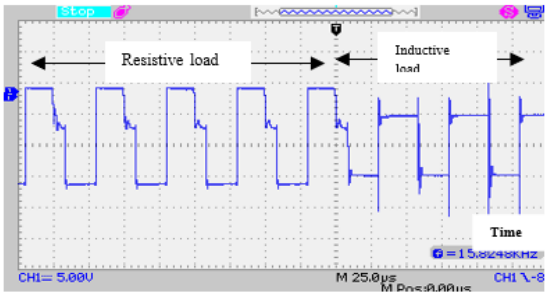

Fig.19 Converter output waveform with 14.99kHz

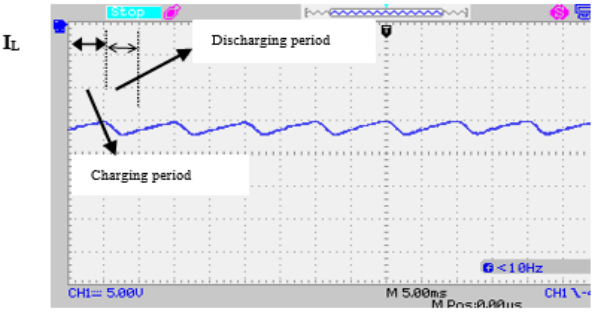

Fig.20 Converter output waveform with 25kHz

TABLE II

Case study: 1 Converter with Resistive load

Type of load	Input /Output voltage	Maximum power	Inductance peak current	Range	Output Ripple Voltage	Frequency range
Resistive load	24V/12V	120W	100mA	500Ω,2A	$100.1X10^{-3}V$	15KHz to 50KHz
				450Ω,2A	$98.6X10^{-3}V$	
				400Ω,2A	$97.3X10^{-3}V$	
				350Ω,2A	$95.2\ X10^{-3}V$	
				300Ω,2A	$92X10^{-3}V$	
				250Ω,2A	$91.24X10^{-3}V$	
				200Ω,2A	$90.01X10^{-3}V$	
				150Ω,2A	$89.9X10^{-3}V$	
				100Ω,2A	$89.4X10^{-3}V$	
				75Ω,2A	$89.02X10^{-3}V$	
				50Ω,2A	$89X10^{-3}V$	

TABLE III.

Case study 2: Converter with Inductive loads

Type of load	Speed References	Load Reference	Open Loop		Close Loop	
			Speed	Stator Current	Speed	Stator Current
Inductive load	@ 1000 RPM	@ 1 N/m	@ 1 N/m Speed is 1578 RPM	1.5 A	1000	2.1 A
		@ 3 N/m			1000	4.01 A
	@ 1100 RPM	@ 1 N/m	@ 3 N/m Speed is 1500 RPM	1.75A	1100	2.25A
		@ 3 N/m			1100	4.15A
	@ 1200 RPM	@ 1 N/m	@ 3 N/m Speed is 1500 RPM	1.9A	1200	2.4A
		@ 3 N/m			1200	4.2A
	@ 1300 RPM	@ 1 N/m	@ 3 N/m Speed is 1500 RPM	2.1A	1300	2.6A
		@ 3 N/m			1300	4.25A
	@ 1400 RPM	@ 1 N/m	@ 3 N/m Speed is 1500 RPM	2.2A	1400	2.7A
		@ 3 N/m			1400	4.28A
	@ 1500 RPM	@ 1 N/m	@ 3 N/m Speed is 1500 RPM	2.3 A	1500	2.8 A
		@ 3 N/m			1500	4.3 A

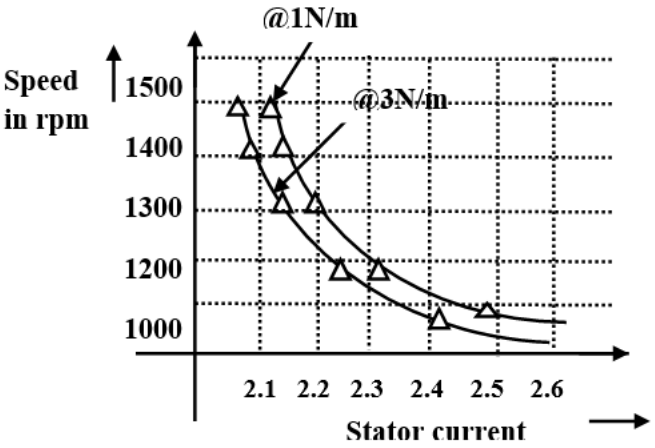

Fig.21 Output characteristics of speed vs stator current

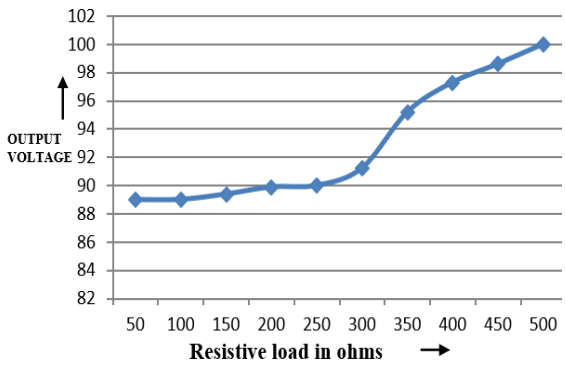

Fig.22 Converter output voltage vs various resistive load

VIII.CONCLUSION

This paper discussed about discontinuous mode DPSM controller for DC-DC converter. Variable high frequency switching applied for both resistive and inductive loads. The load range limited to 2A current rating, it is based on design components of hardware. High efficiency maintained from 500mA to 2A various load variations. Experimental results show the ripple free output voltage and current. Stability analysis of linearized modeling and design of DPSM were discussed and designed in the MATLAB Simulink. The prototype of step down converter developed and tested. DPSM controller implemented in FPGA board, hence the controller is programmable. Digital PSM improves the light load efficiency and gives stable operating conditions.

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