# DESIGN OF LINEAR RAMP GENERATOR AND DIGITAL ORA FOR AN AREA EFFICIENT HIGH SPEED ADC BIST

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***Abstract:*** *This paper presents a design of linear ramp generator and a digital output response analyzer for an on-chip testing of analog to digital converter. Linear ramp signal has generated by the self-biased adaptive ramp generator design and applied to the converter for test pattern generation. The digital output response of an analog to digital converter for the ramp signal has analyzed through the fully digital output response analyzer for the primary non-idealities of a converter. Non-ideal parameters have described in hardware description language and simulated to exhibit the performance and feasibility of an analog to digital converter in testing. The final uncertainty of the analog to digital converter outputs has observed through the proposed test scheme which detects the static errors in the logical evaluation procedure.*

***Keywords:*** *Ramp, Transition width, Integral non-linearity, Differential non-linearity, Built-in self-test, ADC.*

## 1. Introduction

Analog to digital converter (ADC) is a mixed signal banding system of analog circuit and digital circuit, and it has a capacity of evaluating the performance of the mixed signal devices. Extensive applications and the increasing popularity of ADC forces the inventor to design the converter with high performance and accuracy. To obtain high precision data conversion, the design of a converter must produce an error free output code in the testing process. Most common ways of ADC testing are ensuring the accuracy of the comparison of actual and ideal characteristics. Also, the static parameters (Linearity, offset, gain) and dynamic parameters (noise, threshold, and distortion) are verified to observe the perfectness of digital output. In standardized testing methods, linearity has considered as an important parameter since it decides the transfer function of ADC. The nonlinearity found due to the parasitic components of the converter circuit figures the static and dynamic performance characteristics [1]. Thus, an effective testing block implementation for detecting the linearity leads the design of ADC to acquire high precision digital data from analog signal [2]. The high-resolution ADCs offer extremely high noise with robustness against the process variation. Comparative analysis of ADC parameters is a common method to project the noise effect in the data conversion.

## 2. Existing Methods

Automatic test equipment (ATE) is a method, popularly used in the standard conventional off-chip testing method. However, the use of ATE circuit is the toughest and costliest one in the high-resolution analog mixed signal (AMS) circuit testing [3]. Also, the long evaluation time, accessing limitations of logic functions and unavailability of external resources in support of complex applications cut down the use of off-chip testing. Due to these drawbacks, on-chip testing methods [4] are highly preferred in the next generation IC testing, but the testing block uses an additional area in the silicon die. In the initial stages of 3-dimensional IC, the functionality of on-chip testing increased with reduced power and latency [5], but it has failed to attain the controllability and observability in testing [6] - [7] due to the deficiency of input/output pads. To overcome these problems, the circuit under test (CUT) incorporated with highly demanded on-chip testing techniques called design for testability (DfT) and built-in self-test (BIST). DfT and BIST are the major technological differentiator with enhanced quality control, lower production cost and testability features [8]. A limited test resource requirements and the support of parallel testing takes the BIST based testing one step ahead from DfT based testing. Also, the BIST is portable to incorporate with the mixed signal circuit like ADC, which is not only yielding industry standard testing, furthermore, reduce the cost and increase controllability, observability, and accessibility of test parameters.

A deviation in linearity parameters of ADC is the errors which cannot be calibrated and corrected certainly in testing methods. In [9], Static and spectral analysis have effectively used to measure the non-linearity. The static analysis develops a pre-consolidated histogram with extended test time while the spectral analysis generates the step signal using the precise input signal. The generated step signal covers

the full scale conversion range of ADC with good accuracy. The use of precise input signals requires an efficient signal generator in addition to the system blocks [10]-[11]. Histogram method is an alternative technique for testing linearity of data converters. It has performed in two phases with nonlinear input: first, it generates the test pattern and then compares the output of ADC with a generated test pattern to diagnose the error. The use of linear signal for pattern generation cut down the required testing time with improved fault coverage. But when the resolution of the ADC is increasing, the circuit to occupy large area overhead for storage with large number of test patterns. To address this problem a multi-histogram method presented in [12]-[13]. In this, the input signal has broken down into small sections and then each section generates the histogram with a small amplitude sequentially. Conversely, it is not a suitable solution due to the discontinuity raised when the transition carried out from one section to the next. For high-resolution ADC testing, ref. [14]-[17] proposed the Fast Fourier Transform (FFT) based mixed signal circuit test methods which are more suitable for using few thousand samples. One restriction is that the FFT cannot be employed directly in the data converter for linearizing or measuring the static characteristics due to the accessing uncertainty of nonlinearity description test procedures present in the frequency domain. Also, the complex multipliers found in the testing stream use many buffers which requires an additional area to build the storage elements and that make the on-chip FFT based ADC BIST as very complicated. For lowering the overhead, a cost-effective signal generator is proposed in [18] using stimulus error identification and removal (SEIR) algorithm and in [19] using triangular input for nonlinearity estimation. The actual implementation of signal generators in an analog form reduced the area, but the variation of dynamic parameters in an analog test circuit may degrade the performance and the accuracy of testing. For high precision testing, the histogram based output response analyzer (ORA) proposed and used effectively in [20]-[21] with the help of double CORDIC techniques. In which, the test vectors are generated by the modified histogram based test pattern generator (TPA), and then stored in the memory elements for testing. A fully digital ORA has implemented in [22] for high-performance ADC testing. The main advantages of digital BIST are the low area overhead [4] and the ability to test integral non-linearity (INL) and differential non-linearity (DNL) for all digital codes, which eliminates the unnecessary calibration [23]-[24] during the fault diagnosis. A fully digital based BIST technique [25] is well suited for distributed architecture where the routing path of an analog signal minimized over long distance interconnections. A code width based ADC BIST has proposed in [26]-[28] to detect parametric, arbitrary and catastrophic faults and the ADC is repeatedly tested to find the faults. The built-in area requirement of on-chip digital BIST is fluctuating with the resolution of the ADC. However, the overhead and linearity of the on-chip ADC testing are a primary concern in the BIST design.

## 3. ADC BIST

An ideal ADC converts the continuous time signal into discrete N-bit digital code. It is mathematically represented as

$$V_i(t) = q2^{N-1}.\sin(2\pi ft) \xrightarrow{Encode} V_{FS}\sum_{k=0}^{N-1}\frac{d_k}{2^{k+1}} + \xi \qquad (1)$$

Where q is a weight of 1 LSB, N is a resolution, $V_{FS}$ denotes the full-scale voltage, $d_k$ denotes a digital output word, K is the number of bits and $\xi$ is quantization error. Considering the ramp signal as input, the signal generation is expressed as

$$V_{ramp} = \int \frac{I_C}{C}dt = \frac{I_C}{C}t + V_{ramp}(0) \qquad (2)$$

where $I_C$ is a charging current into the capacitor, C is the capacitance and $V_{ramp}(0)$ is the ramp voltage at starting position. The ADC converts an analog ramp signal into digital word sequence with different reference points in constant time interval as shown in Fig.1(a). A quantization points of analog signal has performed within the full-scale range of ramp. The quantum voltage level ($V_q$) between two analog reference points is calculated by,

$$V_q = \frac{V_{ramp}}{2^N} = 1.LSB \qquad (3)$$

where $V_{ramp}(C)$ is the full-scale conversion range of ramp signal, N is the resolution of ADC

In practice, the performance and accuracy of the ADC are affected due to the non-idealities caused by characteristic mismatches and the nonlinearity's caused by component mismatches. The variants in the quantization staircase called non-ideality where the mismatch between the ideal and actual transition voltage called nonlinearity. The change of an analog input voltage leads to a transition in digital output word. Differential non-linearity (DNL) and Integral non-linearity (INL) are the two different nonlinearity parameters present in an ADC. DNL is the maximum deviation between the actual transfer curve and the ideal transfer curve between the two consecutive codes for the input axis [22], [25]. Mathematically, it is described as

$$DNL_k = \frac{\left|k.LSB\right| - \left|(transitionwidth)_k\right|}{k.LSB}, \forall k \to 0,1,2,.....\left(2^N - 2\right) \qquad (4)$$

where $(transition\_width)_k=(C_t(k)- C_t(k-1))$; $C_t(k)$, $C_t(k-1)$ are the LSB value at $k^{th}$ and $(k-1)^{th}$ transition positions, respectively. DNL error has initiated when the transition width is hived off from 1LSB. INL error is a deviation that occurs between the actual and the ideal transfer curve of a converter. Mathematically, it is described as

$$INL_k = \frac{\sum_{i=0}^{k-1}(transitionwidth)_i - k.LSB}{1.LSB}, \forall k \to 0,1,2,.....(2^N - 1) \quad (5)$$

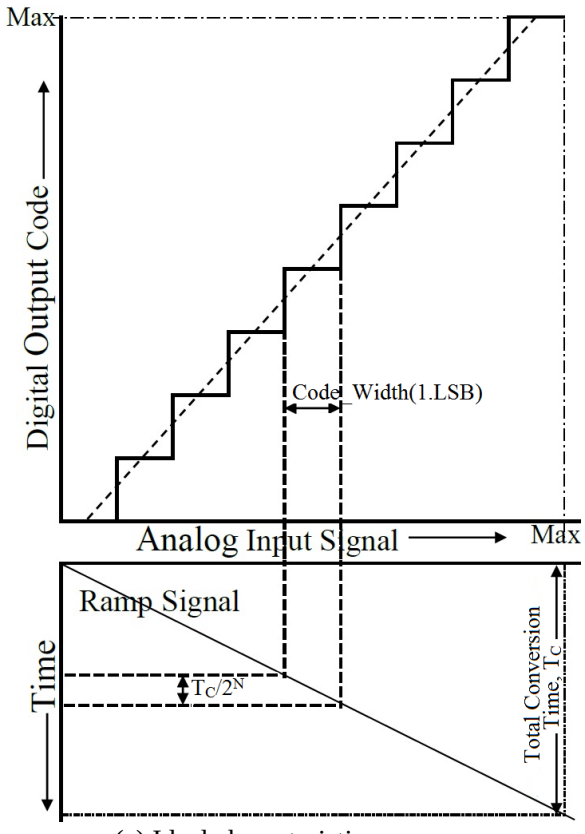
Offset error referred as a deviation that occurs between the actual and the ideal voltage at the first transition where a gain error referred as a deviation that occurs between the actual and the ideal slope of converter through the end points at zero and full-scale value in an ADC. The offset and gain errors evaluated by (for Unit LSB)

$$off_e = \frac{d_0 - d_{\min}}{1.LSB} \quad (6)$$

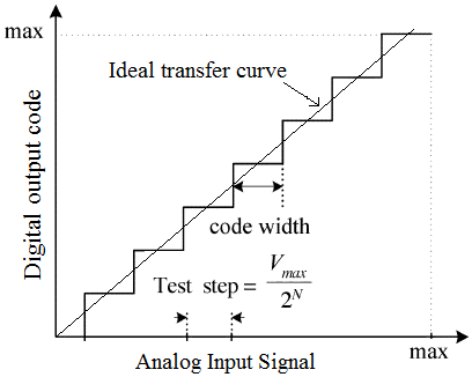
and

$$gain_e = \frac{d_{2^N-1} - d_{\max}}{1.LSB} - offset\,error \quad (7)$$

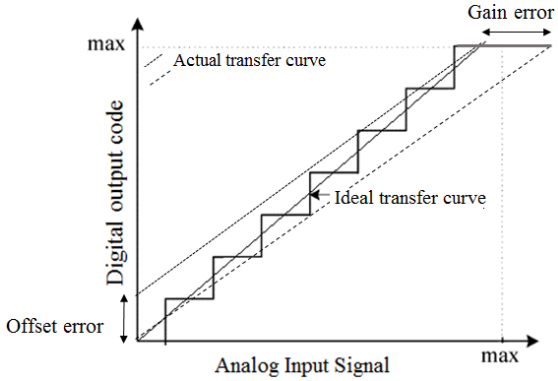
Where, $d_0$, $d_{2^N-1}$ are the digital output at zero and full-scale value of ADC, $d_{min}$, $d_{max}$ are minimum and maximum allowable code width of ADC with N-bit resolution.



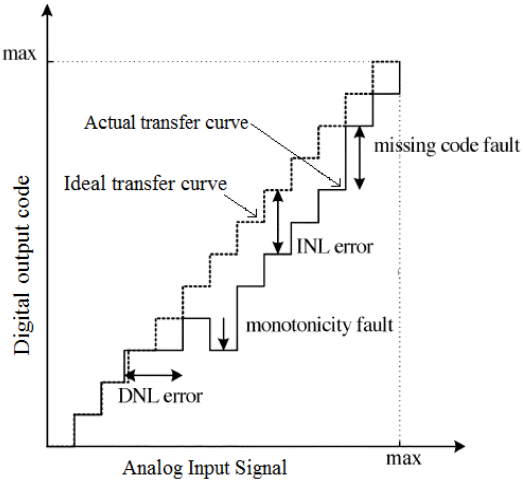

(a) Ideal characteristic response




(b) Measurement of Code width




(c) Measurement of Offset and gain error




(d) Missing code, Monotonicity, INL, DNL

Fig. 1. Characteristic response of A/D converter

This paper considers the measurement of non-linearity, monotonicity and missing codes in the ADC through the digital BIST Module. Monotonicity is known as a descending function in digital output as an analog amplitude increasing. The loss in digital code when an analog amplitude is increasing greater than 0.5LSB known as missing code error. Fig.1 illustrates the characteristic curve and the non-linearity parameters of ADC. The building blocks of proposed BIST have implemented with a fully digital circuit which claims the accuracy and efficiency of mixed-signal testing.

An efficient ADC BIST circuit has proposed and verified using adaptive ramp generator and digital output response analyzer (ORA). The ORA has designed to detect the presence of static parameters and non-ideal transitions in the primary test related input constraints. The nonlinearity diagnosis of data converter efficiently achieved Since the ORA blocks has implemented entirely with digital elements. The proposed design claims the effectiveness for test accuracy and an area overhead with the reduced test pattern storages and few test stimuli of testing blocks. Testing the nonlinearity of ADC has explained in the following sections with the reference of the proposed algorithm and the flow diagram.

## 4. Proposed ADC BIST

The proposed digital optimized BIST technique consists of an adaptive ramp generator, ADC (Circuit under test) and digital output response analyzer. The main aim of the work is to increase the test accuracy and shrink the area overhead and testing time of a built-in testing block with increased test accuracy. Another constraint concern with ADC testing is to generate the linear input signal that generates quality test samples for testing. Also, the digital-based test block requires perfect timing in the switching of digital code in its input terminal. To illustrate this point, a self-biased adaptive analog ramp generator has used to generate the input signal and 10-bit flash ADC has considered in developing the test samples. Also in mixed-signal testing, the digital-based testing block struggle with computation time and an area overhead of test blocks. By considering these constraints, the digital testing system has modeled mathematically and implemented as a memory controlled digital ORA. Fig.2 shows the hardware resources demanded to build the BIST architectures. It consists of a linear ramp generator, an ADC under test mode, the BIST module. Initially, the linear ramp signal is applied to the ADC to generate the digital test patterns and then the digital data have processed through the digital BIST module to observe the malfunctions/errors present in the output.

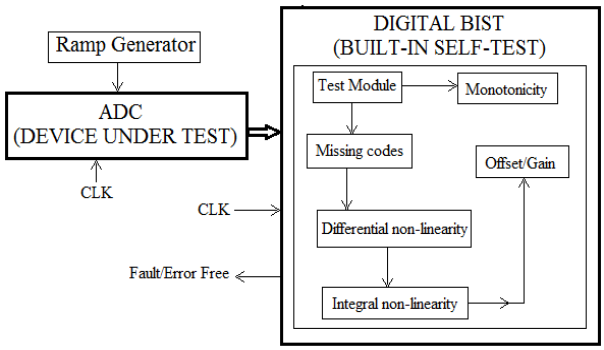



Fig. 2. Block diagram of Proposed ADC BIST

### 3.1 Linear Ramp Generator

The requirement high precision and low overhead adaptive ramp generator is considered for testing ADC's non-idealities. The static characterization of an ADC requires a slow enough slope of a ramp signal. An adaptive ramp generator has introduced as shown in Fig.3 to satisfy the above mentioned testing requirements. A self-biased current mirror (M1-M7) produces very stable output current to generate the linear ramp signal. Transistor M9 controls the current with the help of transistors M7-M8. Assuming linear operation of transistor M9, a well-controlled constant low current has applied to the capacitor. Slow charging of the capacitor with small current reduces the sensitivity of ramp signal to noise and leakage on the charging of the capacitor. The linear voltage ramp required for testing can be expressed as

$$I_C = C.\frac{dV_{ramp}}{dt}$$

$$= \frac{2K(W/L)_{10}{}^2(V_{Ctl}-V_{Tn})^2\left((W/L)_9-\sqrt{\left(\frac{L}{W}\right)_8\left(\frac{L}{W}\right)_9}+\left(\frac{L}{W}\right)_8\right)}{\left(K(W/L)_{10}(V_{Ctl}-V_{Tn})+1\right)^2} \quad (8)$$

$$V_{out} = \frac{I_C}{C}.t + V_{ramp}(0) \quad (9)$$

The total time period of the ramp signal is given by

$$T = \left(\frac{V_H - V_L}{2^N - 1}\right).M_{VI} \quad (10)$$

Where $M_{VI}$ is required a number of voltage intervals.

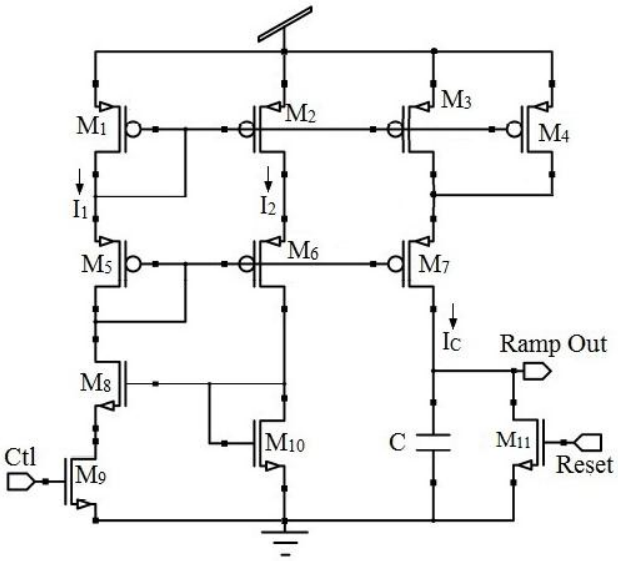



Fig.3. Schematic of adaptive analog ramp generator

### 3.2 ADC

A threshold inversion quantization (TIQ) comparator based flash ADC has designed for the circuit under test as described in [29]. The transistor scaled cascaded inverters form a TIQ comparator. The transistors of each comparator have scaled to set the threshold voltage to the required reference points. Threshold voltage of an inverter is expressed by

$$V_{th} = \frac{V_{tn}\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \Big/ \mu_p C_{ox}\left(\frac{W}{L}\right)_p} + (V_{dd} - |V_{tp}|)}{1+\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n \Big/ \mu_p C_{ox}\left(\frac{W}{L}\right)_p}} \quad (11)$$

where, $V_{dd}$ supply voltage, $V_{tp}$ and $V_{tn}$ threshold voltage of PMOS and NMOS transistor, respectively, $\mu_n$ and $\mu_p$ carrier mobility of electrons and holes of NMOS and PMOS, respectively, $C_{ox}$ gate oxide capacitance, $(W/L)_p$ and $(W/L)_n$ width/length of PMOS and NMOS transistor, respectively. Assuming $L_p$=$L_n$ and $\mu_p = 2.5\mu_n$, equation. (11) cab be reformed as

$$\frac{(W)_p}{(W)_n} = 2.5\left(\frac{V_{th} - V_{tn}}{V_{dd} - |V_{tp}| - V_{th}}\right)^2 \quad (12)$$

Equation. (12) confirms that the desired threshold voltages can be obtained by changing the width of transistors. The design of N-bit flash ADC has to be designed with $2^N$-1 TIQ comparators. The digital test pattern generated by the ADC through ramp signal is applied to the digital output response analyzer to measure the non-idealities.

### 3.3 Digital Output Response Analyzer

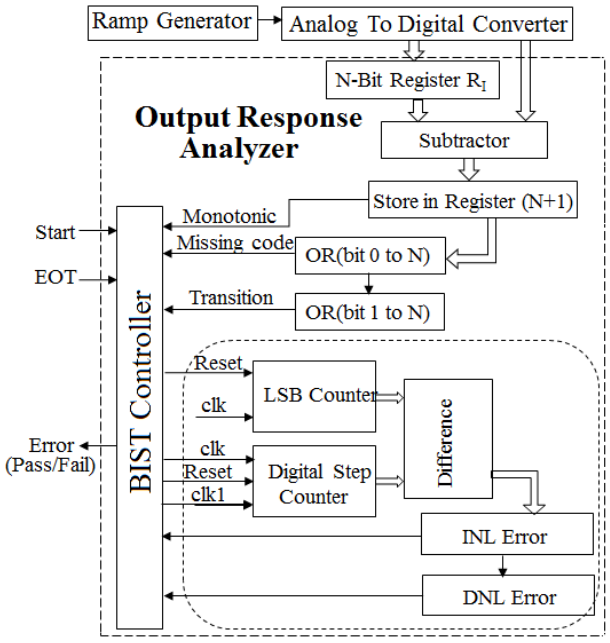



Fig.4. Architecture of Proposed BIST of ADC

The BIST module has constructed by a BIST controller and an output response analyzer which consists of subtractors, counters and few registers. The BIST controller enrolled as a master block among the test blocks to manage the functions of the digital data processing, and the control signals to enable and synchronize test blocks with ADC output. The counter block appropriated to count from 0 to $2^N$-1. In the proposed method, the ADC has tested to project the missing codes, monotonicity, transition error, and nonlinearity. A number of transitions taken out in a digital word are calculated by the ORA based on the step size of each code transition. The total number of transitions of an error free N-bit ADC are $2^N$.LSB. The total error free code resolution is expressed as

$$= \log_2\left(\frac{2^N}{Error\ in\ LSB}\right), \forall N \rightarrow 0,1,2,.....(N-1) \quad (12)$$

The error in the code transition is measured by a subtractor, in which the difference between two successive digital codes has been calculated to find the transition size. Since the transition code position is unknown, the step size of transition measured by calibrating the difference between the adjacent transitions in the output of the ADC. Identification of divergence in the difference output from the ideal transition helps to determine the faultiness of the result. The maximum deviation in the step size of each transition categorized to find the faultiness with the linearity error. By considering the maximum step size variation of ideal 1. LSB Value from (-Δ to +Δ), the divergence in the transition is expressed as

$$\nabla T_{step\,size} = (+\Delta) - (-\Delta) \quad (13)$$

Where, +Δ, -Δ are the maximum positive and negative side step variation in the transition curve.

In fault diagnosis, the test block calculates the integral nonlinearity first and then the DNL, gain and offset errors are calculated from observed INL. Since the INL error carried out from the accumulated digital codes, here, the nonlinearity is calculated by taking the difference between the ideal and actual code transition of any $k^{th}$ code, $d(k) = x(k) - x(k-1)$. Then, the INL error is calculated by taking the maximum difference in the transitions which are greater than the transition boundary. The BIST is using two clock signals with different time periods. In which the first clock enables the feeding sequence of digital data while the second clock permits to have the numbers of increment in the evaluation of integral non-linearity per word. Note: number of increments not restricted to a certain limit, it can be increased further by dividing the second clock cycle. In this structure, the increment factor is considered as 4 with 3-bit binary representation (one bit for integer; rest for fractions). Thus, the test architecture designed with

4-bits to observe the non-linearity errors. The first stage of test procedure calculates the difference between the adjacent digital data. In the second stage, the clock gets incremented to calculate the INL when the digital step size wider than 1LSB. The mathematical form of INL diagnosis is expressed as follows,

$$INL\ error = Max\left|\nabla T_{step\ size} - \nu T_{step\ size}\right|_k > \Delta.LSB,$$

$$\forall k = 1,2,,.....2^N \quad (14)$$

Where, $\nabla T_{step\ size}$ is an ideal divergence in the transition, $\nu T_{step\ size}$ is an actual divergence in the transition. Then the DNL error calibrated from the INL value as follows,

$$DNL\ error(i) = \begin{cases} INL(i) - INL(i-1); if\left(i \neq 0\right) \\ 0 \qquad\qquad\quad ; if\left(i = 0\right) \end{cases},$$

$$\forall i \to 0,1,2,.....\left(2^N - 1\right) \quad (15)$$

Offset error is the INL error observed in the first digital code transition where the gain error is the INL error observed in the last digital code transition. Monotonicity and missing codes are observed directly from the adjacent digital output code differences. The error named as missing code when the difference between adjacent digital word is greater than the ideal LSB value, where the difference less than zero or the transition is descending then the error named as monotonicity. In the architecture, the sign bit in the difference value states the monotonicity and the logic OR operation of {d1, d2, …..dN} states the missing code error. Table 1 shows the fault diagnosis of proposed BIST methods. The pseudo code and flow diagram of the proposed algorithms shown in Fig.3. The following test procedures are considered for testing ADC with the proposed fully digital BIST methods.

**Procedure of proposed ADC BIST**

1. Initialization of testing→ ADC has taken Under test: Apply a linear ramp input to the ADC and observe the digital output
2. Apply a linear ramp input x[t] to ADC and generate the discrete output sequence x[k] then convert into digital output X[N]

$$x[t] = \begin{cases} t, & t \geq 0 \\ 0, & t = 0 \end{cases} \xrightarrow{A/D\ converter\ yields} x[k] \quad (16)$$

$$X[N] = function\{x[t]\} = 2^N A/V_r \quad (17)$$

3. Apply the generated of digital output code X[N] into the BIST module

$$d_N = func\{X[N],2\} \quad (18)$$

4. Load the digital word to BIST module
5. Determine the difference of the adjacent digital output codes D(n)-D(n-1) to find the digital code transition

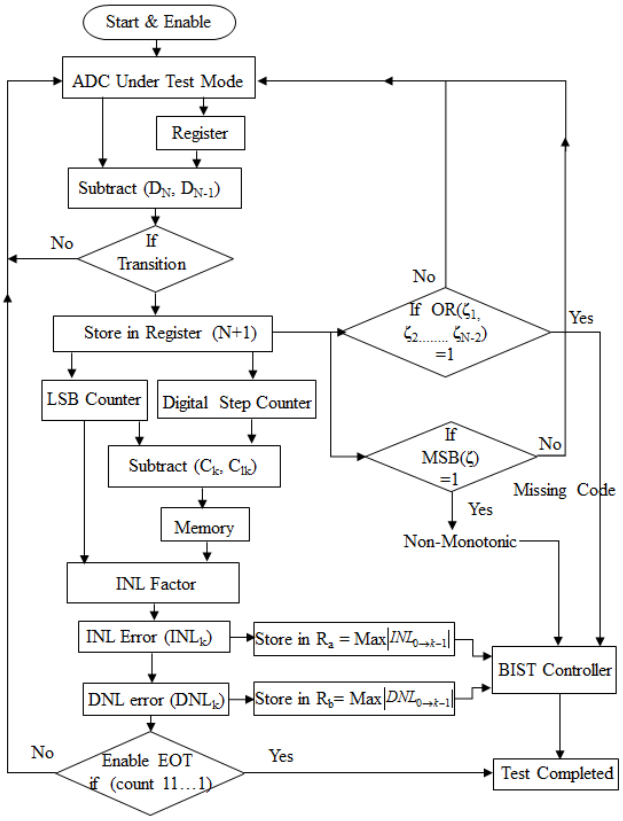
Table.1. *Fault Diagnosis of Proposed Digital BIST Techniques*

| ADC Specifications | Test Procedure of Proposed ADC BIST |
|---|---|
| Transition width | $(d_k - d_{(k-1)})$ |
| Monotonicity | $(\text{Transistion\_width})_k < (0\ldots\ldots000001)_k$ |
| Missing Codes | $(\text{Transistion\_width})_k > (0\ldots\ldots000001)_k$ |
| DNL | $INL(i) - INL(i-1)$ |
| INL | $Max\left\|\nabla T_{step\ size} - \nu T_{step\ size}\right\|_k > \Delta.LSB$ |
| Offset | $INL(1)$ |
| Gain | $INL(2^N) - INL(1)$ |
| BIST Output (Pass/Fail) | OR (Monotonicity, Missing Codes, INL) |

**Proposed ADC BIST:**

1. INITIALIZE
2. APPLY linear ramp signal into A/D converter
3. COMPUTE digital output code ($d_k$) for N samples
4. APPLY $d_k$ to BIST module
5. WAIT until next digital code $d_k$,
   i. DO SUBTRACTION
6. WHILE transition is larger than one
   i. COMPUTE missing code error
7. end WHILE
8. WHILE sign bit -ve
   i. COMPUTE monotonicity fault
9. end WHILE
10. INITIALIZE DNL and INL
11. WHILE transition not 1LSB
    i. ENABLE INL factor, Ɛ
    ii. ENABLE INL computation
    iii. ENABLE DNL computation
12. end WHILE
13. FIND INL for each clk1
14. ADD INL and Ɛ for each clk1
15. STORE in register
16. COMPUTE DNL errors
17. DO SUBTRACTION of $INL_k$, $INL_{k-1}$
18. WHILE zero scale INL = 1
19. EQUATE offset error to INL
20. end WHILE
21. WHILE full scale INL = 1
22. EQUATE gain error to INL-offset
23. end WHILE
24. until counter reach 11….1, repeat step 5 to step 23.
25. When counter reach 11….1, enable EOT
26. END

(a)




(b)

Fig.5. Diagnosis static specifications of ADC (a) Pseudo code (b) Flow diagram

6. Do observation for transition error, missing code and monotonicity faults:
   a. If the adjacent digital code difference is zero, then no transition will occur, which has identified by ORing the individual bits of subtracted output $\tau_i$. Missing code fault has exposed when the subtracted output is greater than one.
   b. Negative adjacent code difference project monotonicity fault with logic high in a sign (MSB) bit
   c. Appearance of code transition generate the reset $\tau_i$
7. Enable the INL Computation counter with reset and clock signals
8. Enable the INL factor Ɛ, if the transition is not equal to 1LSB
9. Initialize DNL and INL to zero
10. Determine INL for each clock signal clk1 by adding the INL with the factor Ɛ
11. LSB bits represent the fractional variation of INL. Integer bit represents the full 1LSB variation in INL
12. Compute the DNL error from INL error
13. INL error at zero scale value represents the offset error
14. Calculate the gain effort by the difference of INL errors at full-scale value and zero-scale value
15. Repeat the steps until the counter reach 111….1
16. Enable End of Test (EOT) signal when the counter reaches the peak 111….1
17. Compute the test result from the observed static errors

## 5. Result Analysis

This section explains the simulation and analytical results of the proposed ramp based ADC BIST. The proposed ramp generator and TIQ comparator based ADCs are designed and simulated using CMOS 0.18µm technology with the supply voltage of 1.8V. The analog ramp generator is implemented using a self-biased current source with 10pF of capacitance and 100kHz of reset switching frequency. Monto Carlo simulation of simulation of ramp generator resulted a linear ramp signal generation with the peak to peak voltage of 0 V – 1.53V with the power consumption of 140.7µW as shown in Fig.6.

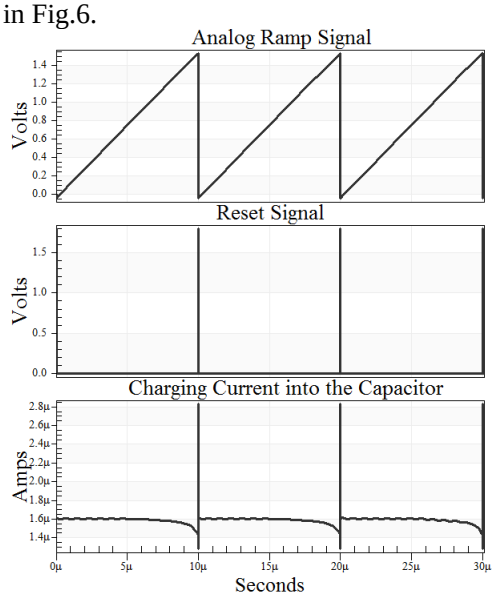



Fig.6: Output Response of Ramp Generator

The design of analog ramp generator has integrated with an ADC for linear test pattern generation. The test pattern is digital in nature. The fully digital ORA of ADC has been implemented in hardware description language as described in section 3.3. The ORA implementation was simulated and synthesized to verify and prove the effectiveness error measurement. The digital form of test pattern has been applied to the digital ORA to measure the nonlinearity's and non-idealities DNL, INL, offset, gain, missing codes, and monotonicity errors with all the possible combination of digital words. Fig.7 shows the output response of proposed BIST for the digital word applied through linear ramp based ADC. In the figure, the static errors

are measured by an ORA from the digital outputs of ADC. The ORA diagnosed the non-idealities based on the transition size of digital code obtained from ADC output. The initial state transition cuts into zero when the word length is increasing and that lead the circuit to have a transition error, missing codes, monotonicity, and INL error as shown in the figure. And from a calculated INL error the DNL has obtained with the reference of equation 15. Similarly, all other possible combinations of digital data sets are tested through a design ORA system. Simulation result of BIST show that the data conversion has no missing and monotonic codes. And, the non-linearity errors DNL and INL are measured as –0.21/0.16 and –0.13/+0.19, respectively for the 8-bit data conversion.

The proposed BIST schemes have compared with the existing methods presented in ref. [27], [26], [12] and [28] with the bit-resolution of 4, 8, and 12 bits, respectively. The test schemes are synthesized in ISE project navigator with the ambient temperature of 25$^{o}$C using Zynq-7000 family device of XC7Z020-1CLG484 package. Same setup has been used in the standard and proposed test schemes separately in the design and implementation of digital BIST at different resolutions. The advanced HDL synthesis results of testing schemes have observed and tabulated for the comparison. The test results are verified in Zynq-SDR kit through ISE iMPACT. Macro statistics of existing and proposed BIST schemes have obtained from the test reports generated during the advanced HDL synthesis. Logic block utilization factors listed in the macro statistics of 8-bit resolution ADC BISTs are observed and compared in Table.2 to show the area effected. Where, the utilization ratio of the logic blocks in the proposed test schemes has reduced about as half. Other parameters registered in Table.3 shows the effectiveness of proposed test structures. Timing constraints like frequency, offset, combinational path delay and logic and route delays have obtained from a timing report of detailed HDL synthesis with speed grade: -1. In frequency comparison, the proposed 4-bit ADC BIST gained a maximum operating frequency of 1.145GHz, which is 34.6% of greater testing speed than the existing methods implemented and compared in this paper. Also, the frequency comparison shows that as the resolution of the converter is increasing, the operating frequency of BIST has reduced gradually due to the logic and routing delay. The variations in the logic and routing delay with the effect of frequency variation are also shown in Table.3. In which, the proposed test schemes are taking less testing time when compared to the existing methods. The maximum path delays listed for different test schemes are also showing that the proposed systems are efficient in the BIST based ADC testing.

In the BIST structures, the input signals are organized and processed in digital blocks with the help of common clock control. In general, the digital circuits suffer from offset and skew, which lead logic circuit to get variation in a sampling interval, input routing delays, and wire interconnect delay. Also, it degrades the output stability. Comparative results of an offset time in the proposed techniques have reduced considerably. Net-skew of the BIST systems has recorded from PAR statistics and listed in Table.3. The reduced net length and tree segmentation, area efficient routing procedure in the layout design shrinks the skew value more than the value obtained in the synthesis. Slack time is another important constraint which requires to optimized for balancing the data path and clock tree path. The timing analyzer GUI was used to measure the worst case slack from the best case of achievable for the implemented built-in test systems. The worst case slack and best case achievable value of each system with different resolution has observed from PAR Auto time specific constraints generated by timing analyzer and reported in the table. Table.3 shows the comparison for the worst case slacks, in which the slack marked against the bit resolution of the ADC BISTs. The timing slack distribution of the critical path significantly reduced when compared with the best case achievable value. Since the best case achievable value is significant, the testing circuit provides linearly guaranteed a diagnosis of faults and supports for downscaling of the supply and bias voltage. In the proposed BIST schemes, the average Fan-out of Non-Clock Nets of the testing architecture is also considered and recorded from Xilinx post-mapping report file as in the table. The dynamic power response of the ORA has measured in xPower analysis tool for 100kHz of input frequency and tabulated for comparison. High switching activity enrolled in the digital ORA has increased the power consumption of proposed technique larger than some of the existing techniques.

The complete design of ADC BIST has been simulated to measure the static parametric errors present in the data conversion. The measured results of static parameters of the proposed ADC BIST is compared with the existing methods for accuracy. Table.4 shows the comparative results of ADC BISTs with static parameters, technology, type of signal generator, ADC and output response analyzing methods. The proposed ADC BIST has gained high accuracy with low non-linear faults. This is notably good achievement among the ADC BISTs.

## 6. Conclusion

This work presented a linear ramp generator and an output response analyzer for a mixed single ADC BIST application. A linear ramp signal generated in the first

section has been used to generate the digital output from a converter. The effect of non-idealities affecting the performance of ADC have been diagnosed in the output response analyzer. The design of digital ORA structure has implemented in HDL and verified in the logic simulator for static parameters of ADC. The simulation resulted the DNL and INL range for the 8-bit flash ADC as –0.21/0.16 and –0.13/+0.19, respectively. Also, the measurement of static error in digital ORA has good accuracy in comparison. Advanced HDL synthesis of digital ORAs are obtained in Xilinx ISE for the proposed ADC BIST with 4, 8, and 12-bits of resolution and compared with standard testing methods presented in ref. [12], [26], [27] & [28]. The comparison result authorized the effectiveness of the proposed BIST schemes positively over the available one. The major concentration involved in area overhead and feasibility of the proposed testing method is verified successfully through the comparative results. In comparison, the area utilized by the proposed testing schemes has reduced about 50% from the standard methods. The largest operating frequency of the proposed systems has increased about 34.6%. Also, the proposed structures have compared with the existing structures for the effectiveness in logic delay, routing delay and combinational path delay, which has an excellent continuation in performance. The comparison of timing constraints offset, skew and slack also have better results for linear processing and supply downscaling. Since the proposed techniques evaluated the converter through the digital output, the proposed BIST schemes opted for testing any ADC. Also the design has

***Acknowledgement***

The authors gratefully acknowledge UGC, New Delhi for providing financial support to carry out this research work under Rajiv Gandhi National Fellowship Scheme. One of the authors M.Senthil Sivakumar is thankful to UGC, New Delhi for the award Rajiv Gandhi National Fellowship. Grant number: F1-17.1/2016-17/RGNF-20510.

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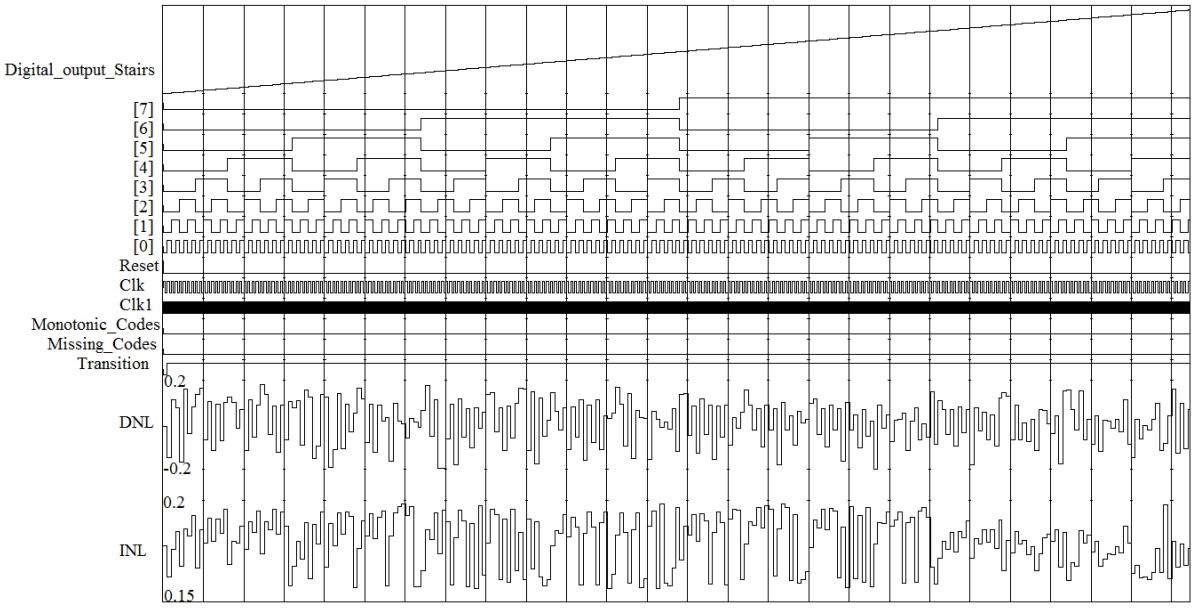


Fig.7: Output Response of Proposed 8-bit ADC BIST for Monotonicity, Missing codes, transition, INL and DNL

**Table.2:** *Comparison of logic blocks utilization*

| | Adder | Subtractor | Counter | Flip-Flops | 2:1 Mux |
|---|---|---|---|---|---|
| Ref.[27] | 2 | 4 | 2 | 48 | - |
| Ref.[26] | 2 | 4 | 2 | 40 | - |
| Ref.[12] | 3 | 4 | 3 | 56 | 8-bit – 1 |
| Ref.[28] | 2 | 1 | 2 | 16 | 2:1 – 16; 16:1 –1 |
| Proposed | 1 | 2 | - | 13 | 1 |

**Table.3:** *Comparative Results between the existing and proposed digital ORA modules of Analog to Digital Converter*

| Technique | No of Bits | Logic Delay (ns) | Route Delay (ns) | Max. Frequency (MHz) | Max. Combinational Path Delay (ns) | Max. ambient temp($^{o}$C) | Junction temp ($^{o}$C) | Worst case slack (ns) | Best Case Achievable (ns) | Fan-out | Net Skew (ns) | Dynamic Power (mW) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ref.[27] | 4 | 0.556 | 1.09 | 607.681 | 1.866 | 84.7 | 25.3 | 0.139 | 1.352 | 9 | 0 | 4 |
| | 8 | 0.865 | 1.269 | 468.702 | 2.476 | 84.7 | 25.3 | 0.186 | 2.089 | 18 | 0.166 | 4 |
| | 12 | 0.879 | 1.432 | 432.844 | 3.012 | 84.7 | 25.3 | 0.133 | 3.193 | 29 | 0.165 | 7 |
| Ref.[26] | 4 | 0.32 | 1.013 | 748.811 | 2.644 | 84.7 | 25.3 | 0.221 | 1.483 | 8 | 0.02 | 5 |
| | 8 | 0.865 | 1.269 | 468.702 | 2.648 | 84.7 | 25.3 | 0.344 | 2.383 | 18 | 0.02 | 6 |
| | 12 | 0.879 | 1.432 | 432.844 | 3.315 | 84.7 | 25.3 | 0.221 | 3.545 | 19 | 0.171 | 7 |
| Ref.[12] | 4 | 0.721 | 1.426 | 465.669 | 2.179 | 84.7 | 25.3 | 0.156 | 1.96 | 12 | 0.009 | 5 |
| | 8 | 0.882 | 1.685 | 389.59 | 2.861 | 84.7 | 25.3 | 0.129 | 2.654 | 19 | 0.025 | 7 |
| | 12 | 0.911 | 2.134 | 328.369 | 3.337 | 84.7 | 25.3 | 0.152 | 2.594 | 29 | 0.064 | 9 |
| Ref.[28] | 4 | 0.475 | 0.651 | 887.627 | 1.424 | 84.7 | 25.3 | 0.223 | 1.050 | 4 | 0 | 7 |
| | 8 | 0.475 | 1.061 | 651.041 | 1.942 | 84.7 | 25.3 | 0.352 | 1.849 | 7 | 0.018 | 11 |
| | 12 | 0.764 | 1.898 | 375.657 | 3.355 | 84.7 | 25.3 | 0.289 | 1.849 | 9 | 0.042 | 18 |
| Proposed | 4 | 0.373 | 0.5 | 1145.147 | 0.943 | 84.7 | 25.3 | 0.186 | 0.679 | 1 | 0 | 7 |
| | 8 | 0.373 | 0.527 | 1110.802 | 1.709 | 84.7 | 25.3 | 0.137 | 0.974 | 3 | 0.22 | 9 |
| | 12 | 0.416 | 0.728 | 873.858 | 1.805 | 84.7 | 25.3 | 0.144 | 0.976 | 3 | 0.088 | 14 |

**Table 4:** *Comparison results for 8-bit ADC BIST*

| Reference | Ref.[10] | Ref.[9] | Ref.[8] | Ref.[5] | Ref.[2] | This work |
|---|---|---|---|---|---|---|
| ADC resolution in bits | 8 | 8 | 8 | 8 | 8 | 8 |
| Technology in μm | 0.5 | - | - | 0.18 | - | 0.18 |
| Supply voltage in volts | 5 | 5 | - | 1.8 | - | 1.8 |
| Ramp Switching Frequency in kHz | 80 | - | 98 | - | - | 100 |
| DNL in LSB | 75 mV | –0.81/+0.74 | –0.4/+0.7 | –0.43/+0.45 | –0.72/ +0.75 | –0.21/ +0.16 |
| INL in LSB | 87.5 mV | –0.72/+0.5 | –0.3/+0.8 | –0.5/+0.5 | ±0.85 | –0.13/+0.19 |
| Signal Generator | Analog Ramp | Triangular Wave | Ramp Signal | Triangular Wave | Ramp Signal | Adaptive Ramp |
| ADC/Test Type | Flash ADC/Ramp Input | ADC/ Histogram Method | ADC/Non-Linear Polynomial Model | ADC/Time Tick Based BIST | ADC/Spectral Analysis | Flash ADC/Digital ORA |