EXPERIMENTAL STUDY AND SIMULATION OF ELECTROSTATIC DISCHARGE (ESD) IN PCB

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Abstract: *In electronic circuits, printed circuit boards (PCB) are ideal media for the propagation of disturbances of electrostatic discharge (ESD), and they act as antennas. It's therefore important to take account the electromagnetic compatibility for the design of the electronic circuits. This work demonstrates a simple experimental setup compared with simulation to measure ESD-induced voltage to trace on a printed circuit board when ESD current is injected directly onto a nearby electronic trace using ESD generator qualification of the equipment according to IEC 61000-4-2, and presents how the induced voltage can be affected by the physical structure of the PCB. The correlation between ESD-induced voltage and the method of connecting the PCB shall be discussed, as well as how the electronic trace spacing increase or decrease an ESD disturbance. These experimental results may provide guidance for a better design for ESD immunity.*

Key words: *Electrostatic discharge, Disturbance, PCB, Electronic traces, ESD Generator, IEC61000-4-2, Near-end crosstalk.*

1. Introduction.

A transfer of electric charge between bodies of different electrostatic potential in proximity to each other or through direct contact. This definition is observed as a high-voltage pulse that may cause damage or loss of functionality to susceptible devices. Although lightning differs in magnitude as high-voltage pulse, the term ESD is generally applied to events of lesser amperage and more specifically to events triggered by human beings.

The tight noise margin for the low voltage in high-speed digital circuits and physically high density and small product trend challenge engineers to pass the electrostatic discharge ESD standard test in IEC61000-4-2[1]. One of reasons that analysing ESD failure and solving ESD problems seem difficult is that there are many cases which cause ESD failure in system level. For example, ESD current is directly injected into signal traces, which destroys ICS (called hard-error), ESD transient field is electrically or magnetically coupled to traces, or direct field coupling to ICS occurs as well. These incidents often occur all together when ESD is injected into electronic devices.

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures, which protect against ESD damage also increase input leakage [2].

The keys to eliminating ESD damage are: (1) awareness of the sources of ESD voltages, and understanding the simple handling steps that will discharge potential voltages safely.

Once ESD is discharged to printed board system, the ESD current is distributed in the system. It is associated with a strong electromagnetic field that can couple into the electronic traces. There it induces voltages and currents. These voltages or currents may cause bit-errors, wrong instructions, or even a system crash [3, 4]. There is limit to solving ESD failure problems resulting out of the foregoing causes mentioned earlier with artwork design or ESD protection devices.

The aim of the present paper is to describe a method of calculating the induced transients due to ESD in PCB.

For this purpose, a Transmission Line coupling model is developed for determining the transient voltages induced within electronic traces by an impinging transient pulse generated by an ESD generator qualification of the equipment according to IEC 61000-4-2. The simulation method was characterized and compared with real measurements.

2. Experiment setup and device under test

The contact discharge mode of this test requires the pulse generator tip to be placed in contact with the device under test (first trace (aggressor)) and study the influence of the ESD noise on the second trace (victim) by computing the voltage induced in the victim trace. To realize this experiment, an ESD generator (TESEQ NSG437) was used and a positive ESD pulse was selected according to the standard test IEC61000-4-2. The aggressor trace is finally connected to coaxial cable containing ferrites, the other end of this latter is connected to the oscilloscope. An attenuator is placed in the middle of the coaxial cable to prevent damaging the oscilloscope. The bottom of the PCB and the ground strap are connected to a standard ground table. The

experimental setup is shown in Fig. 1. It's decomposed into several parts: ESD generator, PCB, and the elements outside of system (coaxial cable, oscilloscope, etc...).

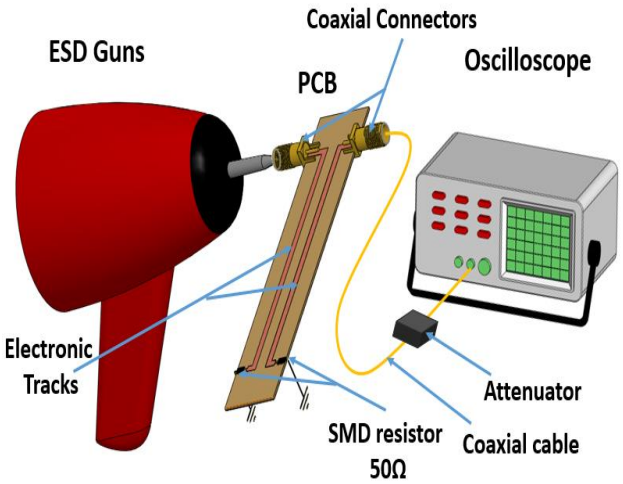

Fig. 1. Experimental setup for induced voltage measurement.

A. ESD pulse generator

The ESD generator can generate discharge pulses of 200 V to 15 kV to simulate the approach of a human body hand in specified patterns using the IEC of 61000-4-2 standard. Various setting options (polarity, pulse repetition, counters, etc...) are available on this generator [6].

There are four recommended stress levels shown on Table 1 for contact discharge (conducting surfaces) and air discharge (insulating surfaces). Many systems are specified to pass at the highest defined levels in the standard (8 kV for contact discharge, and 15 kV for air discharge).

In contact-discharge testing [7-12], the ESD generator was charged, the tip of the generator is placed against the object to be stressed and a relay inside the generator is closed, initiating the stress. IEC 61000-4-2 specifies a waveform for contact-level testing (Fig. 2). The current waveform is characterized by an initial current spike with a rise time of 0.7 to 1.0 ns and specified currents at 30 ns and 60 ns. The current levels scale tracearly with voltage from 2000 to 8000 volts. At 8 kV, the peak current is 30 amps and the 30 ns and 60 ns current levels are respectively 53, and 27 percent, of the peak current [1]. Those familiar with component level ESD testing will likely assume that contact discharge testing according to IEC 61000-4-2 standard is done similar to Human Body Model testing [20].

Table. 1. Conformity level for the IEC 61000-4-2 standard [1].

IEC 61000-4-2 Level	Max voltage Contact discharge (kV)	Max voltage Air discharge (kV)
1	2	2
2	4	4
3	6	8
4	8	15

A simulated ESD generator lumped circuit is supposed to synthesize the typical standard ESD waveform through ADS transient analysis [9, 10]. Refer to the model as shown in Fig. 3. C_1 = 150 pF and R_1 = 330 Ω are for fitting into a standard that simulates the charge and discharge in the human body mode (HBM). The values of C_2 and L_1 give the impedance of the ESD generator grounding wire and these two components are for shaping the second pulse of the current waveform. The resistor R_2 and the capacitor C_3 extracted from internal network are the parasitic resistor and capacitor for the ESD generator. Otherwise, different brands of ESD generators usually have considerable variation in these parameters. L_2 is regarded as the inductance between the ESD generator and its electrodes. This equivalent component determines the amplitude only at the second pulse. Oscilloscope internal impedance consists of C_4 and R_3; providing a main path that allows the discharge current to return to ground.

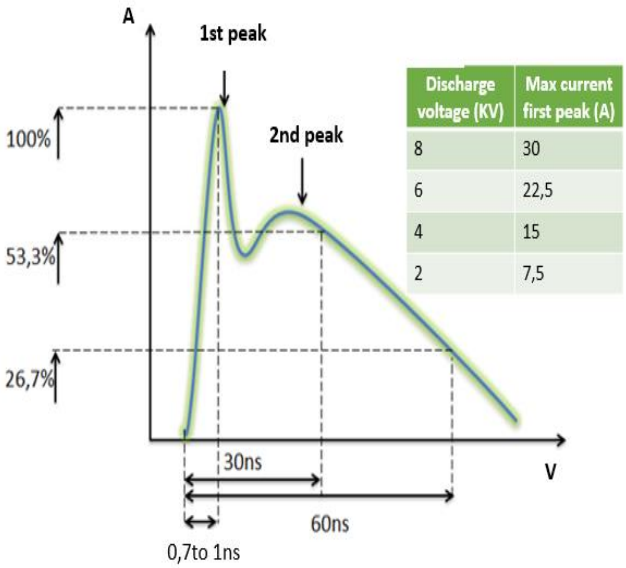

Fig. 2. Waveform required for the 61000-4-2 standard.

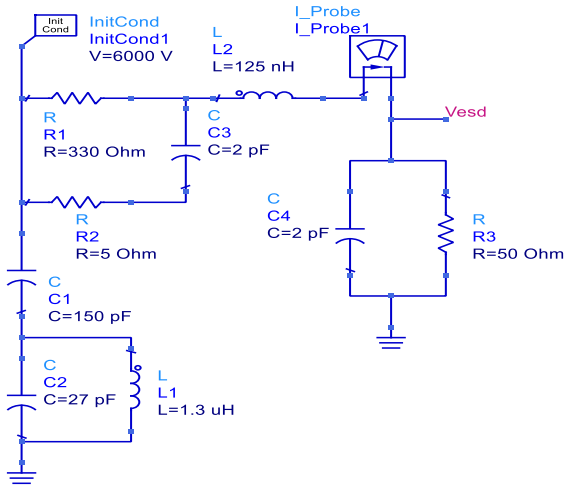

Fig. 3. Simplified model of the ESD generator [5].

B. Device under test (PCB)

The device under test for these measurements is composed of two parallel traces of a copper metal thin conductor. The first trace is the transmit trace and the second one is the disturbed trace. Both traces have characteristic impedance close to 50 Ω and a length of 80 mm placed above a ground plane, which is the return path of the current.

Figure 4 and Table 2 show the characteristics of microstrip traces used in this study. The dielectric material of PCB (Epoxy FR4) is the central element of this technology. It serves as both a mechanical support and support propagation of electromagnetic field by its electrical characteristics, which are the relative permittivity of the dielectric substrate (ε_r) and the thickness (H).

Table. 2. Parameters of the Microstrip trace.

Dielectric	Epoxy (FR4)
Thickness (H)	1,6 mm
dielectric constant	Ɛr = 4.6
Copper Thickness (T)	0.35 µm
Number of coats	2
width (W)	1.6

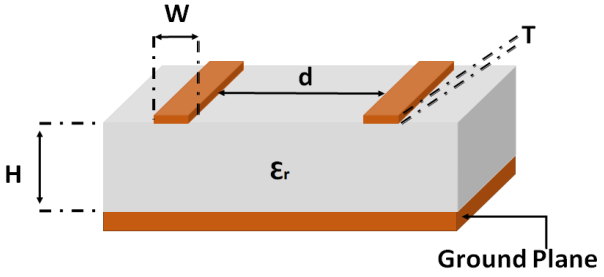

Fig. 4. Geometric parameters of the Microstrip line

All these microstrip traces are finished by a SMD (Surface Mounted Components) resistor of 50 Ω, then connected to a standard ground table for a good adaptation and eliminate the reflecting waves. This value of resistance has been chosen to characterize the propagation of an ESD stress along of trace. In the extremity of the trace (first edge of trace), the coaxial connectors SMA (Subminiature version A) loads was used which can be easily connected typically and to transmit the ESD pulse by direct contact on the aggressor trace and measuring induced voltage on the victim trace.

The microstrip traces system was modeled. The wiring and its conventional termination, called the "Line Impedance Stabilization Network" (LISN) further on, using the numerical simulation tool ADS [6], as shown in Figure 5.

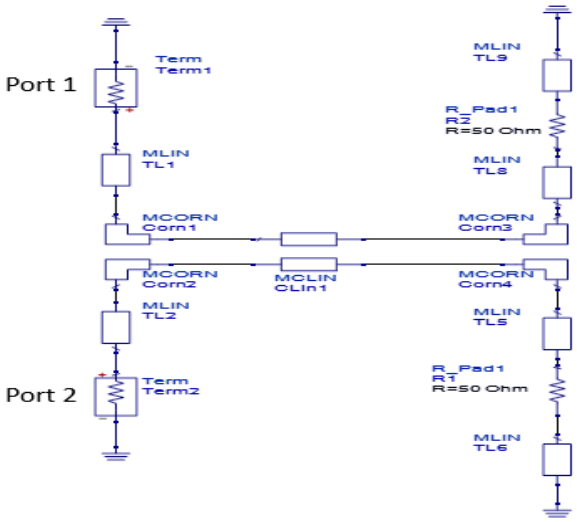

Fig. 5. Modeling of printed circuit board PCB.

Other cards PCB were made with similar characteristics but with other spacing between different traces (d = 0.5 mm, d = 1.5 mm and d = 3 mm) (Fig. 6) as well as how the electronic trace spacing increase or decrease an ESD disturbance.

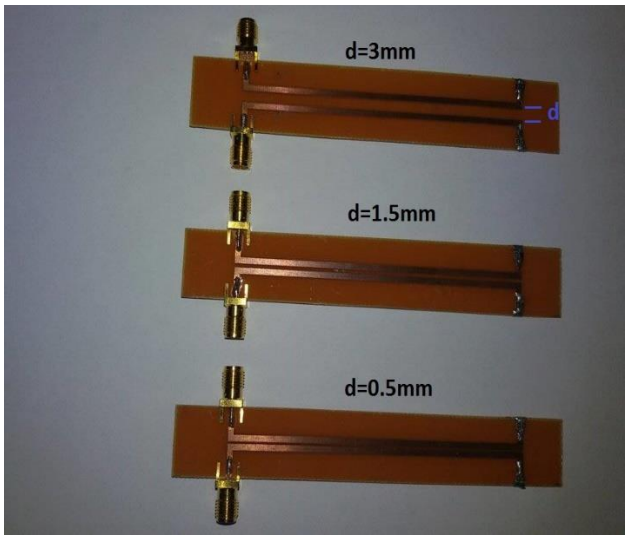

Fig. 6. PCB cards with different distances.

3. Experimental tests and simulations

Two transmission lines (TL_1, TL_2) run in parallel close by the coupling length is "L=80mm". The ESD pulse signal is appliqued at one transmission line (TL1) and the crosstalk voltages (V_{NEXT} (t), V_{FEXT} (t)) are observed at both ends of the victim trace (TL2) [13]. V_{NEXT} (t) and V_{FEXT} (t) are called the Near-end crosstalk and Far-end crosstalk, respectively. In this section, we use an experimental test compared with simulation to have optimal evaluation of ESD disturbance.

To obtain accurate ESD discharge waveform, a broadband digital oscilloscope MSO6104A (1GHz) was used to measure the induced ESD voltage. Because the digital oscilloscope (DSO) maximum input voltage is only 50 VDC, a 20dB attenuator was place near the DSO input port to prevent instrument damage. Port1 induces energy through Near-end crosstalk (NEXT) to Port2. Injecting 8 kV contact ESD energy into the designed PCB structure was performed through a 20 dB attenuator with only 1/10 voltage be detected.

A. Crosstalk coupling between PCB traces

Before starting the experiments, it is necessary to use the ADS software dedicated to microwave simulations in order to calculate crosstalk coupling. In this paper, the type of crosstalk coupling is Near-end crosstalk (NEXT).

In the frequency domain, figure 7 shows the coupling ESD noise computed between the two microstrip transmission traces with three distances : d = 0.5 mm, d = 1.5 mm and d = 3 mm, when a 1 V/m plane wave is applied on the device under test. All the loads of the line impedance stabilization network (LISN) are equal; all the components of the vector are almost equal. However, if the loads are different, the components of the vector may be themselves very different [12, 13].

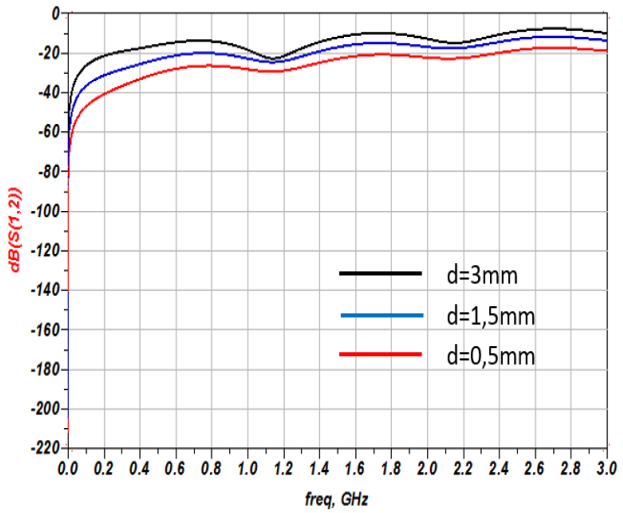

Fig. 7. Simulated result for S12 analysis of ADS.

Generally, the LISN is chosen with symmetric load values. All these results presented in this section were obtained with a 50 Ω loaded LISN, and the frequency is varied between 1 Hz and 3 GHz.

S-parameters S12 have been computed that the level of coupling is more serious according to the distance between microstrip traces and the aggressor's energy couples to the victim beginning from low frequency.

B. Results and discussions.

The voltage relation of the coupled traces had been described and the (V_{NEXT}) voltage can be calculated as: [11-13]

$$V_{NEXT}(t) = \frac{1}{4}\left(\frac{L_M}{L_S} + \frac{C_M}{C_M + C_S}\right) . \left(V_{in}(t) - V_{in}\left(t - 2t_f\right)\right) \quad (1)$$

Where: C_S and C_M represent respectively the self and mutual capacitances of micro strip traces per unit length. The L_S and L_M represent respectively the self and mutual inductances. The cross section of a coupled traces pair and the input voltage V_{in} (t) is applied at the aggressor trace and t_f is the time of flight along the coupled length is shown in Fig. 8.

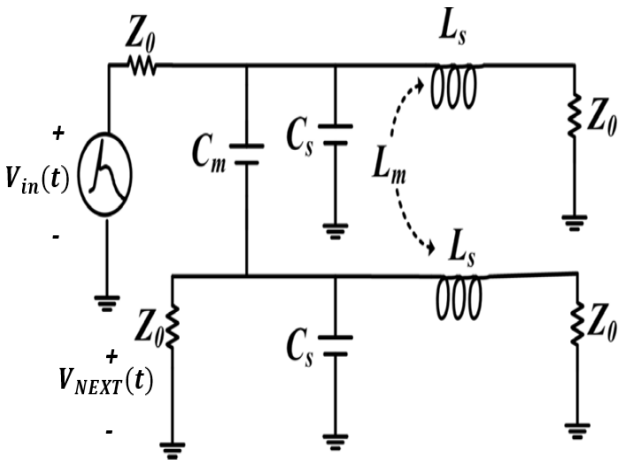

Fig. 8. Equivalent circuit of a coupled MTL pairs.

Injecting the ESD positive 8 kV using the contact mode according to IEC 1000-4-2 standard described in the first part delivered to several designed structures (d = 0.5 mm, d = 1.5 mm, d = 3 mm). The actual measurement and simulation results in the time domain are shown in Figs. 9, 10 and 11. It shows a good matching for the induced voltage waveform measured by the oscilloscope and simulated by ADS.

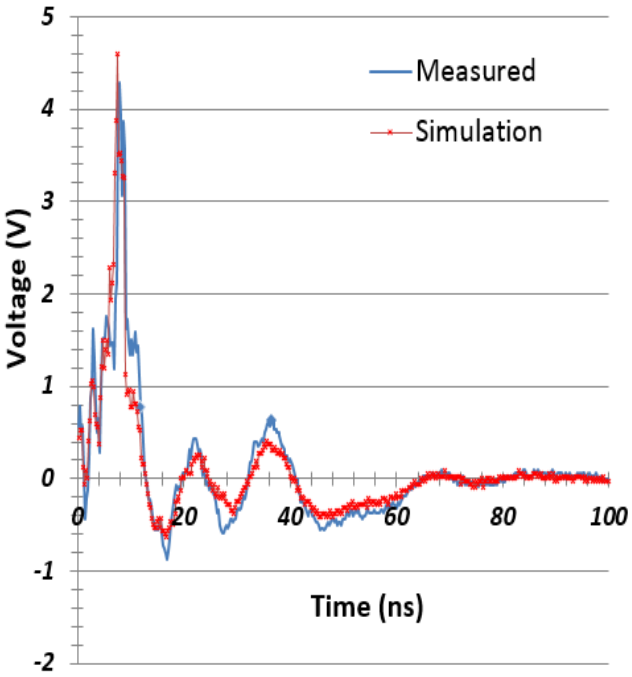

Fig. 9. Induced voltage in the victim trace for d = 0.5 mm.

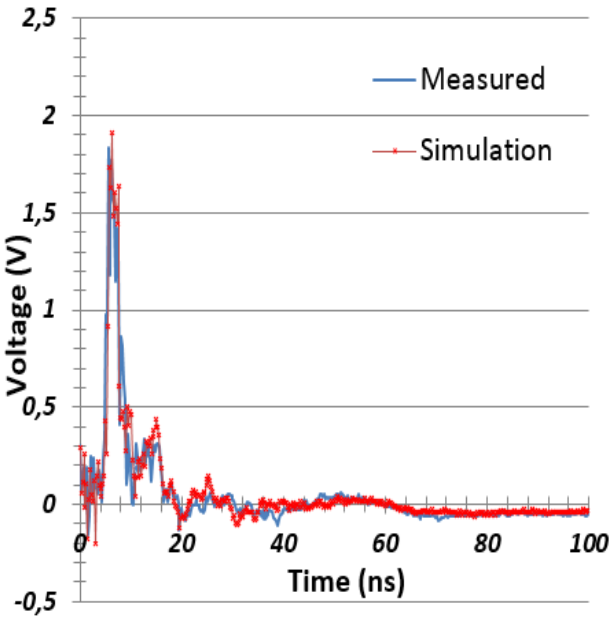

Fig. 10. Induced voltage in the victim trace for d = 1.5 mm.

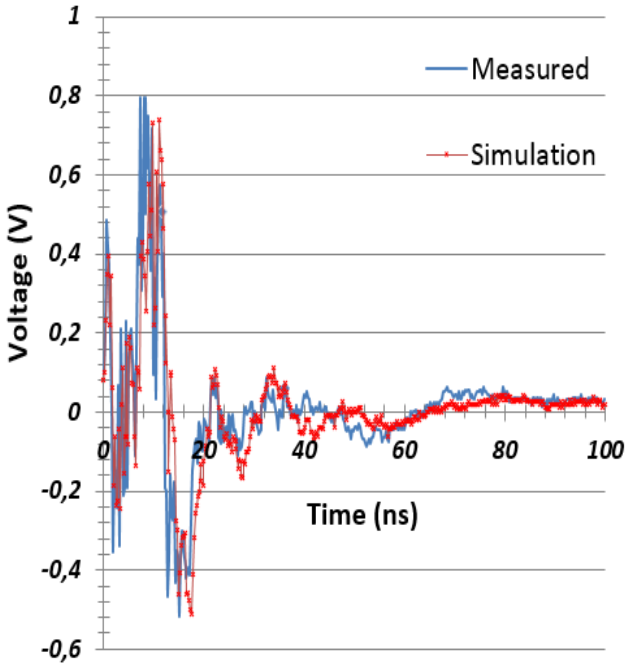

Fig. 11. Induced voltage in the victim trace for d = 3 mm.

By analyzing the results of these figures, the ESD generator produces the oscillations of induced voltage in the end of victim trace due to (NEXT). It shows that the PCB structure with d=3mm spacing has low NEXT as well as the structure of d=0.5 and d=1.5mm. In other words,

The peak amplitude of the induced voltage measured in victim trace is correspondingly decreases with increase in the spacing of the PCB traces.

The peak value of the induced voltage for a PCB increases from a maximum value, of 4.7 V for a traces spacing of d=0.5 mm, to 1.8 V for d=1.5mm and to 0.8V for d=3mm. This change in occurrence of the peak is due to smaller value of mutual inductance in case of shorter spacing as compared to long spacing between Microstrip traces, there is a reduction of ESD noise coupling depending on the distance between the Microstrip traces.

5. Conclusion

This study successfully implemented an equivalent ESD generator circuit model, according to the IEC61000-4-2 standard. An effective ESD measurement system compared with simulation was developed to analyze the ESD disturbance in printed circuit boards was another important contribution of this study.

This work demonstrates that a level of crosstalk coupling is more serious when two parallel Microstrip traces are close. In other words, the remoteness between lines is an effective solution for crosstalk reduction.

The measured and simulated results are perfectly

consistent. However, it would be a challenge to improve the full-wave model and to have exactly the same settings as the measurement.

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