LOW COST DESIGN OF A FPGA BASED DYNAMIC VOLTAGE CONTROLLER

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Abstract: *This paper presents a design of adaptive hysteresis band voltage controller based a dynamic voltage restorer (DVR) with minimum VA loading. The DVR is desirable to have mitigate the typical all voltage problems and improve stability of the system and its controller strategy is opted the adaptive hysteresis band voltage controller technique, to generate accurate injected voltages with optimum injected angle. Hence to mitigate the voltage problems under different considerations. The optimal angle at which series voltage has to be injected so minimum VA loading of DVR is evaluated by particle swarm optimization (PSO) and he results are verified with genetic algorithm (GA).The dynamic model of DVR has been adopted with adaptive hysteresis band voltage control by using MATLAB/Simulink. Experimental studies are carried out on single-phase FPGA based open loop dynamic voltage controller prototype to verify the proposed topology*

Key words: *Adaptive Hysteresis band voltage Control, Dynamic Voltage Restorer (DVR), Field Programmable Gate Array (FPGA), PWM,Praticle Swarm Optimazation (PSO) and Power Quality (PQ).*

1. Introduction

In present era increased usage of nonlinear loads, digital electronic controllers and switching apparatus in different working areas, these has led to many problems related to power quality [1-6], such as harmonics, Voltage flickers, Voltage sags [7], unbalanced voltages etc. Most of the sensitive loads require a pure sinusoidal supply voltage for proper functioning of load. To meet the requirements of power quality regulation [8-9], passive and active power filters are being used in conjunction with the conventional converters. Presently, active power filters (APFs) [10] are becoming more affordable due to cost reductions in power semiconductor devices, their auxiliary parts, and integrated digital control circuits. In addition, the APF also acts as a power-conditioning device which provides a cluster of multiple functions, such as harmonic filtering, damping, isolation and termination, load balancing, reactive-power control for power-factor correction and voltage regulation, voltage-flicker reduction, and/or their combinations. Now research focuses on use of the FACTS devices [11] to compensate for power-quality problems.

The paper presents a design of adaptive hysteresis band voltage control for a dynamic voltage restorer[12] [13], the dynamic voltage restorer DVR consists of one series voltage source converter (VSC) with DC-link C_{dc} as shown in Fig.1. The VSCs are 3-level (H-bridge) inverters which work independently and they work on the output feedback of adaptive hysteresis based Control. The adaptive hysteresis band PWM voltage control generates reference injected voltage signals with influence of system parameters and to generate switching signals to the converter [14-15] with proper switching times. Such that the accurate tracing bus voltages can be present as per requirement. The VSC are formed by the combination of reactor (L_{se}), resistor (R_{se}), ac filter capacitors (C_{se}) and three phase converters to prevent the flow of the power quality problems into the distribution system generated due to switching at each phase of PCC. Regulate the load voltages by DVR against voltage sags, swells and voltage harmonic content (v_h). The proposed methodology ensure that, even with the minimum VA loading. GA and PSO technique [16-19] are utilized as a tool for evaluating the optimum angle of injection voltage with constraints.Simulations on a power distribution system are carried out and results are presented. The test results verify that FPGA based OPEN loop dynamic voltage controller achieves good performance for mitigating the effects of voltage sag

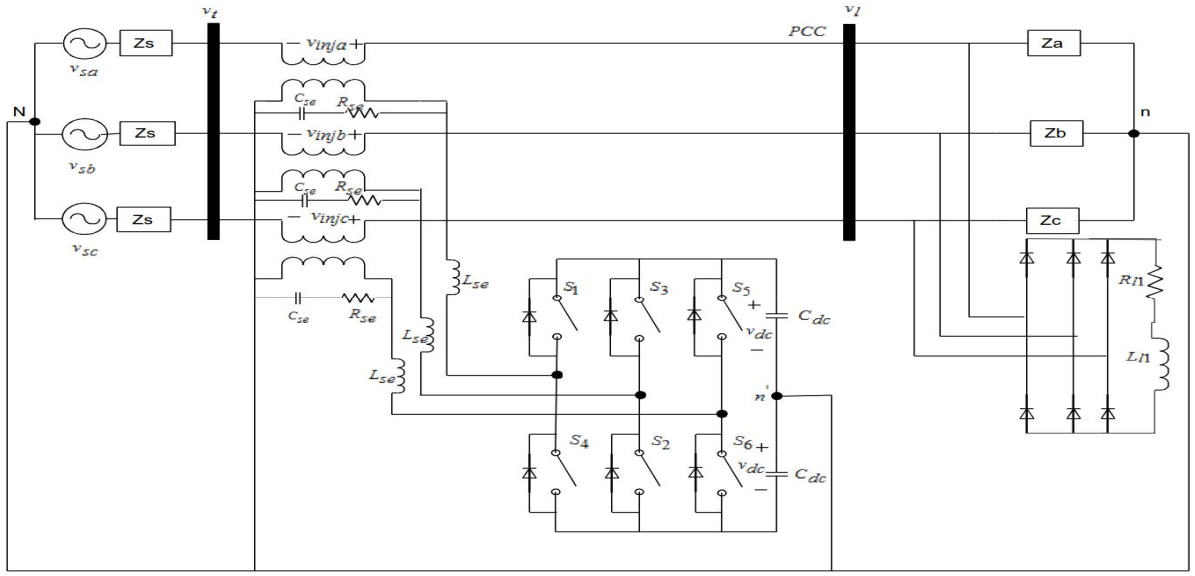


Fig.1. The single line diagram of a dynamic voltage regulator (DVR)

and suppressing the load voltage harmonics.

2. System Representation

A dynamic voltage restorer is a power electronic device, connected in series to the three phase system and to protect the loads from typical voltage problems in the source. The single line diagram of a dynamic voltage regulator in distribution system is shown in Fig. 1. In Fig.1 shows that the three phase source voltage is represented by V_{sabc}, R_S and L_S represent feeder resistance and inductance respectively. The three phase load voltage and injected voltages are represented by V_{labc} and V_{dvrinj} respectively. The DVR is realized by a voltage source converter (VSC) with DC capacitor voltage (Vdc) and power electronic switches S1, S2, S3, S4,S5 and S6. The L_{se} C_{se} is filter across the VSC and R_{se} is the copper losses of the connecting transformer. The operating principle of the DVR is to inject a voltage (V_{dvrinj}) of required magnitude and phase to compensate sag/swell and distortion in the terminal voltage and provide a balanced sinusoidal voltage (V_{labc}) at the load. The reference DVR voltage to be injected (V^*_{dvr}) is realized by switching S1, S2, S3, S4,S5 and S6 through hysteresis controller method. The single line equivalent circuit diagram of DVR is shown in Fig. 2. Hence to obtain the mathematical model of DVR, by applying the Kirchhoff laws in the above equivalent circuit.

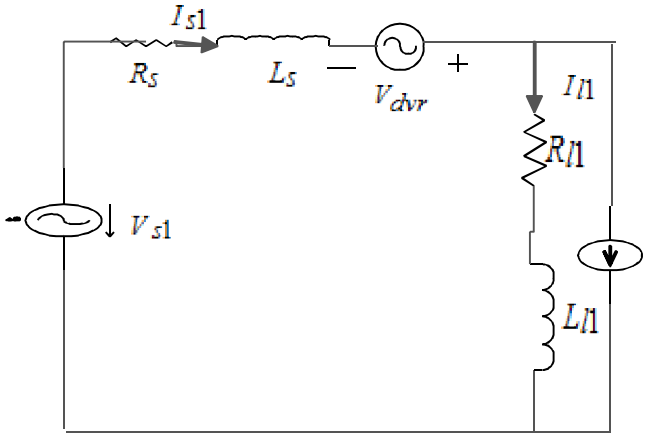


Fig .2. Single-line equivalent circuit diagram for DVR

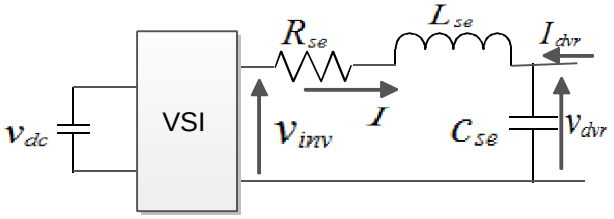


Fig .3. Equivalent diagram of series active power filter (SAPF)

$$L_{s1}\frac{di_s}{dt} = -R_{s1}is + V_{dvr} - V_{s1} + V_{l1} \qquad (1)$$

$$L_{l1}\frac{di_l}{dt} = -R_{l1}i_l + V_{l1} \quad (2)$$

The series active power filter (SAPF) system modeled following equations from fig.3.

$$\frac{dv_{dvr}}{dt} = \frac{1}{C_{se}}\left(I + I_{dvr}\right) \quad (3)$$

Where v_{inv} is the inverter-side voltage and to having paid attention to Fig.3 , the relations can be obtained.

$$v_{dvr} = -v_{inv} + L_{se}C_{se}\frac{dv_{dvr}^2}{dt} + R_{se}C_{se}\frac{dv_{dvr}}{dt} - L_{se}\left(\frac{di_{dvr}}{dt}\right) - R_{se}i_{dvr} \quad (4)$$

2.1 Rating of Dynamic Voltage Regulator

Fig. 4 shows that the phasor diagram of the operation of the DVR with sag. The V_{s1} and V_{l1} are source and load voltages at pre-sag at power factor $\cos\varphi_l$. When x=44% sag occurs at feeder the source voltages and load voltages are represented by V_{s1}^1 and V_{l1}^1. The injected angle and phase jump angle are represented by α and θ_l.

At during the sag period the input power at feeder can be expressed by

$$P_s = V_{s1}^1 I_{s1} = (1-x)V_{l1}I_{s1} \quad (5)$$

The load active power at feeder can be expressed by

$$P_l = V_{l1}I_{l1}\cos\phi_{l1} \quad (6)$$

We assuming lossless system equating both load power and input power, hence we get the input active source current component I_{s1}

$$(1-x)V_{l1}I_{s1} = V_{l1}I_{l1}\cos\phi_{l1} \quad (7)$$

$$I_{s1} = \left(\frac{I_{l1}\cos\phi_{l1}}{(1-x)}\right) \quad (8)$$

Now to find out DVR injected voltage (V_{dvr}) and angle of injection (α) expressions from the above phasor diagram

$$V_{dvr} = \sqrt{\left(V_{l1}{}^1\cos\theta_{l1} - V_{s1}^1\right)^2 + \left(V_{l1}{}^1\sin\theta_{l1}\right)^2} \quad (9)$$

$$\alpha = \tan^{-1}\left(\frac{V_{l1}{}^1\sin\theta_{l1}}{V_{l1}{}^1\cos\theta_{l1} - V_{s1}^1}\right) \quad (10)$$

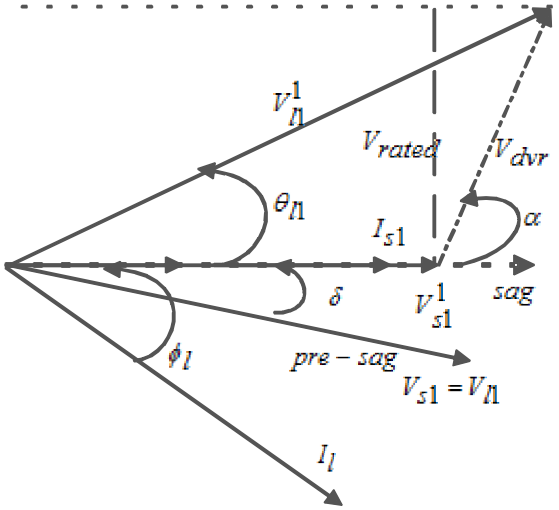


Fig. 4.Phasor diagram of the DVR with voltage sag.

Hence to calculating the total VA loading of dynamic voltage restorer during sag condition (S_{dvr})

$$S_{dvr} = V_{dvr} * I_{s1} = I_{s1}\sqrt{\left(V_{l1}{}^1\cos\theta_{l1} - \left(\frac{V_{l1}{}^1}{1-x}\right)\right)^2 + \left(V_{l1}{}^1\sin\theta_{l1}\right)^2} \quad (11)$$

From the equation (11) the total VA loading of DVR is controlled by varying phase jump angle (θ_{l1}) and remaining all the variables are system dependant. Therefore the objective function is the

$$\min imize - f(\theta_{l1}) = S_{DVR} = I_{s1}\sqrt{\left(V_{l1}{}^1\cos\theta_{l1} - \left(\frac{V_{l1}{}^1}{1-x}\right)\right)^2 + \left(V_{l1}{}^1\sin\theta_{l1}\right)^2} \quad (12)$$

Where subject to $-90° < \theta_{l1} < 90°$

$$0 < x < 1$$

3. Control scheme of dynamic voltage restorer

The generation of reference voltages for dynamic voltage restorer are given as

$$v_{dvr}{}^*(abc) = v_l^*(abc) - v_s(abc) \quad (13)$$

Where $v_l^*(abc)$ and $v_s(abc)$ are desired load voltages and sag/swell effected supply voltages in three phases. Then these reference injected voltages are compared with measured actual injected voltages

and generate the switch commands for VSI by using hysteresis voltage control methods.

Now the DVR is realized and adapted with a new control strategy related to hysteresis control method for the voltage source inverter. The main aim of the DVR is control section that must be able to derive the reference voltage waveforms with matching harmonic, sag and swell contents etc. in the supply voltage.

3.1Fixed Hysteresis band voltage controller

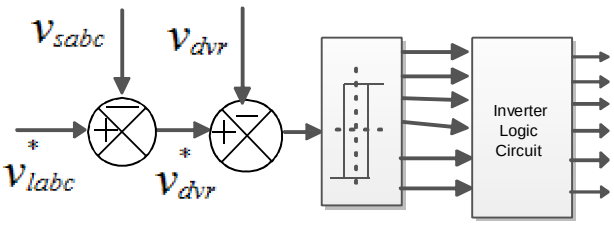


Fig .5. Fixed hysteresis band voltage controller

3.1.1 Fixed hysteresis band method:

The principle diagram of fixed hysteresis band voltage control is shown in fig.5 the hysteresis value band governs the inverter switching pattern in such a manner as to maintain the mean value of the control state at the required value. The instantaneous value of the output voltage is compared with the reference voltage, at the point when the sensed output signal strays from the reference by more than a prescribed value, the inverter is worked to diminish the deviation. This implies that switching happens at whatever points the output current crosses the values of HB. Where HB is the width of the hysteresis band.

If $V_{dvr} < (V^*_{dvr}$- HB), then upper switch S_1 will be OFF and lower switch S_4 will be ON in the phase "a" leg of inverter.

If $V_{dvr} > (V^*_{dvr}$+HB), then upper switch S_1 will be ON (P_1=1) and lower switch S_4 will be OFF (P_4= 0) in the phase "a" leg of inverter.

The switching pulses for the other remaining two legs can be derived. Thus the output wave is restricted to flow with in a channel of width (HB) that follows the reference waveform.

3.1.2 Fixed hysteresis band with derivative component:

Understanding of the system helps us to find the effective ways to make the output ripple under control irrespective of filter.

The equation shows that the rate of change of the output voltage gives a measure of inductance trapped energy at no load that charges over. At loading case this state gives a measure of the excess energy that prolongs the charging time outside the tolerance band. The state $\left(\frac{dv_{dvr}}{dt}\right)$ is an important signal that can be used to modify the control signal of the hysteresis controller. Hence the control signal should be composed of the derivative term in addition to the proportional of the output voltage signal of DVR. The control signal is given by:

$$V_{dvrnew} = V_{dvr} + \frac{dv_{dvr}}{dt} \tag{14}$$

This signal its reference determine the suitable switching instants so that the output remains in prescribed tolerance.

If $V_{dvrnew} < (V^*_{dvr}$- HB - $\frac{dv_{dvr}}{dt})$, then upper switch S_1 will be OFF and lower switch S_4 will be ON in the phase "a" leg of inverter

If $V_{dvrnew} < (V^*_{dvr}$+HB + $\frac{dv_{dvr}}{dt})$, then upper switch S_1 will be ON (P_1=1) and lower switch S_4 will be OFF (P_4= 0) in the phase "a" leg of inverter

3.1.3 Adaptive hysteresis voltage controller

The fixed hysteresis band is very simple and easy to implement, but it has the disadvantages of uncontrollable high switching frequency. This high frequency produces a great stress on the power transistor and induces important switching losses. An adaptive hysteresis band method [20] allows operation at nearly constant frequency and is usually performed by software which uses the system parameters.

Where $v^+_{advr}(t)$ and $v^-_{advr}(t)$ are the rising injected voltages and the falling voltage

$$\frac{dv^+_{advr}(t)}{dt} * t_1 - \frac{dv^*_{advr}(t)}{dt} * t_1 = 2HB \tag{15}$$

$$\frac{dv^-_{advr}(t)}{dt} * t_2 - \frac{dv^*_{advr}(t)}{dt} * t_2 = 2HB \tag{16}$$

$$f_c = \frac{1}{(t_1 + t_2)} \tag{17}$$

Where t_1,t_2 and f_c are switching intervals and frequency. By substituting equations (15), (16) and (17) in (4), the hysteresis band (HB) can be achieved as follow

$$HB = \frac{0.125 v_{dc}}{f_c R_{se} C_{se}} \left[1 - \frac{4(R_{se}C_{se})^2}{V_{dc}^{\ 2}} \left[\frac{v_a(t)}{R_{se}C_{se}} + \frac{dv^*_{advr}(t)}{dt} \right]^2 \right] \tag{18}$$

Where

$$v_a(t) = v^*_{dvr} + L_{se}C_{se}\frac{dv^2_{dvr}}{dt} - L_{se}\left(\frac{di_{dvr}}{dt}\right) - R_{se}i_{dvr} \qquad (19)$$

The adaptive HB should be derived instantaneously during each sample time to keep the switching frequency constant.

4. Minimization of objective function

4.1 Minimization of objective function by using genetic algorithm (GA)

GA has been used for global optimization of the parameters of control system, which are complex and difficult to solve using Ziegler's & Nichols's method, and conventional optimization methods. GA maintains a set of solutions called population and repeatedly modifies them. At each step, the GA selects individuals from the current population to be parents and uses them to produce the children for the next generation called Reproduction. Candidate solutions are usually represented as strings of fixed length, called chromosomes. A fitness or objective function is used to reflect the best of each member of the population. Given a random initial population, GA operates in cycles called generations.

Table: 1
Parameters and Values

Parameters	Values
No of dimensions	1
Population size:	100
No of Iteration:	50
C1 and C_2	1.04 & 0.04
Weighting factor w	0.9

The parameters of genetic algorithm are shown in table 1, now the function (12) is minimised by using genetic algorithm and find the optimal phase jump angle and minimum VA loading of DVR,measure angle of injection and injectec voltage. All these values are tabulated in table 2.

4.2 Optimization of objective function by using particle swarm optimization (PSO)

The PSO is best suited for optimizing non-smooth and non-linear functions as compared to evolutionary methods like genetic algorithms, Newton-based method etc.In this work the PSO was considered for minimizing the objective function. It is used to find a solution to an optimization problem in a search space and predict behaviour of all particles in the presence of various constraints and objectives.

Algorithm:

Step: 1 Initialization for each particle & each dimension

// initialize all particles' position and velocity

x_i= Rand (x_{min}; x_{max})

v_i = Rand (-v_{max}/2; v_{max}/2)

End for

// Initialize particle's best position

Pbest = x_i

// update the global best position

if f ($Pbest_i$) < f (Gbest) then Gbest = $Pbest_i$

End if

End for

Step:2 Particle Swarm Optimization (Global Best)

During the execution of PSO algorithm for every iteration of the particle, velocity of each particle is modified based on its current velocity and its distance from personal best position "pbest" and global best position "gbest" according to

$$v_i^{n+1} = w(n)* v_i^n + c_1* \text{rand1}( )*(pbest_i^n - x_i^n) + c_2* \text{rand2}( )*(gbest_i^n - x_i^n) \qquad (20)$$

After the velocity of each particle update is done, each particles move to its new positions according to

$$x_i^{n+1} = x_i^n + v_i^{n+1} \qquad (21)$$

Considering minimization function, the personal best ($pbest_i^n$) position at the next time step n+1, is calculated as

$$pbest_i^n = \begin{cases} pbest_i^n ; & \text{if } f(x_i^{n+1}) > pbest_i^n \\ x_i^{n+1} ; & \text{if } f(x_i^{n+1}) \le pbest_i^n \end{cases} \qquad (22)$$

Where 'f' is the fitness function or objective function. The global best $gbest_i^n$ position at time step is calculated as

$$gbest_i^n = \min(pbest_i^n) \qquad (23)$$

The parameters of particle swarm optimization are shown in table 1. Now the objective function (12) is optimized by using PSO and find the optimal phase jump angle and minimum VA loading of DVR, compare the both optimization results. Hence Minimization of VA loading and minimum phase jump angle of the DVR are obtained more by using the PSO than by using GA is shown in fig.6.

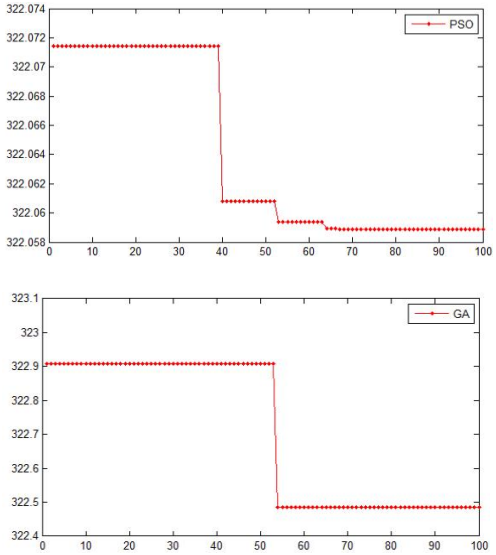


Fig.6.Global best vs No.of. Iterations

Table: 2
Comparison GA & PSO Values

Parameters	**With GA**	**With PSO**
VA loading	322.4857	322.0589
θ_l	0.0303	37.6991
$Vdvr_{inj}$	101.00	149.69
Angle of injection (α)	89.93	20.997

5. Simulation Results

The extensive case study of DVR proposed topologies, were obtained through simulation using SIMULINK/MATLAB environment.

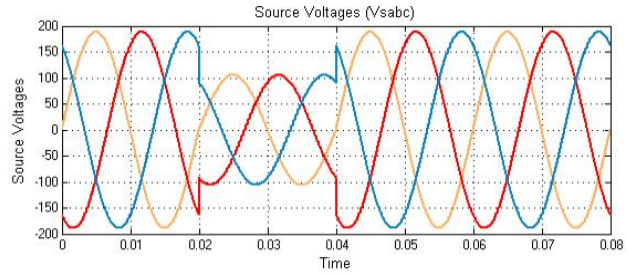
Table: 3
System parameters

Line-Voltage (V_{sa})	3-pahse 50HZ, $400/\sqrt{3}$ Volts
Feeder Impendence	1+3.14Ω
Series LC Filter -(L_{Se}) & (C_{se})	2.3mh & 80μF
Filter-Resistance (R_{se})	0.1Ω
Unbalanced Load	50+j31.4Ω,75+j31.4Ω and 100+j15.7Ω
Nonlinear Load	Three phase Diode with R-L load 300Ω and 50mh
Dc side capacitor (Cdc) & capacitor Voltage(V_{dc})	2000μF , 1040 V
V_{dcref}	1040
Three phase-Linear Transformer	4kva,230/230,50hz, 0.002pu,0.008p.u 1:1 ratio
Switching frequency(f_c)	10khz

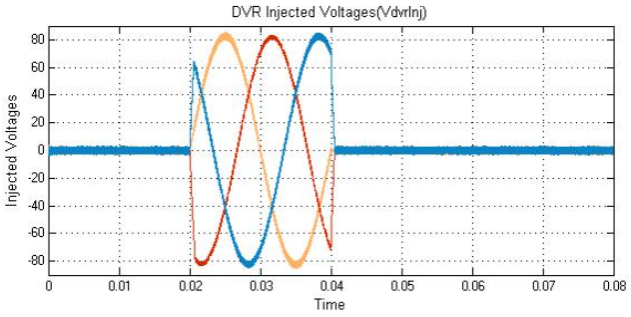
The system parameters which are given Table 3. The simulation results for both the hysteresis voltage controlled topology are presented in this section for better understanding and comparison between both the topologies.

Case1: Using fixed hysteresis voltage Controller

In this case it is assumed steady state condition the simulation time is taken as t=0 to t=0.08 sec with constant nonlinear load and unbalanced load. In case 1 applied a 44% of sag was considered in all phases of the terminal at the time of interval 0.02s to 0.04s and applied fixed hysteresis band voltage controller. The supply voltages and load voltages with 4.96% total harmonic distortions before compensation are same shown in Fig. 7 (a). Now to compensate the load voltages with help of DVR. Initially before compensation to generate the accurate reference voltages (V^*_{dvr}) by using equation (13) are shown in fig 7 (b).



(a)



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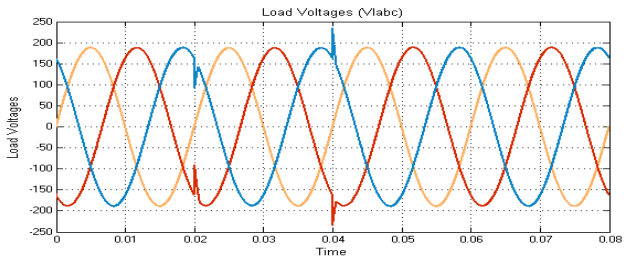

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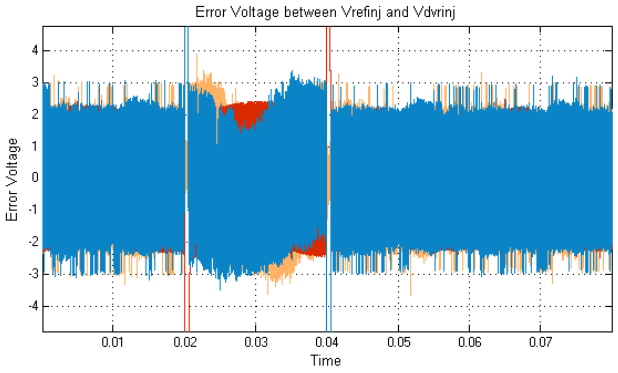

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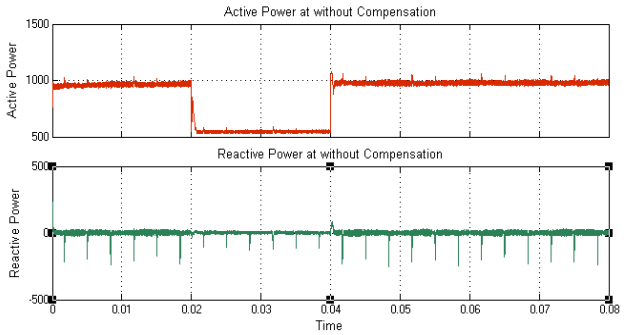

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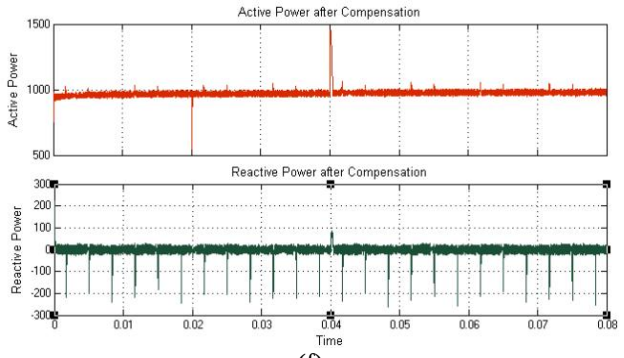


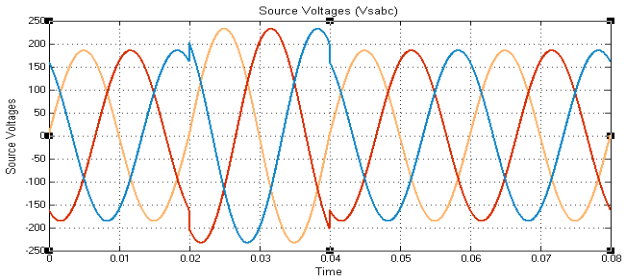
(f)

Fig.7 (a) Source voltages (V_{sabc}),7(b) Injected voltages (V_{dvrinj}), 7(c) Load voltages (V_{labc}), 7(d) Error between reference injected voltages and actual injected voltages 7(e) active and reactive power without compensation and 7(f) active and reactive power after compensation

The Instantaneous DVR injected voltages (V_{dvrinj}) are compared with reference DVR voltages (V^*_{dvr}) with fixed hysteresis band (HB=±6.5) value. At this point when the sensed output signal strays from the reference by more than a prescribed value, the inverter is worked to diminish the deviation. Hence the VSC injected the accurate injected voltages with minimum phase jump angle, and compensate load voltages becomes pure sinusoidal is shown fig.7(c) with 0.77% total harmonic distortions. After compensation active power also compensated during the sag intervals of time is shown in fig.7 (e). The main drawback of the fixed hysteresis voltage Controller is output current having small ripples due to constant hysteresis band, switching losses at converter are more and error between reference DVR voltages (V^*_{dvr}) and The Instantaneous DVR injected voltages (V_{dvrinj}) are more is shown fig.7(d), now to reduce these drawbacks with help of adaptive Hysteresis voltage controller. Finally the DVR Injects active power during sag interval of time and maintain constant active power are shown in fig 7(e) and 7(f).

Case2: DVR topology with adaptive hysteresis voltage Controller

In case 2 applied a 25% of swell was considered in all phases of the terminal at the time of interval 0.02s to 0.04s and applied adaptive hysteresis voltage controller.In adaptive hysteresis voltage controller the HB value can calculate at nearly constant switching frequency and is usually performed by software which uses the system parameters by using equation (18).



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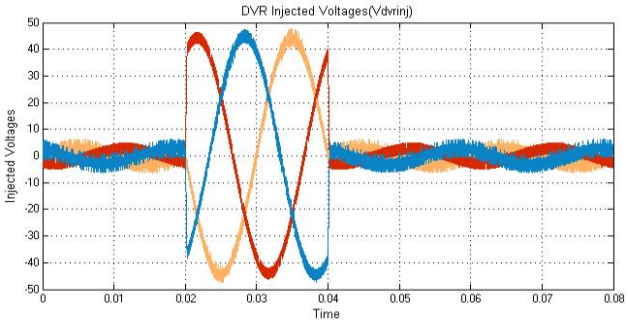

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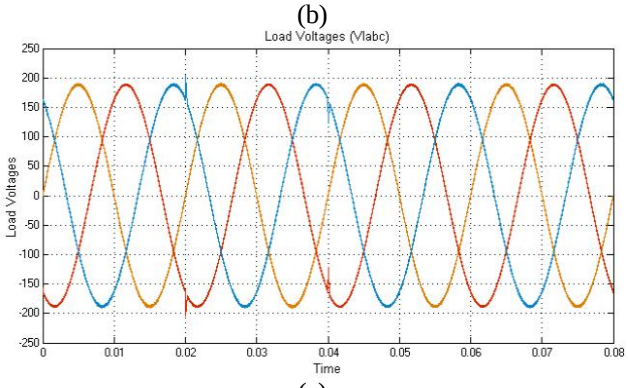

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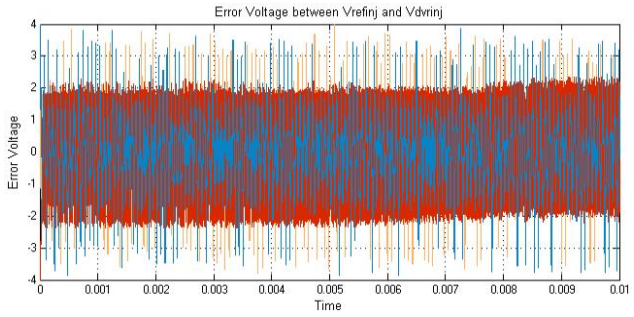

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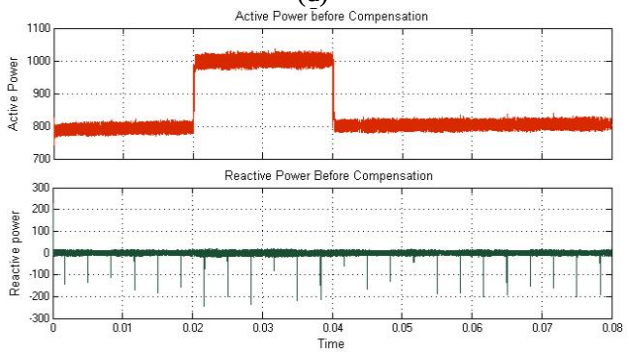

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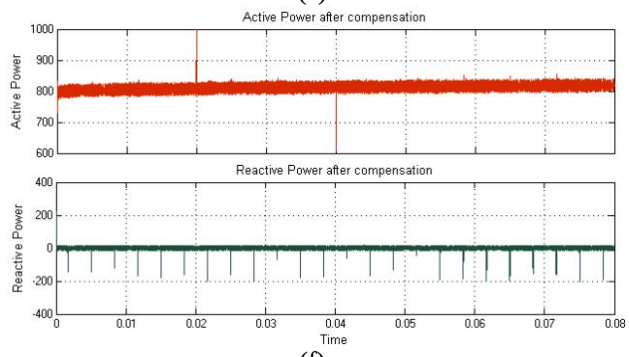


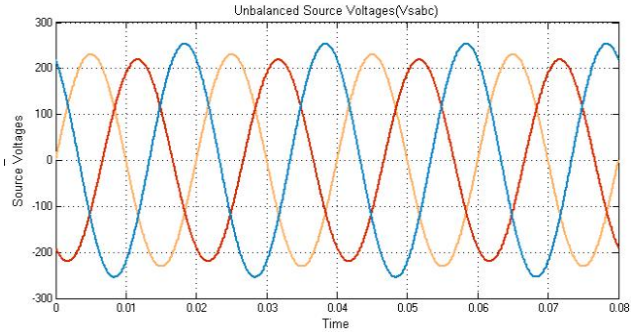
(f)

Fig.8 (a) Source voltages (V_{sabc}),8(b) Injected voltages (V_{dvrinj}), 8(c) Load voltages (V_{labc}), 8(d) Error between reference injected voltages and actual injected voltages 8(e) Active and reactive power before compensation and 8(f) Active and reactive power after compensation

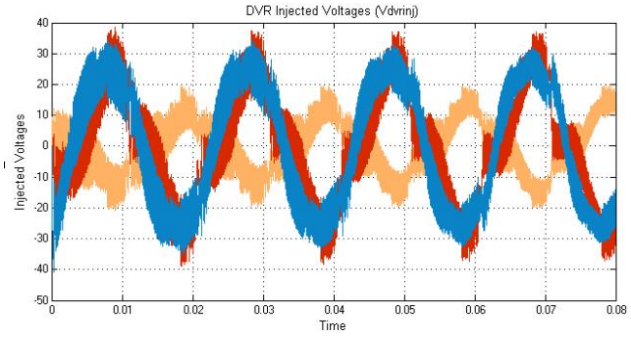
The modified The Instantaneous DVR injected voltages (V_{inj}) are compared with reference DVR voltages (V^{*}_{dvr}) at instantaneous hysteresis band (HB) with each sample time and constant switching frequency (f_c) technique. The modified Instantaneous DVR injected voltages (V_{dvrinj}) are shown fig.8 (b) and hence load voltages becomes pure sinusoidal without ripples shown in Fig.8 (c) with 0.27% total harmonic distortions. Finally by using adaptive hysteresis band voltage controller to Error between reference currents (V^{ref}_{dvr}) and Instantaneous injected currents (V_{inj}) are very less shown fig.8 (d) and active power and reactive power compensations are shown in fig.8(e) and 8(f)

Case3: Mitigate the Unbalanced voltages by using DVR topology with hysteresis voltage Controller

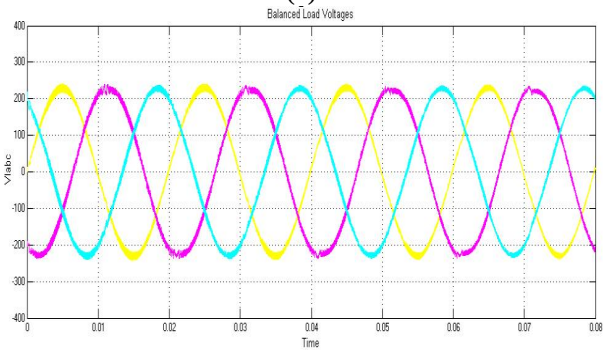
In case 3 applied unbalanced voltage all phases of the terminal at the time of interval 0s to 0.08s shown in fig.9 (a) and applied adaptive hysteresis voltage controller.



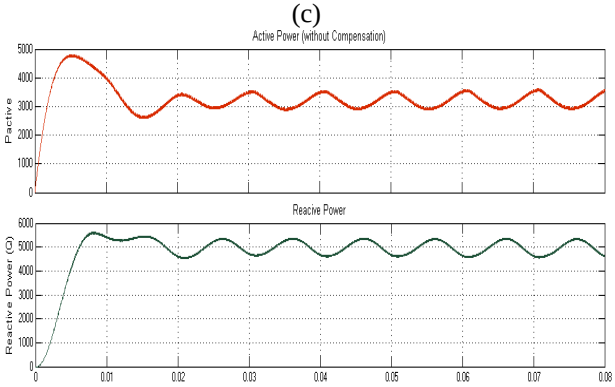
(a)



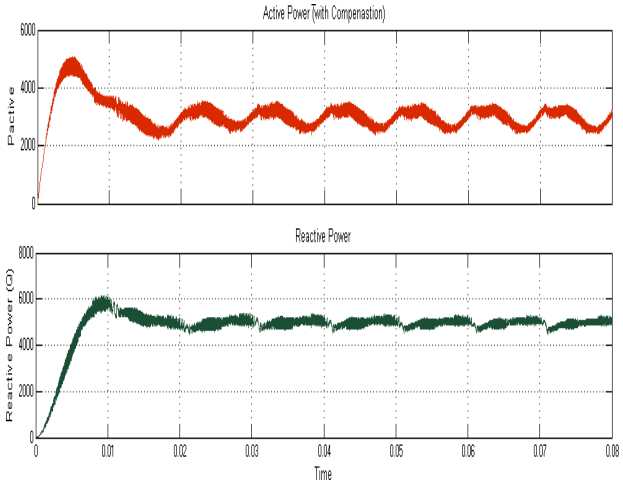
(b)



(c)



(d)



(e)

Fig.8 (a) Source voltages (V_{sabc}), 8(b) Injected voltages (V_{dvrinj}), 8(c) Load voltages (V_{labc}), 8(d) Active power and Reactive Power without compensation and 8(e) Active power and Reactive Power with compensation

The Instantaneous DVR injected voltages (V_{inj}) are compared with reference DVR voltages (V^*_{dvr}) at instantaneous hysteresis band (HB) with each sample time and constant switching frequency (f_c) technique. The Instantaneous DVR injected voltages (V_{dvrinj}) are shown fig.9 (b) and hence load voltages becomes pure sinusoidal without ripples shown in Fig.9 (c) with 1.07% total harmonic distortions. and active power and reactive power compensations are shown in fig.9(d) and 9(e).

6. Experimental Verification

The analog controllers have been implemented at the expense of high complexity and low efficiency due to larger number of components [21]. The capability of higher computational power and programmability enables the digital processors to be predominant in the implementation of complex algorithms. The signals are read through ADG467BR channel protectors respectively. Hence ADG467BR can with stand continuous voltage input from +40v to -40V. The output of channel protector given to the multiplexers ADG526ATE/883 and analog digital converters (AD1674TD). ADC reads such as source voltage (Vs), load voltage (V_l) and error voltage (Vinj). The error reference voltage waveform is obtained by subtracting source voltage and load voltage. The bipolar voltage output DAC (AD664TD-BIP) convert the digital to analog all voltage signals.

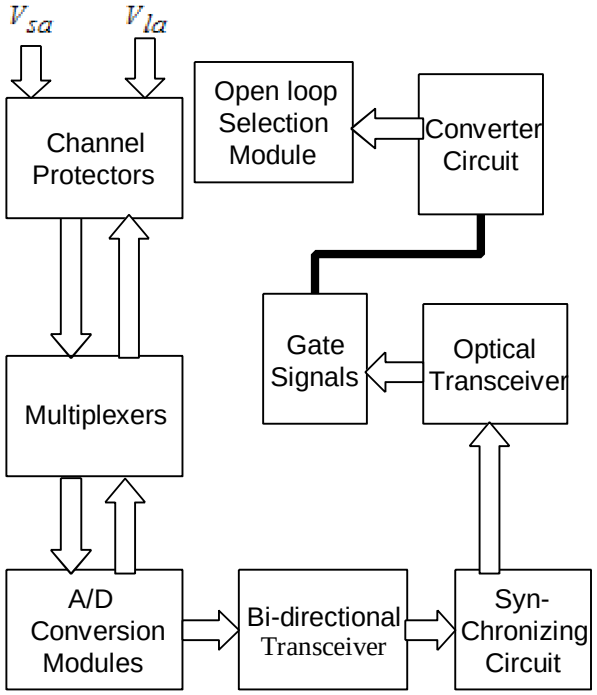


Fig.10.Modular block diagram of FPGA controller

Bidirectional transceiver PI74LPT are used to receive and send all low voltage signals data. These transceiver data reads XLINIX Q PRO II FPGA controller. The FPGA offers significant advantages over the other processors for high performance, low volume applications that can exploit customized bit-widths and massive instruction- level parallelism. Employing FPGA to Realize PWM strategies provides rapid prototyping [22-23], simple hardware and software design and higher switching frequency. The various logic blocks of the control algorithm were programmed using VHDL and synthesized into the FPGA and generating switching signals such a way to ensure that injected voltage is shown in modular block diagram in fig.10.

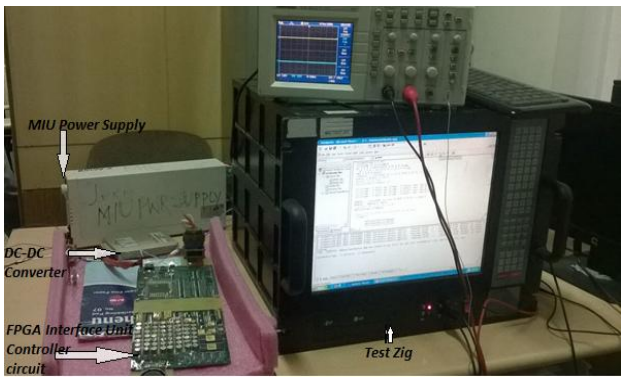


Fig .11.FPGA based dynamic voltage controller experimental set up

The experimental verification of the performance of open loop dynamic voltage controller in a single-phase distribution system with the switching schemes discussed above has been carried out in the laboratory using the prototype model of open loop dynamic voltage controller is shown in fig 11. The source voltage (V_{sa}) and load voltage (V_{la}) wave forms after compensation are shown in fig.12.a and b. The error (injected) voltage (V_{inj}) and FPGA based switching pluses (sw) are shown in fig.13 and 14.

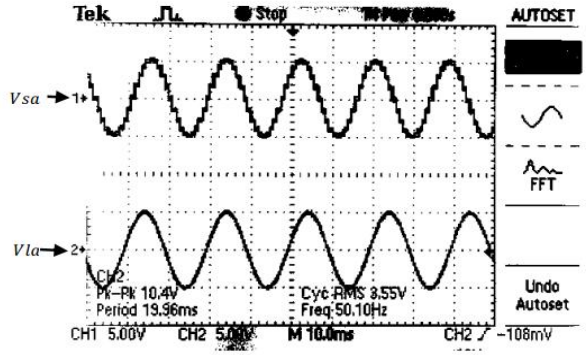


Fig 12.a. Unbalanced Single Phase Source Voltage Waveform in channel 1 and 12.b. after compensation balanced Single Phase Voltage Waveform in channel 2

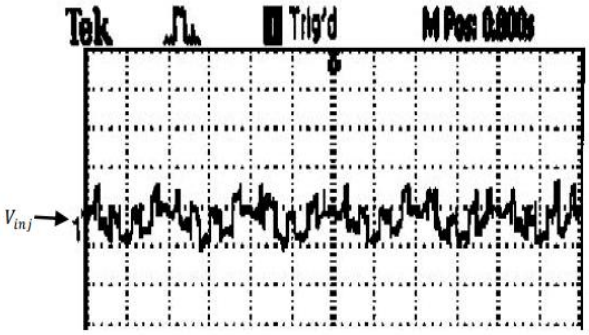


Fig.13.Error (injected) voltage signal wave-form in channel 1

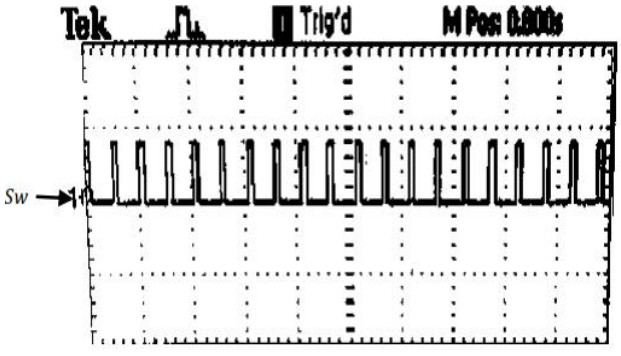


Fig.14.Switching pulse (Sw) from FPGA board in channel 1

7. Conclusions

This paper discuss the new concept of design FPGA based open loop dynamic voltage controller and The FPGA implementation involves voltage and current signal sensing, mathematical transformation, synchronization, control, and modulation. With the exception of the A/D converters and channel protectors, XLINIX Q PRO II FPGA controller hardware built on the comprising registers, adders, comparators, mux and multipliers. The test results verify that FPGA based OPEN loop dynamic voltage controller achieves good performance for suppressing the load voltage harmonics. And discuss another task the modelling and design the adaptive hysteresis voltage controller for dynamic voltage controller by using simulation. The adaptive hysteresis voltage controller generates accurate injected voltages with help of system parameters and having low error value between reference injected voltages and actual injected voltages, smooth and no ripples in source currents. Hence by using adaptive hysteresis voltage controller for dynamic voltage controller to mitigate the all typical voltage problems. Hence adaptive hysteresis current controller is proved best method comparatively fixed adaptive hysteresis current controller.

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