Single DC Source Multilevel Inverter Based on Switched Capacitor with Minimum Number of Switches for Medium Power Applications

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Abstract -In this paper, a single phase seven level inverter is presented with minimal number of switches using switched capacitor circuit based converter and H-bridge inverter. This configuration uses a single dc voltage source and this voltage is balanced across the capacitors to generate multilevel patterns. A basic multilevel inverter topology is developed with two capacitors and two diodes to form the basic cell which is combined further to develop the multilevel pattern. By utilizing the basic cell this paper introduces a modified multilevel inverter with a 7 and a 9 level configurations, compared to the existing capacitors this paper uses lesser number of diodes and capacitors which makes the inverter suitable for lower component count. To validate the performance of the inverter a hardware prototype has been built to evaluate the performance under different loads, the proposed inverter exhibits lower harmonic content around 2.5 % with lower component count.

Keywords: Multilevel inverter, Harmonics, Switched capacitor, voltage balancing, Multicarrier Pulse width modulation.

1. INTRODUCTION

Inverter is the basic device and an important device in power electronics for converting DC to AC. The output AC of single inverter contains more Total Harmonic Distortion, which multiplied component of fundamental frequency. This AC cannot be given directly to the devices used in high power application. Therefore, we go for multilevel inverter. Multilevel inverter is the power electronic device, which produce desired alternating voltage level output using multiple lower level DC voltages.

Multilevel inverter used for its advantages in producing higher voltages with low rating devices. It produces an increase number of voltage levels at the output voltage waveform. It reduces the total harmonic distortion in the output voltage waveform to produce highly defined AC. As it produces the higher levels in the output, the output waveform approximates to the sine waveform.

Multilevel inverter is the preferred choice for the industrial application in high voltage and for high power application. It has become the very important device in the section of high-power medium- voltage energy control. Due to its approximation in output, this AC supply can be directly given as input to the motor. It reduces stress on the insulation level of the motor. This inverter can produce high power output with medium voltage resources like batteries, super capacitor and solar panel.

Multilevel inverters are simply constructed with switches. There are two different types of topologies in multilevel inverters they are single source multilevel inverter and Multisource multilevel inverter. Diode clamped multilevel inverter, flying capacitors multilevel inverters are single source type, Even though Diode clamp and flying capacitor use single dc source, it is not suitable for the application in need of higher level output. Because it is difficult to calculate the number of switches, which increases as the level increases.

Diode clamp MLI use Banks of capacitor to clamp the voltages, Floating capacitor use series of capacitors to clamp the voltage. Cascaded H-bridge inverter use number of DC sources proportional to the number of levels. To reduce the count of capacitors and dc sources in the MLI circuit we go for switched capacitor circuit.

SC circuit is a combination of capacitor and switches. When a single dc source is connected to SC circuit, it works by moving charges in and out of capacitors when switches are opened and closed. So we can acquire the required value of clamped voltage to increase the number of levels in the output.

Multilevel converters are finding considerable attention in academia and industry as one of the preferred choices for high power conversion applications, such as traction drives, active filters, reactive power compensators, photovoltaic power conversion, uninterruptible power supplies, static compensators and flexible AC transmission systems.

In [1] They proposed a novel single dc source 7 level MLI with CPS-PWM technique for controlling switches, even though this system produce 7 level output with single dc source it uses a cascaded H-bridge inverter which may leads to high count in components and complexity in design. In this single dc has been utilized to create 7 levels by using switched capacitor. MLI convert is highly applicable high power industrial AC drives. Medium voltage drives needs low switching operation due to higher switching losses of semiconductor.

In [2] it proposed an optimal PWM based MLI for low power applications to reduce harmonics and low switching frequency. The drawback of the method is that it only applicable medium power drives. It also again use only

cascaded H-bridge inverter and all the output calculation are done in offline assuming steady sate properties. So, it may resistible to work during transient state. In [3] Topology of seven level inverter with PI controller has proposed to reduce switching and conduction losses. This MLI has a conventional cascaded H- bridge topology with DC source for each is replaced by PV cells. . In the recent past, attempts have been made to separate the level and polarity generation part to reduce the number of dc sources and power switches for a given number of voltage levels [4], [5],[6]. In most of proposed work following the commercial availability of power devices (MOSFETs and IGBTs) with a voltage rating up to 1.2 kV sufficing the low power applications, a rapid research on new MLI topologies with a pertinent focus on reducing the number of components count[7], [8],[9],[10].

On the other hand, many hybrid topologies combining the traditional and not so-traditional MLIs are found in the literature [11], [12]. In recent paper, they give an important to the switching capacitors in MLIs to give higher number of levels in the output, SCMLI have been gaining attention in recent years. This new family of MLI inherently solves the issue of unbalanced capacitor voltages that afflicts numerous classical topologies. It is also possible to produce higher number of voltage levels while employing a single voltage source unlike cascaded MLI [19].

The switched capacitor multilevel inverter can produce the desired sinusoidal voltage waveform and boost the input voltage without any bulky transformer. The multilevel inverters that use series–parallel connection of dc voltage source and capacitors attract more attention due to simple control for capacitor voltage control [13]. Because of the inherent voltage unbalancing of capacitors in the switched capacitor multilevel inverters, using complicated capacitor voltage balancing is necessary. Capacitor voltage balancing techniques will be more complex when higher number of voltage levels is produced at the output [14]. In order to mitigate this problem, the hybrid-source switched capacitor topologies can be used. By using this kind of inverter with fewer switching devices and simpler control methods, it is possible to achieve a greater number of voltage levels at the output [15].

In [16] the paper proposed Switched capacitor based 9 level inverter, its design comprises of cascading a three-level T-type neutral point inverter with a floating capacitor (FC) fed two-level converter unit. The switched capacitor unit has been connected on the second unit of the design to fed two level inverter. This work additionally needs two line frequency switches appended across the dc links. There also a Hybrid Multilevel inverter with switched capacitor unit. In this SC unit, there are many capacitors which lead to increase voltage drop across each one [17].

To maintain the voltage balance across the capacitors, we can add voltage balance circuit to the MLIs. However using these additional features make it only applicable for low output voltages resulting in increased harmonics and switching frequency [18]. To overcome the issue in adding voltage balance circuits, the paper presented self balanced MLI based on switched capacitance circuit. However this method leads to the usage of more components in self balancing [20]. To reduces the number of DC sources in producing multilevel output. The DC sources can be replaced with capacitors to self balance the voltage and to produce multilevel in the output [21]. The MLIs with reduced components and increase levels is always found to be successful and it has to be modified with respect to the application. In this paper, we proposed a 7 level inverter which mainly consist of two parts switched capacitor circuit and an H-bridge inverter. The switched capacitor circuit divides the input voltage to apply it across the loads through the IGBT switches. The multi-carrier pulse width modulation method had used in giving control signals to the power electronic switches.

This system is designed and simulated in plexim software. In addition, the output voltage is analyzed for harmonic contents. In the subsequent section, the literature survey regarding MLIs is described. Then the proposed inverter circuit and its working are illustrated in section 2. Section 3 explains the multi-carrier PWM method applied in this work. Section 4 discusses the implementation of the proposed work along with the results and Section 5 discusses the conclusion of the proposed work.

2. PROPOSED 7-LEVEL INVERTER

The most important shortcomings of the conventional inverters are the increased number of switches and voltage sources. In this paper, to reduce the number of switches and voltage source requirements, a novel 7-level inverter with switched capacitor circuit based converter is presented. This switched capacitor circuit is able to reduce the voltage level by dividing the voltage between the capacitors. The switched capacitor circuit contains two capacitors with equal capacitance value and two diodes.

2.1 Configuration of proposed circuit

The circuit diagram of proposed inverter is shown in Figure 1. Figure 2, 3,4 shows the mode of operation as depicted in Table 1. Figure 5 shows the switched capacitor circuit. This topology consists of only one dc voltage source, seven IGBTs, four diodes and four capacitors with equal capacitance values. The switching combinations and the corresponding output voltage levels are depicted in Table 1. The connection of switches $S_4 - S_7$ represents the H-bridge inverter configuration. The switches S_2 and S_3 are used to turn on and turn off the switched capacitor circuits. The capacitors in the switched capacitor conducts only when the switches to which they are connected, are triggered. When the dc voltage is applied at the input terminal, it is obtained as a dc voltage with the same value or a decreased value at the input terminals of the H - bridge inverter. The inverter generates the AC voltage waveform across the load terminals.

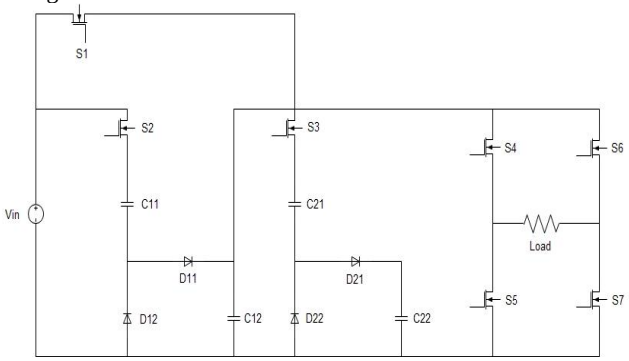

Figure 1: Circuit diagram of proposed configuration

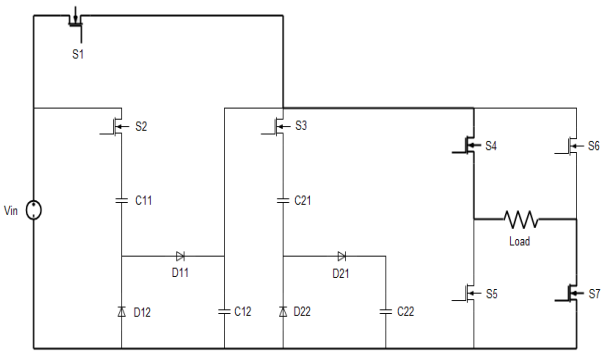

Figure 2: Mode 1 operation

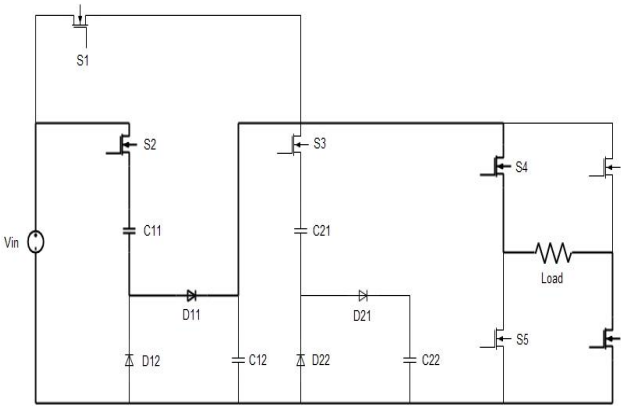

Figure 3:Mode 2 operation

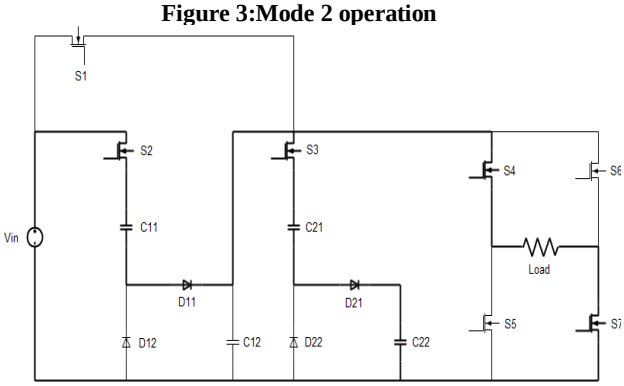

Figure 4: Mode 3 operation

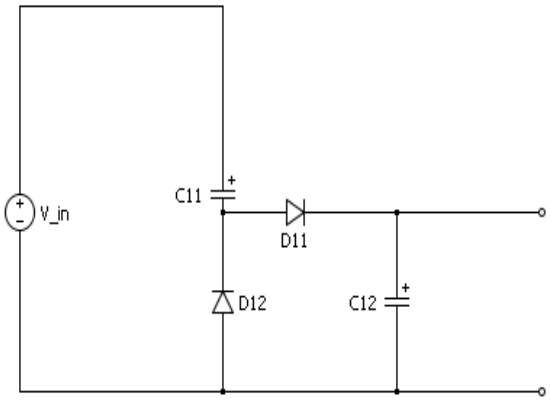

Figure 5: Switched capacitor circuit

Table 1: Switching combinations and corresponding output voltage level

Case	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Voltage
1	1	0	0	1	0	0	1	$+V_{in}$
2	0	1	0	1	0	0	1	$+V_{in}/2$
3	0	1	1	1	0	0	1	$+V_{in}/4$
4	0	0	0	1	0	0	1	0
5	0	1	1	0	1	1	0	$-V_{in}/4$
6	0	1	0	0	1	1	0	$-V_{in}/2$
7	1	0	0	0	1	1	0	$-V_{in}$

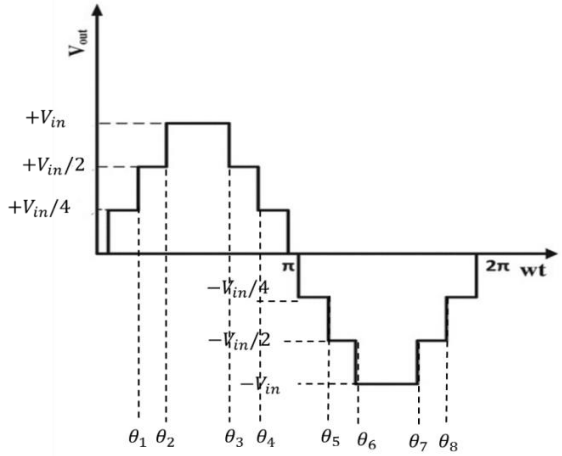

Figure 6:Seven level output voltage with phase angle

In the circuit shown in figure 5, the two capacitors, C_{11} and C_{12} have equal capacitance values and they are connected in series. When the input dc voltage source V_{in} is applied to the circuit, the voltage V_{in} is divided into two equal voltages across the capacitors. The voltage appeared across the capacitors C_{11} and C_{12} are same and equal to $V_{in}/2$. Considering Figure 1, there are seven cases of operation to produce the 7-level output voltage. Figure 2, 3 and 4 represents the mode 1, 2 and 3 operations respectively. In case 1, switch S_1 of the converter is switched ON by the control signal. Similarly, S_4 and S_7 are kept ON in the inverter side.In this case, the output voltage is positive and the value is same as the value of applied input voltage. When S_5 and S_6 are switched ON and S_4 and S_7 are switched off, the negative voltage is obtained (case 7). In case 2, switch S_2 is switched ON and the switched capacitor circuit now comes into working. The capacitors C_{11} and C_{12} start to conduct and the voltage is divided into two equal voltages. Hence the output across the capacitor $C_{12}$is half of the applied voltage. Then this voltage is obtained as the positive voltage at the output of the inverter when the switches S_4 and S_7 are kept ON and the negative of this voltage is obtained at the inverter when S_5 and S_6 are ON (case 6).In case 3, switch S_2 and S_3 are switched ON and the switched capacitor circuit following the switch

S_5also comes into working. The output voltage capacitor C_{12} is again divided into two equal voltages across the capacitors C_{21} and C_{22}. Now the output across the capacitor C_{22} is half of the output voltage across capacitorC_{12}. Hence the value of output voltage is $(1/4)^{th}$ of the input voltage. Then this voltage is obtained as the positive voltage at the output of the inverter when the switches S_4 and S_7 are kept ON and the negative of this voltage is obtained at the inverter when S_5 and S_6 are ON (case 5). In case 4, when switches S_1, S_2 and S_3 are switched off, the output voltage is zero disregarding the switching combinations of inverter circuit. Thus, the ON state of the switches S_4 and S_7 will produce the positive half cycle of the output voltage and the ON state of the switches S_5 and S_6 will produce the negative half cycle of the output voltage. Thus the seven levels of voltage are obtained at the output waveform which are $+V_{in}$, $+V_{in}/2$, $+V_{in}/4$, 0, $-V_{in}/4$, $-V_{in}/2$, and $-V_{in}$.By adding the number of basic cells, the levels can be increased further.

3. PWM TECHNIQUE

3.1 MULTICARRIER PULSE WIDTH MODULATION TECHNIQUE

Multicarrier phase disposition PWM technique is used to produce the gating signals for the switches. In this PWM technique, the sinusoidal reference signal with fundamental frequency is compared with the multiple triangular carrier signals. In order to generate the seven level voltages at the inverter output, six triangular carrier waves with higher frequency are used [22]. All the three carrier signals have different offset voltages but they are in phase with each other and with the reference signal. The allowable frequency ratio between carrier wave and sine wave is 40 [23]. In this PWM, by comparing the six carrier waves with the reference sine wave, three signals are generated and they are given as control pulses to the switches of the inverter. For one cycle of the fundamental frequency, the proposed multilevel inverter operates through seven modes. Figure 6 depicts the output voltage waveform with the amplitude values and phase angles for one cycle. The proposed inverter operates in seven cases as shown in table 1 and the respective phase angles are listed in table 2. The multicarrier SPWM with three triangular carrier signals and a sinusoidal reference wave is shown in figure 7. From the figure it is observed that the carrier signal has the higher frequency and the reference wave has the fundamental frequency.

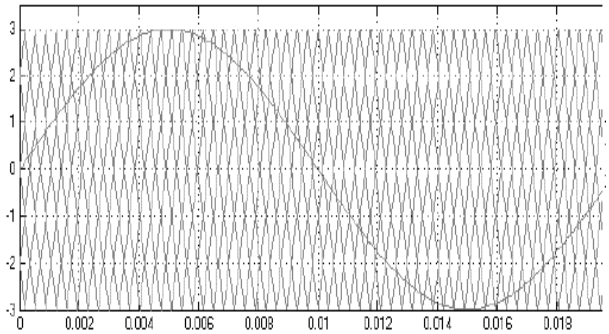

Figure 7: Multicarrier SPWM technique

Table 2: 7-level operation and respective phase angles

Case	Phase angle interval
Case 1	$\theta_2 < \omega t \leq \theta_3$
Case 2	$\theta_1 < \omega t \leq \theta_2$and $\theta_3 < \omega t \leq \theta_4$
Case 3	$0 < \omega t \leq \theta_1$and $\theta_4 < \omega t \leq \pi$
Case 4	$\omega t = 0, \pi, 2\pi$
Case 5	$\pi < \omega t \leq \theta_5$ and $\theta_8 < \omega t \leq 2\pi$
Case 6	$\theta_5 < \omega t \leq \theta_6$and $\theta_7 < \omega t \leq \theta_8$
Case 7	$\theta_6 < \omega t \leq \theta_7$

The phase angle, ωt, varies according to the modulation index, $M.I$,which is given in eqn (1).

$$M.I = \frac{2A_{ref}}{A_{carr}(m-1)} \qquad (1)$$

Where $A_{carr}$is the peak-to-peak value of the triangular wave, $A_{ref}$is the amplitude of the sinusoidal reference wave and m is the number of voltage levelto be generated in the half-cycle. To produce seven levels, the value of m is equal to 4.From the PWM technique, the harmonicanalysiscan be accomplished. Theoutput voltage obtained from the proposed inverter can be given as in equation (2) [24]. The fundamental components of harmonic content and output voltage are investigated using the Fourier series expression.

$$v_{out}(\theta) = A_0 + \sum_{n=1}^{\infty}(A_n \cos n\theta + B_n \sin n\theta) \qquad (2)$$

If there are N pulses per quarter period, and it is an odd number, coefficients$B_n$would be zero, where n isan even number. Hence eqn(2) can be rewritten as

$$v_{out}(\theta) = \sum_{n=1,3,\ldots}^{\infty}(A_n \cos n\theta) \qquad (3)$$

The Fourier series coefficient, A_n can be expressed as,

$$A_n = -\frac{2V_{in}}{n\pi}\sum_{p=0}^{P}\sum_{i=1}^{4}\left\{(-1)^{int(i/2)}sin\left(n\alpha_{p+i}\right)\right\} \qquad (4)$$

Where p is a pulse number and α is the phase displacementangle.In the proposed topology, only six switches are employed and hence the switching losses and conduction loss are low.

3.2 Capacitor Calculation and Ripple Loss Analysis

During the discharge phase of the two capacitors connected in parallel or in series with the voltage source the voltage ripples occur. These ripples must be essentially controlled that it should not exceed 10% of the capacitors' maximum voltages [22]. The level to which the voltage oscillates is determined from the load type. The capacitors in

the SC circuit are merged to produce the voltages at the point V_{in} and $V_{in}/2$ and hence the circuit generates the output voltage levels $V_{in}/2$ and V_{in}, Similarly the biggest discharging gap arises in the negative half cycle during the generation of voltage levels $-V_{in}/2$ and $-V_{in}$. From the connection relations of the two capacitors and the current paths shown in Fig.3, the two capacitors have the same discharging currents, which are $i_d/2$ and i_d at levels $V_{in}/2$ and V_{in}, correspondingly. Thus, the continuous discharging amount of each capacitor during the angle θ_3 to $\pi-\theta_3$ is determined as

$$\Delta Q = \int_{\theta_3}^{\theta_4} \frac{i_d}{2\omega} d\omega t + \int_{\theta_4}^{\pi-\theta_4} \frac{i_d}{\omega} d\omega t + \int_{\pi-\theta_4}^{\pi-\theta_3} \frac{i_d}{2\omega} d\omega t \quad (5)$$

Unambiguously, the biggest discharging rate and the resultant maximum voltage ripple for each capacitor are acquired when the load is purely resistive. The peak value of the load current lines up with the central point of the discharging phase. When the capacitance is computed in pure resistive state, voltage ripple on the capacitor will be less when delivering an inductive load. With purely resistive load, the load current will be a staircase waveform. Thus, ΔQ can be estimated as in equation (6).

$$\Delta Q = \frac{V_{in}}{4\pi f_s R_{load}}(4\pi - 3\theta_3 - 5\theta_4) \quad (6)$$

Where f_s is the frequency of the staircase output, and R_{load} is the resistance of the load. The voltage ripple on every capacitor is estimated as in eqn (7).

$$\Delta V = \frac{V_{in}}{4\pi f_s R_{load} C}(4\pi - 3\theta_3 - 5\theta_4) \quad (7)$$

Where C is the capacitance of the capacitor. By considering the allowable voltage ripple ΔV_{ripple}, the smallest capacitance is found using eqn (8).

$$C_{small} = \frac{V_{in}}{4\pi f_s R_{load} \Delta V_{ripple}}(4\pi - 3\theta_3 - 5\theta_4) \quad (8)$$

Therefore, the ripple loss is estimated using eqn (9)

$$P_{ripple} = f_s C(\Delta V^2 + \Delta V'^2) \quad (9)$$

3.3 Conducting Loss Analysis

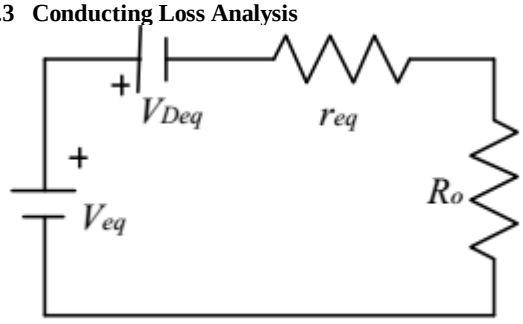

Figure 8: Equivalent current path

On-state resistances of switches and the forward voltage drops of diodes over the current loops are the parasitic parameters which produces conducting loss. Figure 8displays the equivalent current path. In this circuit, V_{eq}, V_{Deq}, r_{eq}, and R_o are the output voltage, the equivalent voltage drop over diodes, the equivalent parasitic resistance and the load resistance, correspondingly. It is assumed that all the diodes as well as the body diodes of power electronic switches take the equal voltage drop V_{drop} and internal resistance r_{int}. Similarly it is assumed that all the switches take the equal on-state resistance $r_{onstate}$. Hence, the equivalent parameters under pure resistive state can be given as in equations (10) – (12).

$$V_{eq} = \begin{cases} 0 & i = 0 \\ \frac{V_{in}}{2} & i = 1 \\ V_{in} & i = 2 \end{cases} \quad (10)$$

$$V_{Deq} = \begin{cases} V_{drop} & i = 0,2,3 \\ 2V_{drop} & i = 1 \\ 0 & i = 4 \end{cases} \quad (11)$$

$$r_{eq} = \begin{cases} r_{int} + r_{onstate} & i = 0 \\ \frac{3r_D + R_{esc}}{2} + 2r_{int} & i = 1 \\ r_{int} + 3r_{onstate} & i = 2 \\ \frac{r_{int} + R_{esc}}{2} + 3r_{onstate} & i = 3 \\ 2R_{esc} + 4r_{onstate} & i = 4 \end{cases} \quad (12)$$

Where $R_{esc}$is equivalent series resistance of each capacitor, and the value of i can be obtained from eqn (13).

$$\mathrm{i} = \left|\frac{2v_o}{V_{in}}\right| \quad (13)$$

$$P_{con} = \frac{2}{\pi}\sum_{i=1}^{4}\left\{\left(\frac{V_{eq} - V_{Deq}}{r_{eq} + R_o}\right)^2 \times r_{eq} \times (\theta_{i+1} - \theta_i)\right\} \quad (14)$$

3.4 Switching Loss analysis

Switching loss of a switch is instigated due to the overlaps of its voltage and current during the process of state change and it can be assessed from the charging and discharging phases of the parasitic capacitance between the drain and the source.

$$P_{switch} = f_s C_p V_b^2 \quad (15)$$

Where f_s, C_p and V_b are the switching frequency, the parasitic capacitance and the maximum block voltage of each switch, correspondingly. Hence the loss of the switch can be calculated from

$$P_{switch} = \frac{45 f_s C_p V_{in}^2}{2} \quad (16)$$

3.5 Comparison with topologies

The LF inverters in [26]-[28] use only one voltage source. However, the topology in [26] provides five output levels and the topology in [27] provides seven levels. The topology in [28] can produce nine levels when many switches are employed to preserve the voltage over the flying capacitor at a preferred level. However it is really challenging to be reached. The lowest THD of the three topologies can only reach 4% [26], although the multicarrier modulation is used to regulate the magnitudes and decrease the THD values of their outputs. More seriously, in multicarrier modulation, the operating frequencies of switching devices are close to the carrier frequency that is dozen times of the output frequency, making modulation methods of this kind inappropriate for applications.

The configurations presented in [29]-[32] employ SC circuits and produce any voltage level depending on the number of component used. Though, a trade off must be maintained between the number of levels and investment costs. An MLI producing nine levels output has the capability to bump into the necessities for industrial applications. Then,

number of components, dc sources used and the peak inverse voltages of the proposed configuration is compared with those of the configurations proposed in [29]-[32] for the equal staircase output of levels.

Table 3: PARAMETER COMPARISONS WITH THE TOPOLOGIES IN [29]-[32]

Parameters	Proposed	Inverter[29]	Inverter [30]	Inverter[31]	Inverter [32]
DC Sources	1	1	2	1	1
Capacitors	4	3	2	3	3
Diodes	4	13	12	10	8
Peak inverse volt	V_{in}	$4V_{in}$	$2V_{in}$	$4V_{in}$	$4V_{in}$

4 EXPERIMENTAL RESULTS

In order to validate the functionality of the proposed multilevel inverter topology a prototype has been built to validate the performances along with the simulation model of the system. The proposed multilevel inverter, the detailed simulation values are listed in the table below. The output of the converter is set to 50Hz and the output is set to 230V ac rms. the functionality of the inverter is validated with the different loads; the Figure 9 demonstrates the output voltage and the required switching signals for the inverter. Moreover the extension of the proposed 7-level inverter to generate 9-level inverter is also validated by inserting another switched capacitor section.

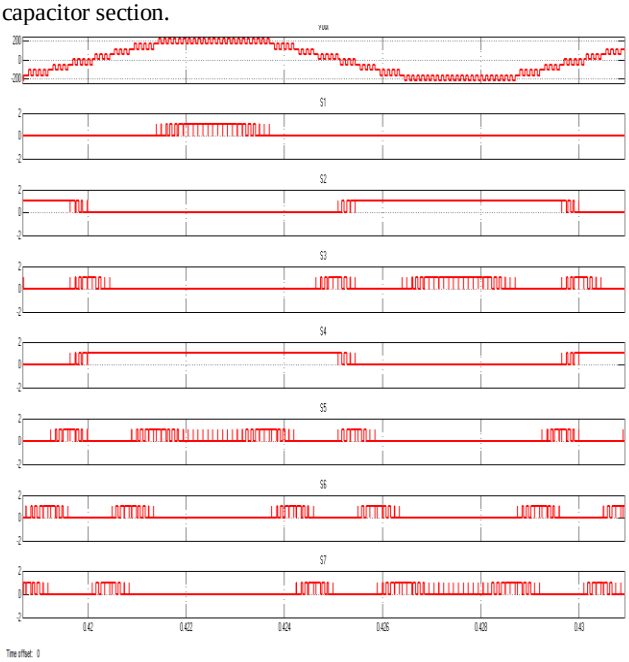

Figure 9: Output voltage and the corresponding switching sequence of the inverter.

In the fig 10, the inverter is derived through the R load with a constant value of 30 ohm pure resistor , the voltage and current patterns of the inverter are seems to be in phase ,and their RMS values are 230V and 7A respectively.

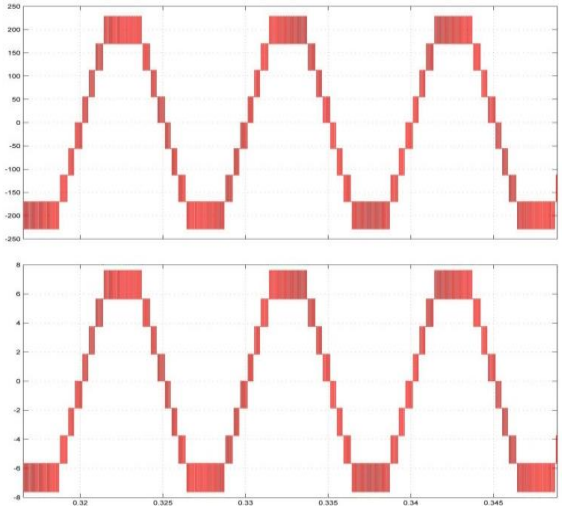

Figure 10: Output voltage and current of the inverter under pure resistive load.

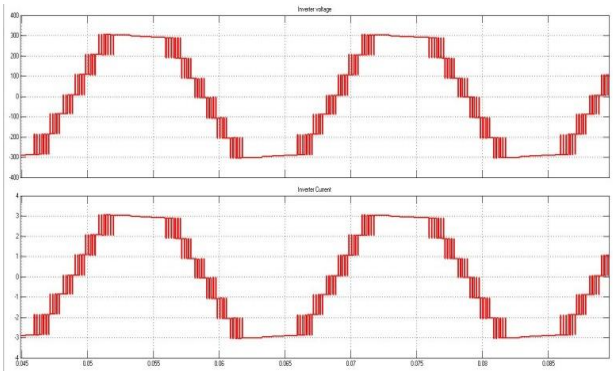

Figure 11: Output voltage and current of the inverter under RL load

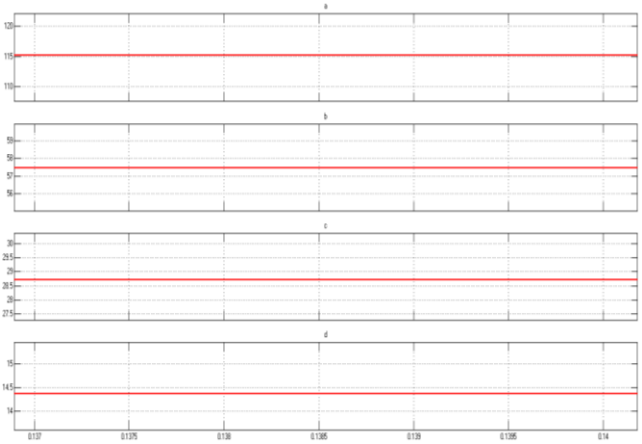

Figure 12: capacitor voltages of inverter under R load

Figure 12 shows the capacitor voltages of the inverter under the R load condition where the input of voltage of the

capacitors are splitted accordance to the voltage balancing conditions of the previous levels by Vdc/2.Starting from the capacitor C1-C4 the voltage is splitted by Vin/2 and second stage by Vdc/4 and the third capacitor by Vdc/8 and Capacitor C4 has a voltage value around Vdc/16. The capacitors are balanced without any additional circuitry; the self-balance of the capacitors brings the output stage combined to form the multilevel pattern.

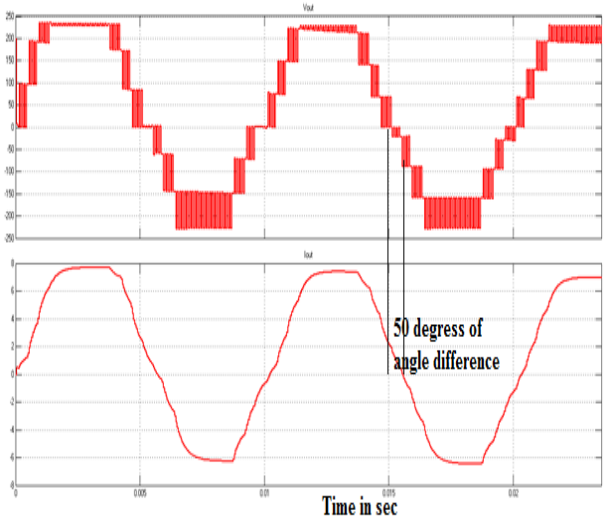

Figure 13: Output voltage of inverter under RL load

Fig 13 shows Output voltage of the inverter under the RL load with a R value of 30 ohm and L value of 30 mH, in this load condition the voltage and the current pattern of the proposed inverter , the current lags behind the inverter around angle of 50 degrees.

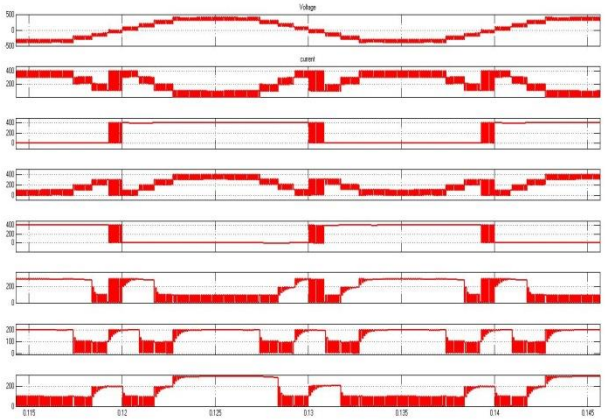

Figure 14: output voltage and the corresponding switch voltages.

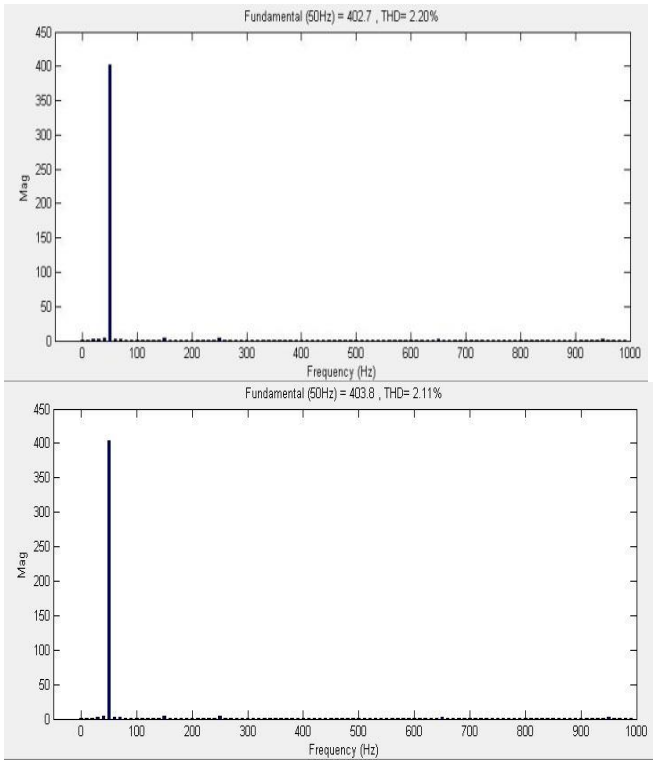

Figure 15: Harmonic analysis for nine level inverter with RL Load. The THD of nine levels for RL load is 2.20% and for R load is 2.11% respectively.

Similarly, for the seven level inverter, the output voltage and current waveforms are shown below.

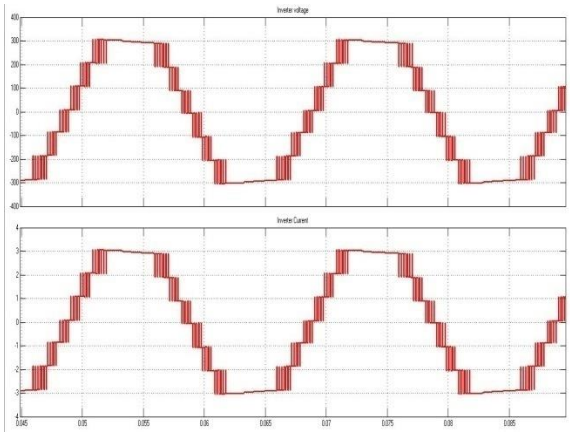

Figure 16: Output voltage and current of the seven level inverter under pure resistive load.

The voltage and current patterns of the inverter are seems to be in phase.

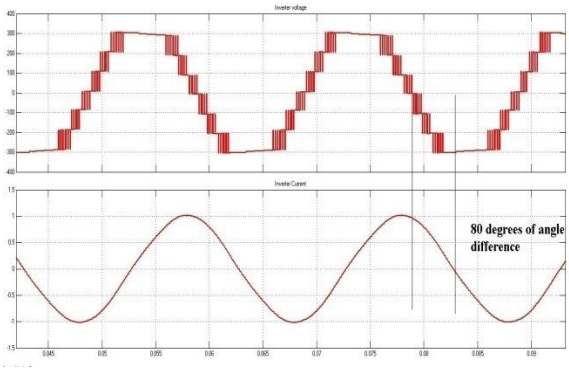

Figure 17: Output voltage of seven level inverter under RL load

Fig 17 shows Output voltage of the seven level inverter under the RL load with a R value of 30 ohm and L value of 30 mH, in this load condition the voltage and the current pattern of the proposed inverter , the current lags behind the inverter around angle of 80 degrees.

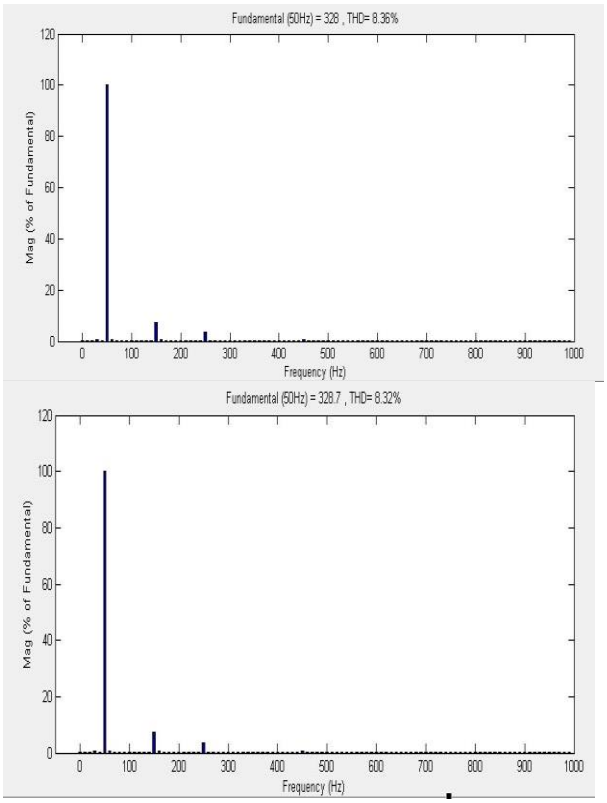

Figure 18: Harmonic analysis for seven level inverter with RL Load. The THD of seven levels for RL load is 8.36% and for R load is 8.32% respectively.

The proposed configuration is realized with hardware components. The results obtained from the hardware experimental prototype are shown in figures 19-24.

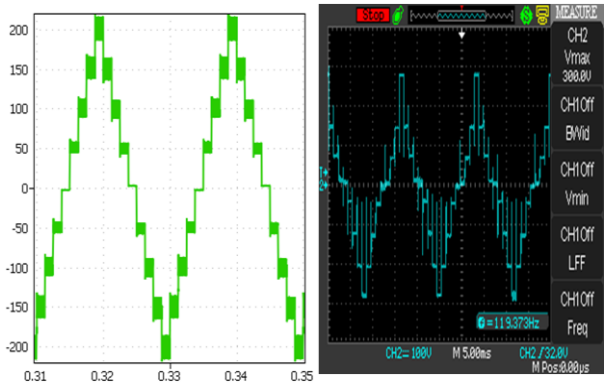

Figure 19: simulated and experimental Output voltage

The above figure shows the simulated and experimental nine level voltages.

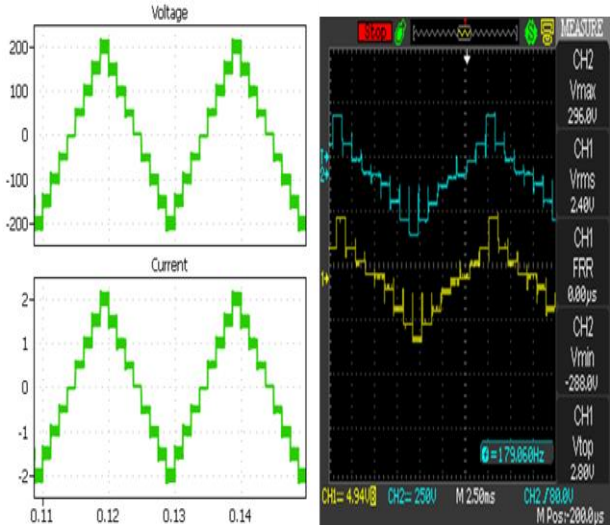

Figure 20: simulated and experimental Output voltage and output current

The voltage and current of the nine level inverter obtained from simulated and experimental results are in phase.

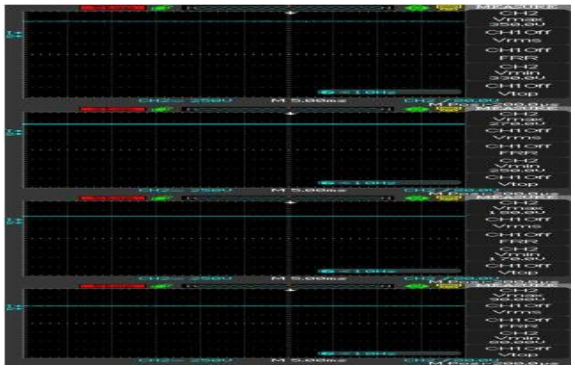

Figure 21: Capacitor Voltages

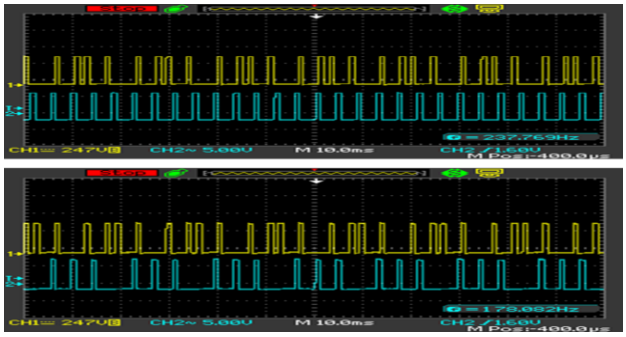

Figure 22: PWM waveforms

Fig.21& 22 shows the experimental waveforms of the capacitor voltages and PWM waveforms respectively.

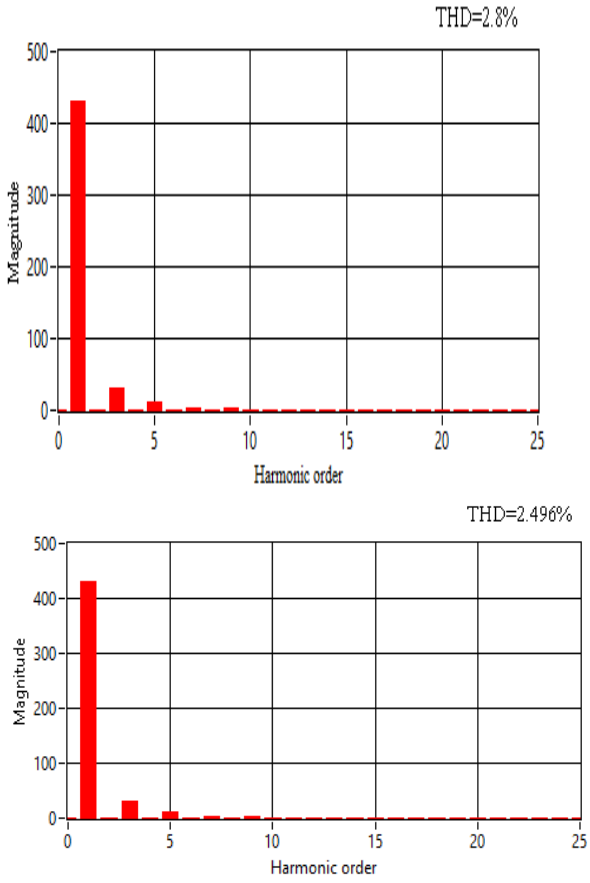

Figure 23: Harmonic analysis for nine level inverter with R and RL Load. The THD of nine level with R load is 2.496% and RL load is 2.8% respectively.

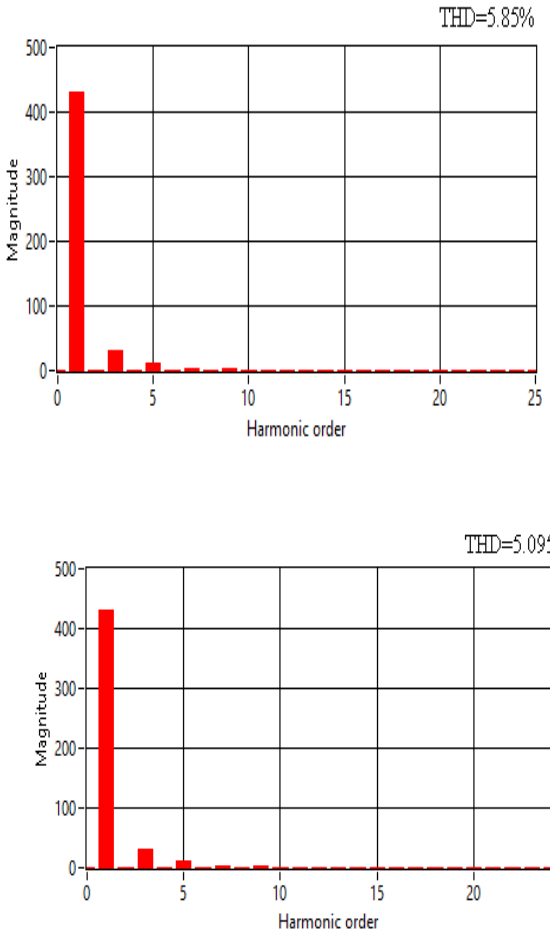

Figure 24: Harmonic analysis for seven level inverter with RL Load. The THD of seven levels with RL load is 5.85% and R load is 5.095%respectively.

5.CONCLUSION

A single phase multilevel inverter is designed with reduced number of switches using switched capacitor circuit based converter and H-bridge inverter. The multilevels are developed from the basic unit. The behavior of the multilevel inverter is validated for seven levels and nine levels. The nine switches are employed to generate the nine level output voltage. The employment of single dc source reduces the system complexity. The levels can be further increased by adding the basic units. It offers lower THD of about 2.8% for nine level and 5.85% for seven levels. The harmonic content can be further reduced by adding the basic units. The multilevel inverter is derived through a simple PWM technique such as sine PWM or multicarrier PWM schemes. The Individual Capacitor voltage balancing is achieved without any additional circuitry or complex algorithms that make the converter design simple. The results shows that the multilevel inverter can be effectively generated with multilevel pattern with reduced harmonic content which makes the converter suitable for larger industrial applications where the quality of power is major concern.

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