A NEW MULTILEVEL INVERTER TOPOLOGY WITH REDUCED SWITCH COUNT FOR SOLAR PV POWER CONVERSION

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Abstract: Multilevel inverters can synthesize a high voltage staircase waveform with low and medium voltage components. A new multilevel inverter topology called Asymmetric Dual Source Multilevel Inverter (ADS-MLI) is proposed. When compared to the topologies found in literature, it can produce multiple levels in the output voltage with less number of power switches. Most of the topologies found in the literature require cascading feature to achieve asymmetric operation; but the ADS-MLI can operate without the need for cascading. Further it requires only two independent DC sources to produce multiple levels in the voltage waveform. The independent sources can be two independent Solar Photo Voltaic (PV) strings. A simulation prototype capable of synthesizing 13 levels fed by Solar PV strings is developed in MATLAB Simulink environment. Its performance is observed in the aspects of number of switching components, efficiency, THD and its efficiency is compared with other topologies. The performance of simulated ADS-MLI is validated with a 1 kW prototype fabricated using FGA25N120-ANTD fed by an Ecosense Solar PV emulator and controlled by FPGA-SPARTAN 6 processor.

Key words: *Multilevel inverter, solar PV plant, Renewable energy, Power Quality*

1. Introduction

Multilevel inverters are getting popular nowadays for medium and high voltage applications. As the number of levels in the output voltage increases, the Total Harmonic Distortion greatly reduces. This improves the quality of voltage delivered as stated in [1]. But increasing the number of levels will require higher number of switches resulting in increased cost and complex control circuitry. The Neutral Point Clamped Multilevel Inverters (NPC-MLI) and Flying Capacitor Multilevel Inverters (FC-MLI) can deliver multiple levels with less number of switches. But these topologies require passive components and diodes which makes the control tedious and also, they cannot deliver asymmetric operation [2]. As far as the Cascaded H-Bridge Multilevel Inverter (CHB-MLI), it is modular with simple circuitry [3-4]; but, the number of switches increases by four for the addition of every two levels in the staircase waveform. Therefore the recent research is focused on the reduction of number of power components required for H-Bridge based topologies to take the advantage of their simplicity and modularity. A topology with reduced circuit components presented in [5] as shown in Fig.1(a). But, the switches employed in the topology are bi-directional switches whose cost is double that single-pack switch and also the higher number of switches in conduction path reduces the efficiency. An Envelope module based topology, wherein the number of switches appears less but, it requires a minimum of four sources in a basic unit is proposed in [6]. With the addition of each basic unit the number of sources increases by four and the number of switches increases by eight. A packed U-cell type topology is given in [7] as shown in Fig. 1(c), but the efficiency of the topology will be low due to the higher number of IGBTs in the conduction path.

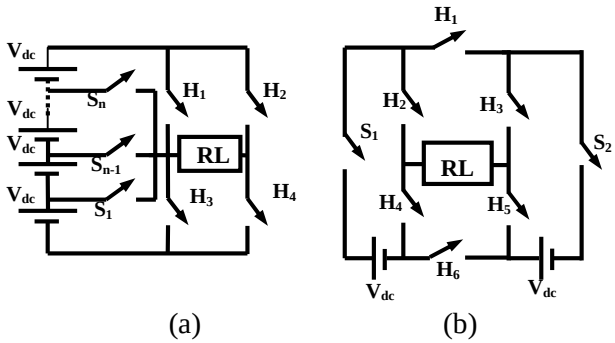


Fig. 1 Topologies presented in [5] and [7]

The above topologies have a limitation that, they have to be cascaded with another similar unit to accomplish asymmetric operation. The ADS-MLI

proposed in this paper can operate in asymmetric mode without the need for cascading. In the following sections the performance of ADS-MLI is analyzed and compared with a conventional CHB-MLI and one of the recent topologies discussed in literature. Also, its capability to operate with solar PV unit is analyzed using an 1 kW Ecosense solar PV emulator.

2. Asymmetric dual source multilevel inverter

The ADS-MLI comprises of two stages viz., i. level adder, ii. polarity changer. The level adder has two independent voltage sources V_{S1} and V_{S2} connected to its upper and lower arm as shown in the Fig. 2. The voltage delivered by the two voltage sources need not be equal and hence it is named as Asymmetric Dual Source Multilevel Inverter. The level adder synthesizes the steps in the voltage wave form as shown in the Fig. 10. The number of steps is proportional to the number of capacitors (Nc) connected in each arm of the level adder. The polarity changer is a H-Bridge that alternates the voltage delivered by level adder. The voltage to be delivered from each source is fixed, based on the number of capacitors clamped in each arm. For the number of capacitors 'N_c' clamped in each arm, the voltage across the capacitor in upper arm should be such that

$$V_{UCX} = N_c V_{LC1} \quad (1)$$

Where, X= 1,2,3…n

From the Equation 1 and Fig.2a it can be understood that if the voltage across capacitor 1 in lower arm is fixed as 1 Volt, and the number of capacitors clamped in each arm is 2, then the voltage across each capacitor of upper arm should be fixed as 2V. The number of levels synthesized from the inverter topology can be determined using the equation

$$N_{Level} = \{N_c[(N_c \times 2)+2]\}+1 \quad (2)$$

The number of IGBTs (N_{switch}) required for producing N_{Level} in the terminal voltage is calculated using the Equation 3.

$$N_{switch} = 2N_c + 5 \quad (3)$$

The number of switches required for the proposed topology for the given number of capacitors is computed using equation 3 and the same has been compared with the similar topologies found in the literature and a comparison chart is plotted as shown in Fig.3

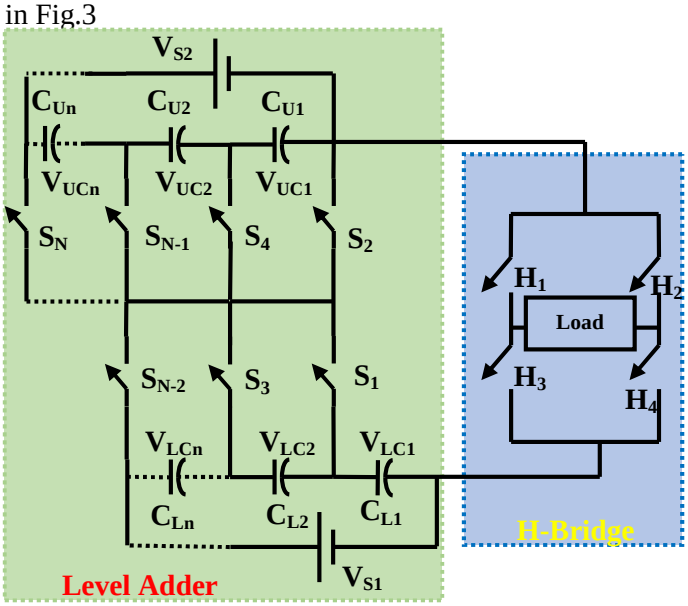


Fig. 2 Structure of ADS-MLI

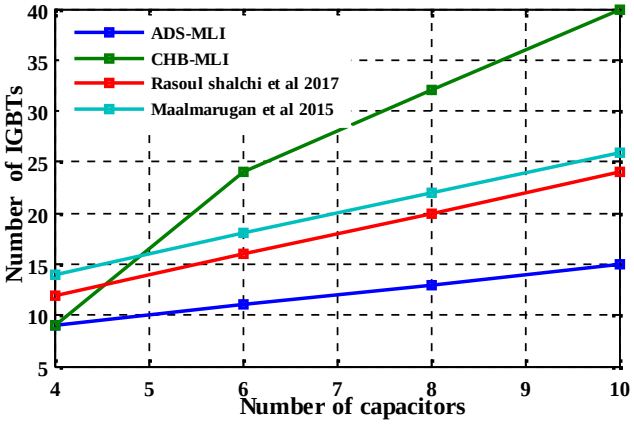


Fig. 3 Number of Capacitors Vs Number of IGBTs

From the Fig.3 it is observed that the number of IGBTS required is only 15 for accommodating a total of 10 capacitors in the circuit. Where as it is 40 for conventional CHB-MLI, 24 for the topology proposed in the Reference [5] and 26 in the topology presented in Reference [7]. With 10 capacitors ADS-MLI can synthesize 62 levels, where as it is only 21 levels in the topology proposed in [5].

3. Simulation of 13 Level ADS-MLI

To understand the operation of the ADS-MLI a 13 level prototype is developed as shown in Fig.4. The sources V_{S1} and V_{S2} are fed by two solar PV strings constituted with combination of PV modules. The solar PV string connected to upper arm is designed to

deliver a voltage of 154 V and the lower one delivers 77 V.

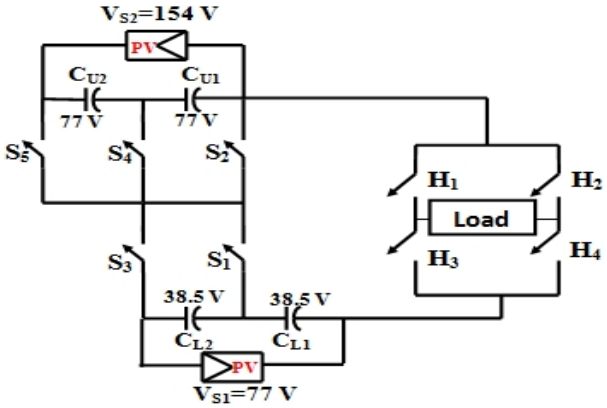
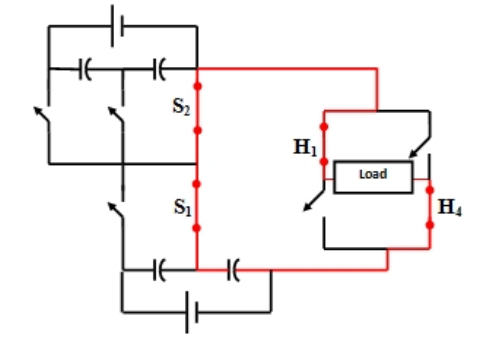
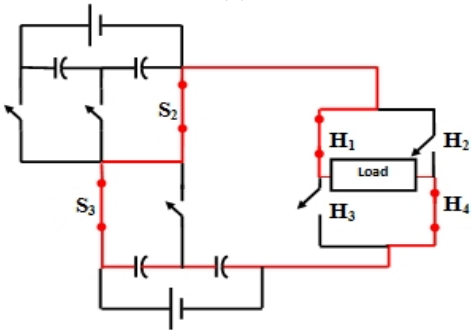


Fig.4. Prototype of 13 level ADS-MLI



(a)



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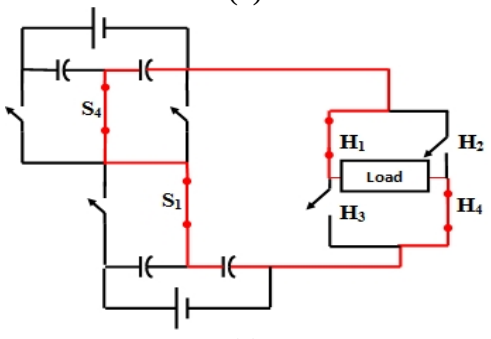


(c)

Fig. 5. Operating modes (a) +38.5 V (b) +77V (c) +115.5 V

To understand the switching sequence the conduction path to synthesize the levels +38.5 V, +77 V and +115.5 V is shown in Fig.5. From the Table 1 and Fig. 5(a) it can be observed that the switches S_1, S_2 in the level adder and H_1,H_4 in the H-Bridge conducts to produce the voltage level 38.5 V. To synthesize the next level 77 V, the switches S_2, H_3, H_4 remains conducting , the switch S_1 turns off and S_3 turns on as shown in Fig. 5(b), to synthesize 112.5 the switches S_3, S_2 turns off and S_1,S_4 turns on as shown in the Fig. 5(c). Similarly other levels can be synthesized as given in Table 1.

Table 1 Switching sequence of ADS-MLI

Level	Switches in Conduction	Voltage Synthesized (v)
1	S_1,S_2,H_1,H_4	38.5
2	S_2,S_3,H_1,H_4	77
3	S_1,S_4,H_1,H_4	115.5
4	S_3,S_4,H_1,H_4	154
5	S_1,S_5,H_1,H_4	192.5
6	S_3,S_5,H_1,H_4	231
7	S_1,S_2,H_2,H_3	-38.5
8	S_2,S_3, H_2,H_3	-77
9	S_1,S_4, H_2,H_3	-115.5
10	S_3,S_4, H_2,H_3	-154
11	S_1,S_5, H_2,H_3	-192.5
12	S_3,S_5, H_2,H_3	-231
13	H_1,H_2 or H_3,H_4	0

4. PWM scheme for ADS-MLI

The pulses for the IGBTs can be obtained using low frequency or high frequency pulse width modulation schemes [8]. The high frequency switching schemes are meant for reducing the THD in two level inverters [9-10]. Since the multilevel inverters have an inherent capability of delivering a voltage waveform with low THD, a low frequency switching scheme can be used for multilevel inverters to reduce the losses [11-12]. The Nearest Level Modulation (NLM) scheme is one of the low frequency switching schemes widely used for multilevel inverters. The concept of NLM is shown in the Fig. 6. In this method, the IGBTs corresponding to a particular voltage level is triggered by the pulse generated by comparing the desired voltage magnitude rounded to the NLM constant with the reference sine wave as shown in the Fig. 6 [13]

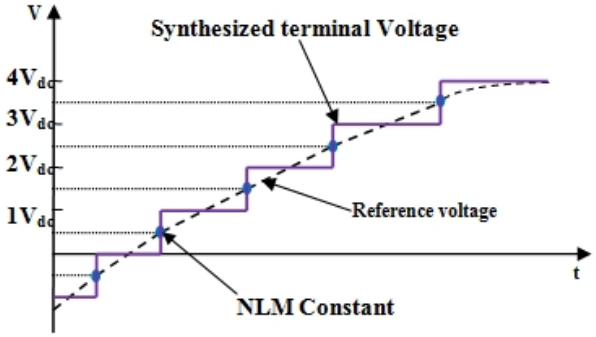
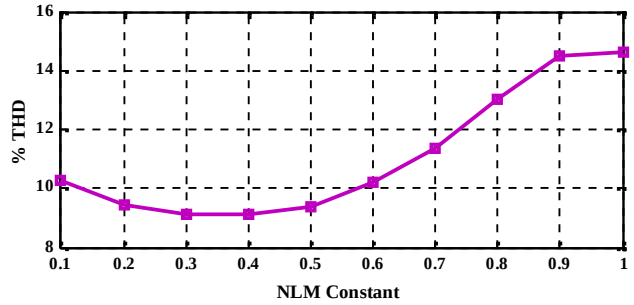
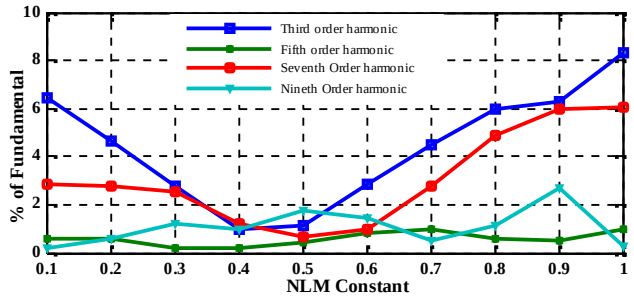


Fig 6. Concept of Nearest Level Modulation

It has been found that at the NLM constant value of 0.4, the magnitude of lower order harmonics and the percentage THD are comparatively low as shown in the Fig. 7 as discussed in [11]. With the reduced lower order harmonics, the power quality of the terminal voltage waveform will be improved. Therefore a nearest level modulation method with an NLM constant of 0.4 is used to control the proposed multilevel inverter topology.



(a)



(b)

Fig. 7 (a) %THD Vs NLM Constant
(b) % of lower order harmonics Vs NLM constant

5. Simulation Results

From the simulation prototype, the parameters like blocking voltage across the switches, terminal voltage, load current and THD of terminal voltage are observed.

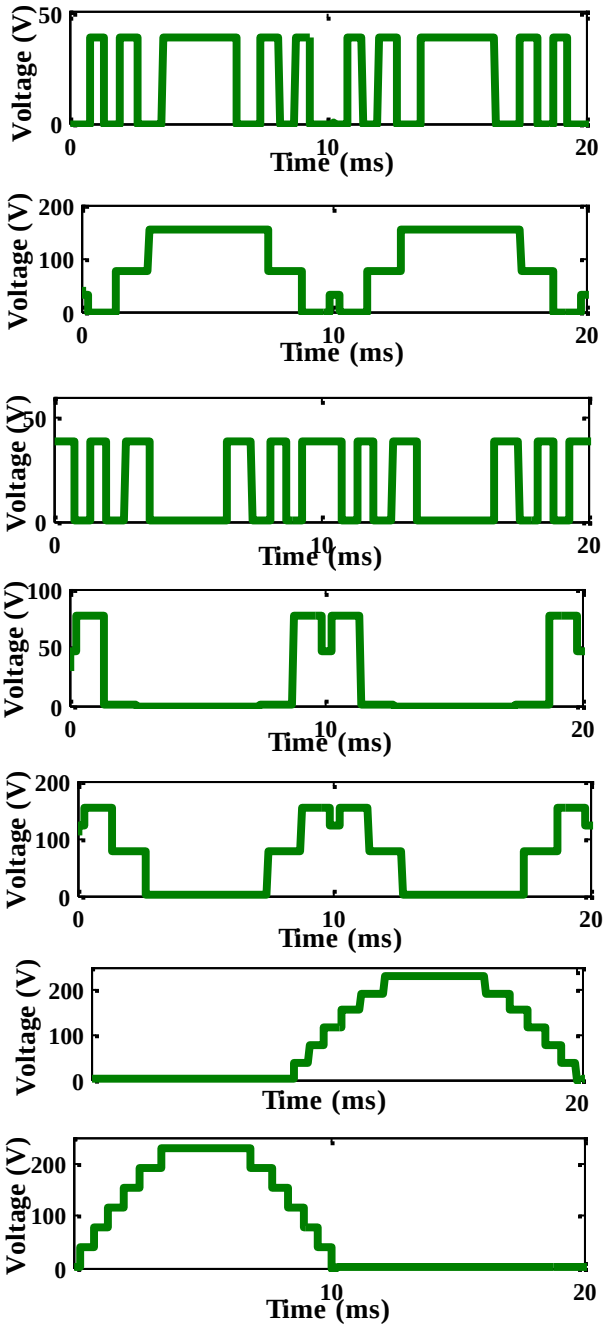


Fig. 8. Blocking Voltage across from top to bottom (a) S_1 (b) S_2 (c) S_3 (d) S_4 (e) S_5 (f) H_1 H_4(g) H_2 H_3

The blocking voltage across the power switch is the voltage across the switch when it is in off state. The switches in the level adder are connected in series with multiple sources and hence, the voltage across any switch is based on the number of open circuit sources in the conduction path. The switches H_1, H_4 and H_2, H_3 are complimentary to each other and they are turned on and off once in every half cycle. Thus, the blocking voltage across each H-bridge will be equal to the maximum voltage in every half cycle,

i.e. the continuous sum of magnitude of all the voltage sources in the level adder. The blocking voltage across the switches in the level adder (S_1-S_5) and the blocking voltage across the switches in H-Bridge (H_1, H_4 and H_2, H_3) are shown in Fig. 8.

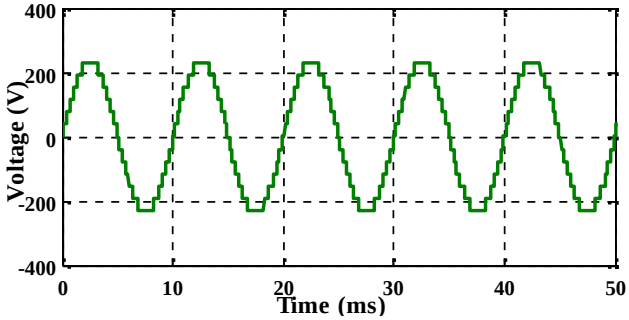


Fig. 9 Thirteen level load voltage delivered by ADS-MLI

With two capacitors clamped in the upper and lower arm, the ADS-MLI synthesizes a stair case waveform with six step in each half cycle. Each step is rated 38.5 V as shown in the Fig. 9. The peak volage magnitude obtained is 231 V.

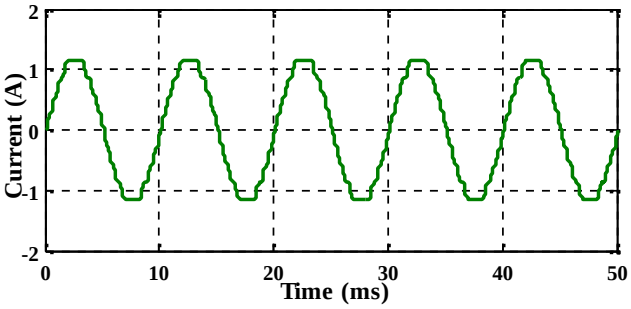


Fig. 10 Load current observed in the terminals of ADS-MLI

For a load with resistance of 200 ohm and inductance 70 mH, the load current observed is 1.15 Ampere peak as depicted in Fig. 10. The load inductance acts as natural filter, thus reducing the ripples in the load current and making it near sinusoidal. The THD of the voltage waveform is calculated using the equation

$$THD = \frac{\sqrt{\left(\sum_{i=1,3,5}^{\infty} V_{oi}\right)}}{V_{of}} \quad (4)$$

The magnitude of fundamental and harmonic voltage components are influenced by the step angle calculated using the Equation 5

$$\sim_k = \sin^{-1}\left(\frac{A-0.5}{N_{step}}\right) \quad (5)$$

Where, $A = 1,2,.....\left(\frac{N_{Level}-1}{2}\right)$ (6)

$$N_{Step} = \left(\frac{N_{Level}-1}{2}\right) \quad (7)$$

From the Equation 5, it is understood that the firing angle is influenced by the number of steps in the output voltage and which in turn determines the magnitude of fundamental and harmonic components in the terminal voltage [14]. Thus with higher number of steps in the terminal voltage the percentage THD can be reduced. Further, the lower order harmonics are reduced to a greater extent by choosing an optimal value of NLM constant, thus the overall THD is reduced to 6.25 % as shown in the Fig. 12.

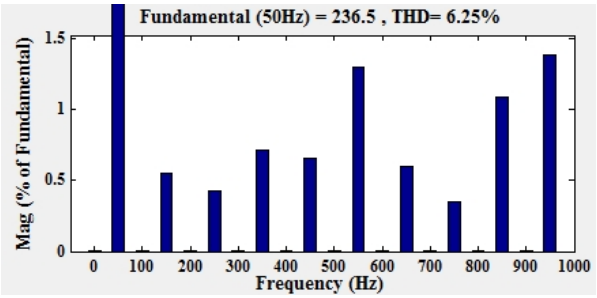
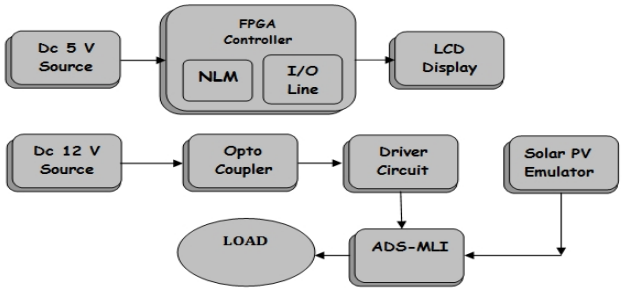


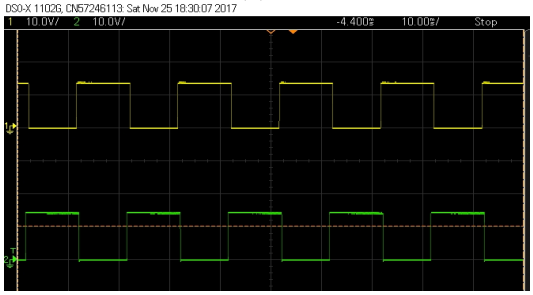
Fig. 11 Harmonic spectra of ADS-MLI

6. Experimental Results

To validate the simulation results an experimental prototype has been developed. An Eco Sense Solar PV emulator is used in the place of solar PV units. The ADS-MLI is fabricated with FGA25N120 IGBT switches. The gate pulses are synthesized using FPGA SPARTAN PROCESSOR with an NLM constant 0.4. The functional block diagram of the experimental setup is shown in the Fig. 12(a). The experimental gate pulses given to the H-Bridge is shown in the Fig. 12(b).



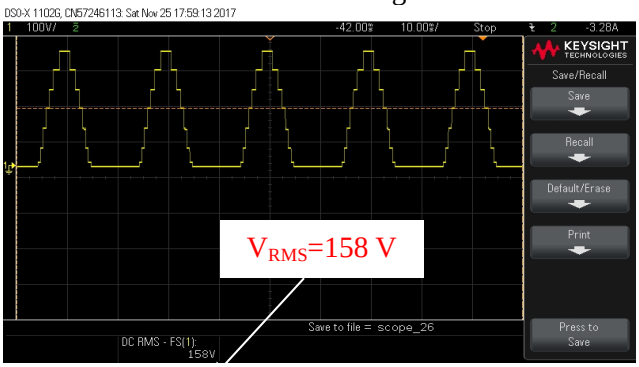
(a)



(b)

Fig. 12 (a) Functional Block Diagram
(b) Gate pulses given to H-Bridge

The complementary nature of the pulses given to H-Bridge can be observed from the Fig. 12 (b). Further the experimental blocking voltage observed across the switches in H-Bridge and one of the switches (S_2) in level adder are shown in the Fig. 13



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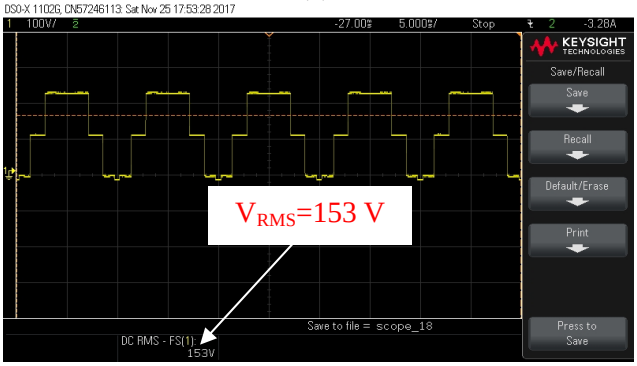
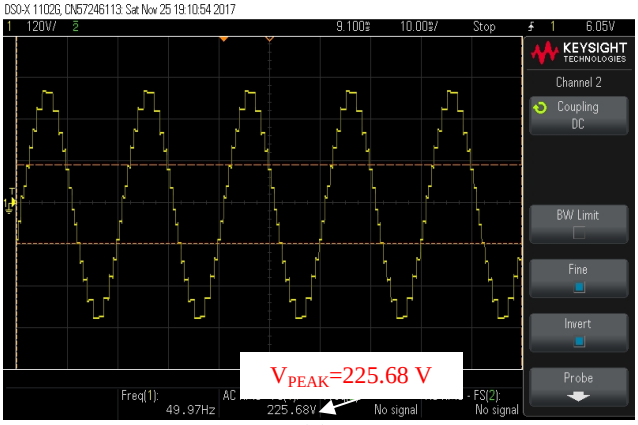


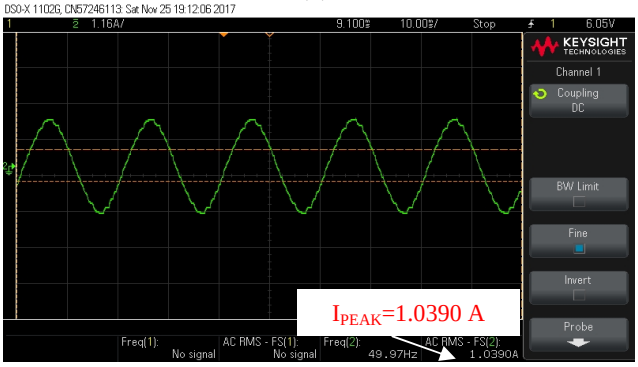
(b)

Fig. 13 Blocking voltage across (a) H_1 (b) S_2

From the Fig. 13, it is observed that the blocking voltage across the switches H_1 and S_2 are 158 V and 153 V respectively. The obtained voltages are given in RMS values. For a load resistance of 200 ohm and inductance 70 mH, the experimental load voltage, load current and voltage THD values obtained are 225.68 V, 1.039 A and 7.1 % respectively as shown in the Fig. 14 (a), (b) and (c)



(a)



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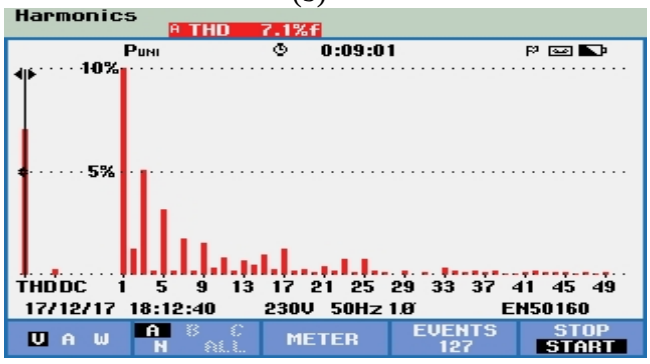


(c)

Fig. 14 (a) Load Voltage (b) Load current
(c) Load voltage THD

7. Evaluation of efficiency

The efficiency of any inverter topology is influenced by the power losses in the switch. A

practical switch requires finite turn on and turn off time, this results in switching losses. The internal resistance of a practical switch results in conduction losses. The turn-on time $T_{S\text{-}on}$ and Turn off time $T_{S\text{-}off}$ and the internal resistance R_{on} is obtained from the data sheet of FGA25N120 IGBT. The average power loss across a power switch in a switching instant is represented using the Equation 8.

$$P_{average} = \frac{1}{T_{total}} \int_0^{T_{total}} v(t) \times i(t) dt \quad (8)$$

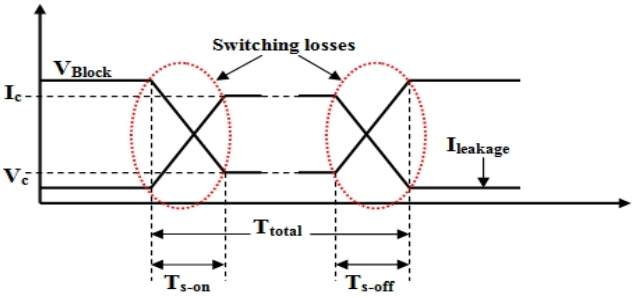


Fig. 15 Linear approximation of current voltage during a switching instant

The linear approximated model of voltage and current in a practical switch during a switching instant is shown in Fig. 15 [15-16]. From the Fig. 15, the instantaneous voltage and current in a switching instant can be written as

$$i(t) = \frac{T}{T_{S-on}}(I_c - I_{leakage}); 0 \le T \le T_{S-on} \quad (9)$$

$$i(t) = I_c; T_{S-on} \le T \le T_{total} - T_{S-off} \quad (10)$$

$$i(t) = -\frac{T - T_{total}}{T_{S-on}}\left(I_c - I_{leakage}\right) + I_{leakage} \quad (11)$$

$$for; T_{total} - T_{S-off} \le T \le T_{S-on}$$

Similarly the instantaneous voltage can be obtained using the equation

$$v(t) = -\frac{V_{BLOCK} - V_c}{T_{S-on}}(T - T_{S-on}) + V_C; 0 \le T \le T_{S-on} \quad (12)$$

$$v(t) = V_c; T_{S-on} \le T \le T_{total} - T_{S-off} \quad (13)$$

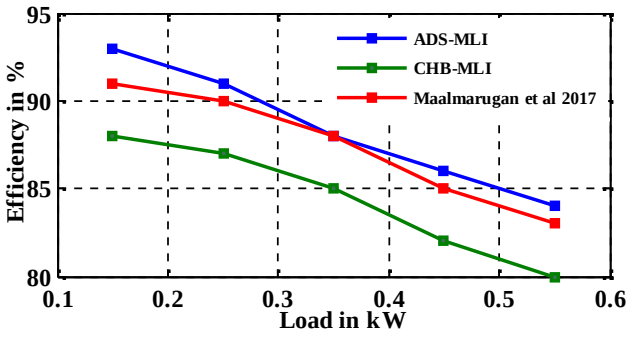
$$v(t) = \frac{V_{BLOCK} - V_c}{T_{S-off}}\left(T - (T - T_{S-on})\right) + V_C \quad (14)$$

$$for; T_{total} - T_{S-off} \le T \le T_{S-on}$$

By substituting the equations from 9-14 in 8, the average power loss is obtained as

$$p_{average} = \frac{V_{BLOCK} I_c}{T_{total}}\left(\frac{T_{S-on} + T_{S-off}}{6}\right) + \frac{V_c I_c}{T_{total}}\left(T_{total} - T_{S-on} - T_{S-off}\right) \quad (15)$$

Here V_c and I_c are voltage and current during conduction of the switch. V_{BLOCK} and $I_{leakage}$ are their off-state counterparts. T_{total} is the total time a switch is in conduction after turning On. The first component in Equation 14 represents the average switching loss and the second components represent the average conduction voltage loss. The parameters $T_{S\text{-}On}$ and $T_{S\text{-}Off}$ are same for all the switches and the values are obtained from the datasheet of FGA25N120 as 50 ns and 190 ns respectively. From the experimental prototype the blocking voltage across the switch H_1 is observed as 158 V and the conduction current is 0.78 A. With the $T_{S\text{-}On}$ and $T_{S\text{-}Off}$ values obtained, The switching loss per switching instant across switch H_1 is approximately 0.0011W since the number of switching instants per cycle is two, the switching loss per cycle is 0.0022 W. The voltage during conduction is calculated using conduction current and the internal resistance of the switch obtained from its data sheet. The conduction loss in switch H1 is observed as 0.6 W. Similarly the switching and conduction loss for other switches can be computed. The total switching and conduction loss in the inverter is 6 W. From the Fig. 14 (a) and (b), The RMS value of load voltage and load current is observed as 0.73 Ampere and 158 Volt respectively. Therefore the output power is 93 Watt at a power factor of 0.8. Thus the efficiency of ADS-MLI topology is calculated as 93 %. The efficiency of ADS-MLI at different load conditions are calculated and compared with the similar topologies available in the literature and the results are plotted as in Fig. 16 (a) and the experimental setup in the laboratory is shown in Fig. 16(b).



(a)

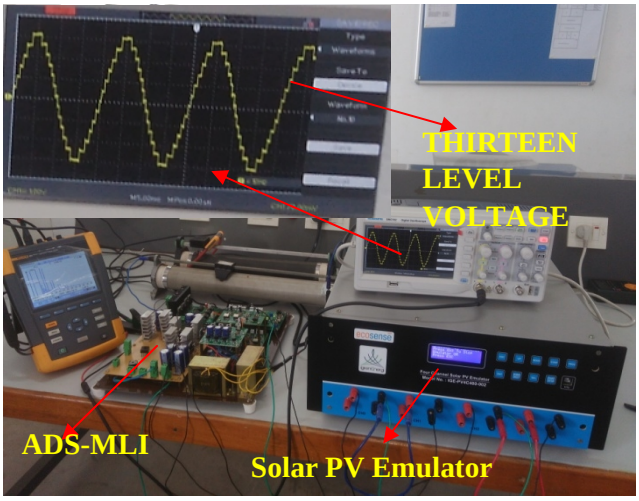


Fig.16 (a) Comparison of efficiency (b) Experimental setup

7. Conclusion

A new multilevel inverter topology called Asymmetric Dual Source Multilevel Inverter is proposed. It employs two independent PV strings constituted by solar PV modules as its sources two produce a 13 level output voltage. A simulation prototype fed by two solar PV strings is developed and it is observed at a load of 0.16 kW (RMS), its peak value of 13 level output voltage is 231 V at a THD of 6.25 %. The simulation results are validated with an experimental prototype, wherein the terminal voltage at same input and load conditions is 228 V peak at a THD of 7.1 %. The experimental efficiency of the ADS-MLI is found as 93% for 0.16 kW load and it is 89 % and 91 % for conventional CHB-MLI and the packed U-Cell proposed in [7]. The efficiency of the ADS-MLI is high, since it has less number of switching components and less number of switches in conduction path while producing every voltage level.

8. References

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