DESIGN AND ANALYSIS OF AN IMPROVED HIGH GAIN NON ISOLATED INTERLEAVED BOOST CONVERTER FOR SOLAR PHOTOVOLTAIC APPLICATIONS

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***Abstract**: In this paper, a novel non isolated four phase interleaved boost converter (IBC) with high voltage gain and reduced stress has been derived. This converter topology is intended to achieve a high step up gain without applying high duty cycle, utilizing input parallel and output series configuration. With less number of components, switching loss and conduction loss are also much reduced. Uniform current sharing without adding complex control methods reduces input ripple current. Due to reduced current ripple at input side and optimal number of phases, this converter is suitable for photovoltaic interface. The design equations has been derived and analyzed for the proposed converter. The theoretical analysis and simulation results validate the performance of the converter.*

***Key words:** Gain, voltage stress, photovoltaic cells, pulse width modulation, voltage control.*

1. Introduction

Energy crisis is the major problem existing all over the world. Due to this shortage of energy, renewable energy sources like wind, ocean, solar cells and fuel cells are widely used. But the problem with renewable energy source is inherent low voltage characteristics. Hence a high quality power conditioning circuit has to be designed. Poor efficiency and high duty ratio to obtain high voltage gain are the main drawbacks of conventional boost and buck–boost converters. High duty ratio leads to large reverse recovery problem which increases the conduction loss and stress on switches which leads to high voltage spikes [1].

Many researches have been carried over to develop a converter with a high step-up voltage gain and without an extremely high duty ratio [2]. A DC–DC flyback converter is a simple isolated structure with a high step-up voltage gain, but the transformer leakage inductance produces a high voltage stress across the main switches. To reduce the stress of the switch and to reuse the leakage inductance energy, some novel energy regeneration technique has been proposed [3-4]. Converters with isolated topology, like phase shifted full bridge converters can achieve a high step-up gain by increasing the turn's ratio of the transformer. But the problem is that the output power will be reduced with higher current ripple which mainly affects the life of the input side capacitor. Hence to reduce further effects of large input current ripple, more number of electrolytic capacitor are used. It is also detected that the output voltage is very less than the voltage stress of the diode hence the efficiency of the circuit depraves. Isolated current-type converters such as the active clamp dual boost converters, full-bridge boost converters with active clamp [5], produces high efficiency and high gain, but the starting operation of these converters must be analyzed separately. Moreover, closed loop controllers, sensors and other switching devices increase the overall cost. To enhance the performance of a standalone PV system whose power output keeps changing with the radiation, automatic sliding mode control technique is chosen [6]. To increase the efficiency of the system and to decrease the cost, a non isolated dc/dc converter [7] will be the best choice. The capacitor-based converters proposed in [8-10] achieves large voltage conversion ratio improving the efficiency, but high transient current and large conduction losses occurs in this switched capacitor technique.

The converter topology with high voltage gain [11–13] that utilizes leakage inductance energy for charging the capacitors with reduced stress is presented, however the input current ripple is high. The interleaved voltage doublers [14-17] with reduced stress and instinctive current sharing capability have been proposed. A high step-up ratio converter with high voltage gain without high duty cycle using switched inductor technique [18] and high gain converter for PV generation system with built in transformer voltage doubler cell using ZVT have been studied. The high step-up converter [19] with ZVT with built in transformer is proposed, however leakage inductance due transformer cause

loss. Besides, to obtain extremely high step-up conversion, many switched capacitor cells are required which increases the circuit complexity [20]. For power factor correction in front end universal line with high efficiency, there is no much voltage gain as well as the stress across switches remains high [21]. Various converter topologies with high gain and reduced stress across the switches are discussed in [22–23].

Energy efficiency of switched-capacitor converters was presented in [24] in which some design rules for high efficient converters have been presented. In [25] switching loss and electromagnetic interference with soft switching technique without using extra components have been analyzed. To reduce the switching loss and electromagnetic interference, many converter topologies have been presented based on a switched-capacitor cell concept using soft switching technique [26]. Ultra high gain converter is introduced in [27], but the diode stress is high. Each converter has its own merits and demerits.

Based on the literature survey, a high power conditioning circuit with very high voltage gain, with reduced losses, with reduced voltage stress has to be designed and analyzed. A two phase transformer-less adjustable voltage quadrupler dc-dc converter with reduced semiconductor voltage stress and high gain is proposed in [28]. This converter provides large step-up voltage conversion ratio with no higher duty ratio and no much complexity but the voltage stress of diodes still remains high.

In this paper, a new topology of four phase transformer-less adjustable voltage quadrupler topology is proposed. It integrates four inductors parallel with each other at the input side for automatic current sharing capability to achieve a high voltage gain. Besides the reduction in the voltage stress of active switches and diodes, the overall conversion efficiency is highly enhanced. Section 2 outlines the circuit topology and the operating principle for each mode of operation. The steady state analysis is further analyzed in Section 3 that provides detailed converter characteristics. The functioning of the proposed system has been validated through MatLab/Simulink and the simulation results that provide detailed information about the stress, efficiency and gain for the converter is presented in Section 4 for demonstrating the merits of the proposed converter. Finally, conclusions are offered in the last section.

2. Modes of operation of the proposed converter

The designed converter topology is derived from a two-phase voltage quadrupler. Fig. 1 shows the novel four phase quadrupler topology. It can be seen that two blocking (auxiliary) capacitors and four diodes are added in the existing topology for a four phase so that during the energy transfer period, the stored energy in the inductor is stored in one capacitor and partial inductor stored energy together with energy stored in the other capacitor is transferred to the output to achieve higher voltage gain. The proposed voltage gain is multiple times higher than that of the interleaved two-phase boost converter. The voltage spike existing across active switches and diodes are much lower than that of the existing converter topologies. The proposed converter produces involuntary uniform current sharing capability without additional circuit and complex control methods. The detailed operating principle can be illustrated as follows.

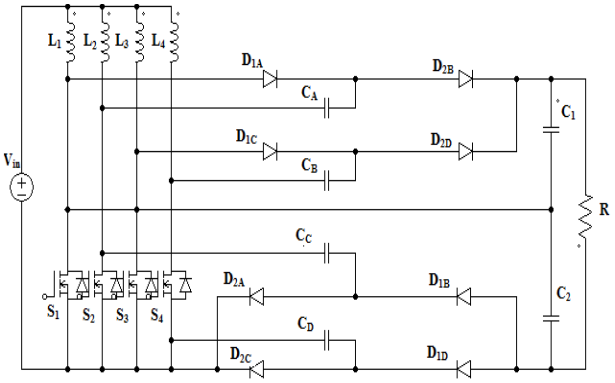

Fig.1. Configuration of four phase proposed converter

The main objective of this paper is to reduce the stress across the switches with high voltage gain in continuous conduction mode (CCM) and that can only be achieved when the duty cycle is greater than 50% hence, the steady-state analysis is made only for CCM mode. But, with duty cycle lower than 50% that is in Discontinuous Conduction Mode (DCM), as there is no enough energy transfer from the energy storage inductors to the auxiliary capacitors, it is not possible to get the high voltage gain for duty ratio greater than 50%.

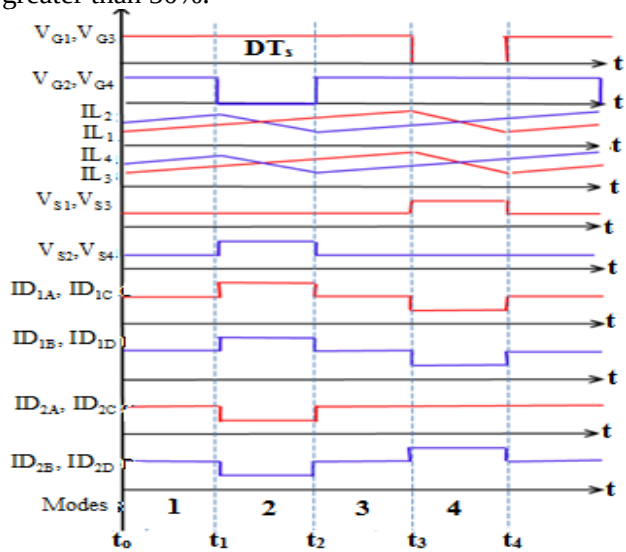

Fig.2. Key operating waveforms of the proposed converter at CCM

Due to the charge balance of the blocking capacitor, automatic current sharing characteristic is possible. With duty cycle is less than 50%, the converter does not produce the automatic current sharing capability. Hence the current-sharing control between each phase should be taken into account. Basically, the working principle of the converter is classified into four modes of operation. The gating signals with 180◦ phase shift and some key operating waveforms are shown in Fig. 2

In order to simplify the circuit analysis of the proposed converter, it is assumed as

- All components are ideal components
- The voltages across capacitors can be considered as constant approximately.

2.1 Mode 1 [$t_0 \le t \le t_1$]: In mode 1, switches S_1, S_2, S_3 and S_4 (Fig. 3) are turned ON and all the diodes D_{1A}, D_{1B}, D_{2A}, D_{2B}, D_{1C}, D_{1D}, D_{2C}, and D_{2D} are OFF. It is seen that the inductor currents i_{L1}, i_{L2}, i_{L3} and i_{L4} are increasing to store energy in L_1, L_2, L_3 and L_4, respectively. The voltages across diodes D_{1A}, D_{2A}, D_{1C}, and D_{2C} are clamped to capacitor voltage V_{CA}, V_{CB}, V_{CC} and V_{CD}, respectively. The voltages across the diodes D_{1B} and D_{2B} are clamped to V_{C2} minus V_{CB} and V_{C1} minus V_{CA}. The voltages across the diodes D_{1D} and D_{2B} are clamped to V_{C4} minus V_{CD} and V_{C3} minus V_{CC} respectively. The load power is supplied from capacitors C_1, and C_2.

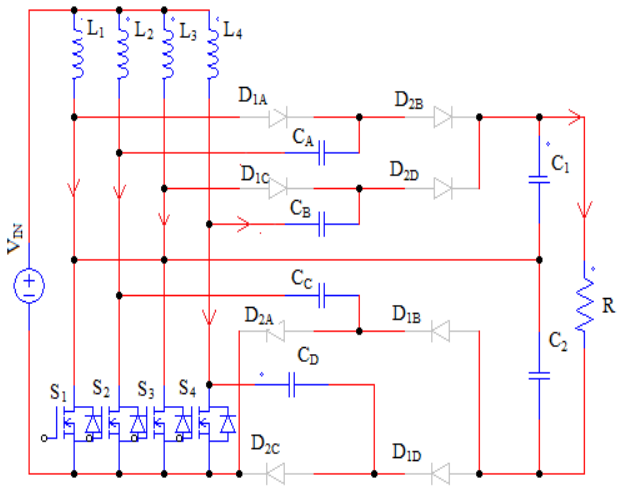

Fig.3. Equivalent circuit for Mode 1 Operation

The corresponding state equations are given as follows

$$L_1 \frac{di_{L1}}{dt} = V_{in} \quad (1)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \quad (2)$$

$$L_3 \frac{di_{L3}}{dt} = V_{in} \quad (3)$$

$$L_4 \frac{di_{L4}}{dt} = V_{in} \quad (4)$$

During this mode of operation the current flowing through the auxiliary capacitors C_A, C_B, C_C and C_D is equal to zero.

$$C_A \frac{dv_{CA}}{dt} = 0 \quad (5)$$

$$C_B \frac{dv_{CB}}{dt} = 0 \quad (6)$$

$$C_C \frac{dv_{CC}}{dt} = 0 \quad (7)$$

$$C_D \frac{dv_{CD}}{dt} = 0 \quad (8)$$

The current flowing through the output capacitors C_1, and C_2 is given by

$$C_1 \frac{dv_{C1}}{dt} = -\frac{(v_{C1} + v_{C2})}{R} \quad (9)$$

$$C_2 \frac{dv_{C2}}{dt} = -\frac{(v_{C1} + v_{C2})}{R} \quad (10)$$

2.2 Mode 2 [$t_1 \le t \le t_2$]: In this operation mode, switch S_1 and S_3 conducts, whereas S_2 and S_4 are turned OFF. Diodes D_{2A}, D_{2B}, D_{2C} and D_{2D} conduct.

Part of stored energy in inductor L_2, L_4 and stored energy of C_A, C_C is now released to output capacitor C_1, C_3 and load and meanwhile, part of stored energy in inductor L_2 and L_4 is stored in C_B and C_D respectively. The corresponding equivalent circuit is shown in Fig.4.

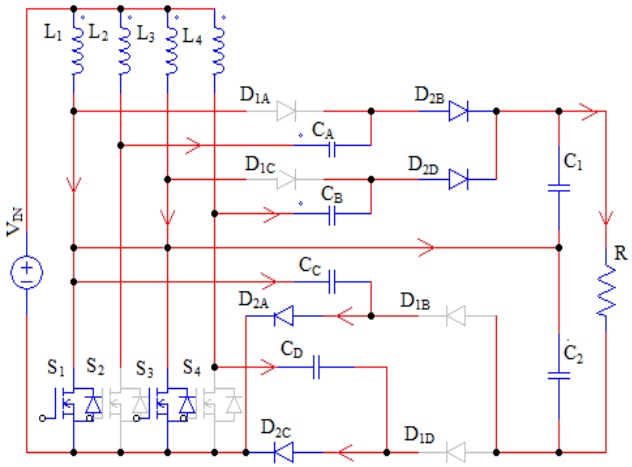

Fig.4. Equivalent circuit for Mode 2 Operation

In this mode of operation, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA} and similarly capacitor voltage V_{C2} is equal to V_{CD} plus V_{CC}. Thus, i_{L1}, i_{L3} still increases continuously and i_{L2}, i_{L4} decreases linearly.

The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} \quad (11)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} + v_{CA} - v_{C1} = V_{in} - v_{CB} \quad (12)$$

$$L_3 \frac{di_{L3}}{dt} = V_{in} \quad (13)$$

$$L_4 \frac{di_{L4}}{dt} = V_{in} + v_{CC} - v_{C1} = V_{in} - v_{CD} \quad (14)$$

$$C_A \frac{dv_{CA}}{dt} = i_{CB} - i_{L2} \quad (15)$$

$$C_B \frac{dv_{CB}}{dt} = i_{CA} + i_{L2} \quad (16)$$

$$C_C \frac{dv_{CC}}{dt} = i_{CD} - i_{L4} \quad (17)$$

$$C_D \frac{dv_{CD}}{dt} = i_{CC} + i_{L4} \quad (18)$$

$$C_1 \frac{dv_{C1}}{dt} = -i_{CA} - \frac{(v_{C1} + v_{C2})}{R} \quad (19)$$

$$C_2 \frac{dv_{C1}}{dt} = -\frac{(v_{C1} + v_{C2})}{R} \quad (20)$$

2.3 Mode 3 [$t_2 \le t \le t_3$]: In this operating mode, all the switches S_1, S_2, S_3 and S_4 are turned ON and that is shown in Fig.3. The corresponding equivalent circuit turns out to be the same as Fig. 3.

2.4 Mode 4 [$t_3 \le t \le t_4$]: For this operation mode, switches S_2 and S_4 remains conducting and S_1 and S_3 is turned OFF. Diodes D_{1A}, D_{1B}, D_{1C} and D_{1D} become conducting. The corresponding equivalent circuit is shown in Fig. 5.

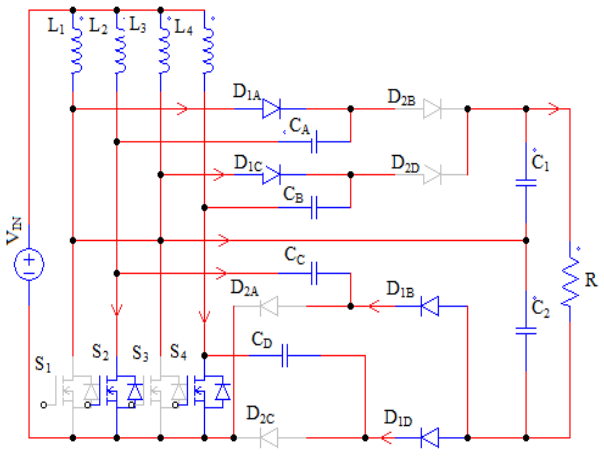

Fig.5. Equivalent circuit for Mode 4 Operation

It is seen from Fig. 5 that the part of stored energy in inductor L_1 and L_3 as well as the stored energy of C_B and C_D is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 and L_3 is stored in C_A and C_C. In this mode, the output capacitor voltage V_{C2} is equal to sum of voltages across all the blocking capacitors.

Thus, i_{L1} and i_{L3} decrease linearly and i_{L2} and i_{L4} still increases continuously. It can be seen from the waveforms, the voltage stresses on the diodes are much reduced and uniform current sharing is achieved.

The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C2} + v_{CB} = V_{in} - v_{CA} \quad (21)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} \quad (22)$$

$$L_3 \frac{di_{L3}}{dt} = V_{in} - v_{C2} + v_{CD} = V_{in} - v_{CC} \quad (23)$$

$$L_4 \frac{di_{L4}}{dt} = V_{in} \quad (24)$$

$$C_A \frac{dv_{CA}}{dt} = i_{CB} + i_{L1} \quad (25)$$

$$C_B \frac{dv_{CB}}{dt} = i_{CA} - i_{L1} \quad (26)$$

$$C_C \frac{dv_{CC}}{dt} = i_{CD} + i_{L2} \quad (27)$$

$$C_D \frac{dv_{CD}}{dt} = i_{CC} - i_{L2} \quad (28)$$

$$C_1 \frac{dv_{C1}}{dt} = -\frac{(v_{C1} + v_{C2})}{R} \quad (29)$$

$$C_2 \frac{dv_{C2}}{dt} = -\frac{(v_{C1} + v_{C2})}{R} \quad (30)$$

From the above equations and illustrations, it can be found that the operation of a four phase interleaved boost converter is simple with excellent features which can be best suited for PV source as input. The performance analysis of the proposed converter is assumed to be in CCM for simplified analysis.

3. Design Considerations

The design procedure of the proposed topology based on the following specifications is described as follows.

Input Voltage = 32 V
Output Voltage = 1024 V
Output Power = 1638 W
Switching Frequency = 40 kHz

3.1. Input Inductance

$$L_{in} = \frac{V_{in}(1-D)D}{\Delta I_L f_s} \quad (31)$$

D represents the duty ratio of the switches.
ΔI_L represents the peak to peak ripple current of the Inductor.

f_S represents the switching frequency.

ΔI_L is chosen in the range between 20 to 40 % of the output Current I_O.

3.2. Auxiliary Capacitance

$$C_A = \frac{I_O D}{\Delta V_{CA} f_S} \quad (32)$$

ΔV_{CA} represents the peak to peak ripple voltage of the blocking capacitor. It is approximately chosen as 1 V.

3.3. Output Capacitor

$$C_O = \frac{V_O D}{\Delta V_{CO} f_S R} \quad (33)$$

ΔV_{CO} represents the peak to peak ripple voltage of the output capacitor.

It is chosen to be 4 to 5 % of ΔVC_A.

R represents the load resistance.

3.4. Voltage Gain

$$\frac{V_o}{V_{in}} = \frac{8}{1-D} \quad (34)$$

3.5. Power Output

$$P_O = \frac{V_o^{\,2}}{R} \quad (35)$$

3.6. Output Current

$$I_O = \frac{P_o}{V_o} \quad (36)$$

4. Analysis of the proposed Converter

4.1 Voltage Gain

From Fig.3 and Fig.5 the volt-time relationship of the inductor L_1, L_2, L_3 and L_4 can be obtained as follows:

$$2V_{in}D + V_{in}(1-D) + (V_{in} - V_{CA})(1-D) = 0 \quad (37)$$

$$2V_{in}D + V_{in}(1-D) + (V_{in} - V_{CB})(1-D) = 0 \quad (38)$$

$$2V_{in}D + V_{in}(1-D) + (V_{in} - V_{CC})(1-D) = 0 \quad (39)$$

$$2V_{in}D + V_{in}(1-D) + (V_{in} - V_{CD})(1-D) = 0 \quad (40)$$

Voltage V_{C1} and V_{C2} can be derived as follows by substituting V_{CA} and V_{CB} in equations (37), (38), (39) and (40).

$$V_{C1} = V_{CA} + V_{CC} = \frac{4}{1-D} V_{in} \quad (41)$$

$$V_{C2} = V_{CB} + V_{CD} = \frac{4}{1-D} V_{in} \quad (42)$$

The output voltage will be equal to the sum of the voltage across the output capacitors C_1 and C_2.

$$V_O = V_{C1} + V_{C2} = \frac{8}{1-D} V_{in} \quad (43)$$

The voltage conversion ratio M of this converter can be obtained as follows:

$$M = \frac{V_O}{V_{in}} = \frac{8}{1-D} \quad (44)$$

4.2 Voltage stress on Semiconductor Components

The voltage ripples on the capacitors can be ignored to simplify the voltage stress on the switches and diodes of the proposed converter. The voltage stresses on active power switches S_1, S_2, S_3 and S_4 can be obtained directly as shown in the following equation:

The voltage stress on the active power switches can be expressed as

$$V_{S1max} = V_{S2\max} = V_{S3\max} = V_{S4\max} = \frac{V_{in}}{1-D} \quad (45)$$

$$V_{S1max} = V_{S2\max} = V_{S3\max} = V_{S4\max} = \frac{V_O}{8} \quad (46)$$

From (46), it can be seen that the voltage stress of the active switches of the proposed converter is equal to one eighth of the output voltage. As a result, lower voltage rating devices are used which enables to further reduce both switching and conduction losses.

The open circuit voltage stress of diodes D_{1A}, D_{2A}, D_{1B}, D_{2B}, D_{1C}, D_{2C}, D_{1D}, and D_{2D} can be obtained directly as shown in equation (47) and (48)

$$V_{D1A\max} = V_{D1B\max} = V_{D1C\max} = V_{D1D\max} = \frac{V_O}{2} \quad (47)$$

$$V_{D2B\max} = V_{D2D\max} = \frac{V_O}{2}$$
$$V_{D2A\max} = V_{D2C\max} = \frac{V_O}{4} \quad (48)$$

From (47) and (48) it is clear that the maximum resulting voltage stress of diodes is equal to $V_O/2$. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

4.3 Characteristic of Uniform Input Inductor Current Sharing

State space averaging technique is utilized to get the averaged state equations as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - (1-D)V_{CA} \quad (49)$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} - (1-D)V_{CB} \quad (50)$$

$$L_3 \frac{di_{L3}}{dt} = V_{in} - (1-D)V_{CC} \quad (51)$$

$$L_4 \frac{di_{L4}}{dt} = V_{in} - (1-D)V_{CD} \quad (52)$$

State space equations of auxiliary capacitors can be expressed as follows:

$$C_A \frac{dvC_A}{dt} = \frac{(1-D)\left[RC_AC_3 - C_PC_Q(V_{C1}+V_{C2})\right]}{RC_R} \quad (53)$$

$$C_B \frac{dvC_B}{dt} = \frac{(1-D)\left[RC_BC_4 - C_PC_Q(V_{C1}+V_{C2})\right]}{RC_R} \quad (54)$$

$$C_C \frac{dvC_C}{dt} = \frac{(1-D)\left[RC_CC_5 - C_PC_Q(V_{C1}+V_{C2})\right]}{RC_R} \quad (55)$$

$$C_D \frac{dvC_D}{dt} = \frac{(1-D)\left[RC_DC_6 - C_PC_Q(V_{C1}+V_{C2})\right]}{RC_R} \quad (56)$$

Where

$$\begin{pmatrix} C_{eq1}I_{L1}(C_2+C_B) - C_{eq2}I_{L2}C_1 \\ +C_{eq3}I_{L3}(C_2+C_D) - C_{eq4}I_{L4}C_1 \end{pmatrix} = C_3 \quad (57)$$

$$\begin{pmatrix} C_{eq2}I_{L2}(C_1+C_A) - C_{eq1}I_{L1}C_2 \\ +C_{eq4}I_{L4}(C_1+C_C) - C_{eq3}I_{L3}C_2 \end{pmatrix} = C_4 \quad (58)$$

$$\begin{pmatrix} C_{eq3}I_{L3}(C_2+C_D) - C_{eq4}I_{L4}C_1 \\ +C_{eq1}I_{L1}(C_1+C_B) - C_{eq2}I_{L4}C_1 \end{pmatrix} = C_5 \quad (59)$$

$$\begin{pmatrix} C_{eq4}I_{L4}(C_1+C_C) - C_{eq3}I_{L3}C_2 \\ +C_{eq2}I_{L2}(C_1+C_A) - C_{eq1}I_{L1}C_2 \end{pmatrix} = C_6 \quad (60)$$

$$C_AC_BC_CC_D = C_P \quad (61)$$

$$C_{eq1} + C_{eq2} + C_{eq3} + C_{eq4} = C_Q \quad (62)$$

$$C_{eq1}C_{eq2}C_{eq3}C_{eq4} = C_R \quad (63)$$

$$C_1 \frac{dv_{C1}}{dt} = \frac{(1-D)C_1(C_AI_{L2}R + C_CI_{L4}R) - C_T(V_{C1}+V_{C2})}{C_{eq1}C_{eq3}R} - \frac{D(V_{C1}+V_{C2})}{R} \quad (64)$$

$$C_2 \frac{dv_{C2}}{dt} = \frac{(1-D)C_2(C_BI_{L1}R + C_DI_{L3}R) - C_T(V_{C1}+V_{C2})}{C_{eq2}C_{eq4}R} - \frac{D(V_{C1}+V_{C2})}{R} \quad (65)$$

Where $C_T = C_A+C_B+C_C+C_D$
$C_{eq1} = C_1C_A + C_1C_B + C_AC_B$
$C_{eq2} = C_2C_A + C_2C_B + C_AC_B$
$C_{eq3} = C_1C_C + C_1C_D + C_CC_D$
$C_{eq4} = C_2C_C + C_2C_D + C_CC_D$

Where i_{L1}, i_{L2}, i_{L3}, i_{L4}, v_{CA}, v_{CB}, v_{CC}, v_{CD}, v_{C1}, v_{C2} denotes average state space values. I_{L1}, I_{L2}, I_{L3}, I_{L4}, V_{CA}, V_{CB}, V_{CC}, V_{CD}, V_{C1} and V_{C2} denote corresponding DC values.

$$I_o = \frac{(V_{C1}+V_{C2})}{R} \quad (66)$$

By selecting $C_1 = C_2 = C_X$, $C_A = C_B = C_C = C_D = C_Y$, one can get the corresponding dc solutions as follows:

$$I_{L1} = I_{L2} = I_{L3} = I_{L4} = \left(\frac{4}{1-D} + \frac{DC_Y}{(1-D)C_X}\right)I_o \quad (67)$$

4.4 Performance Comparison

The proposed converter is compared with some recent high step-up as shown in Table I. Table I summarizes the voltage gain and steady state characteristics of four different converter topologies. From Table 1, it is clear that the proposed converter achieves higher voltage gain and reduced semiconductor stress than conventional topologies of high gain converters.

Table 1
Comparison of the steady state characteristics of four different converter topologies

Gain/ Stress	Voltage doubler [17]	High step up converter [18]	Ultra high step up converter [27]	Proposed Converter
Voltage Gain	$\frac{2}{(1-D)}$	$\frac{(3-D)}{(1-D)}$	$\frac{(3+D)}{(1-D)}$	$\frac{8}{1-D}$
Voltage stress on switch	$\frac{1}{2}$	$\frac{1}{3-D}$	$\frac{2}{3-D}$	$\frac{1}{8}$
Voltage Stress on diode	1	$\frac{2}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{2}$
Number of MOS-FET	2	2	1	4
Number of Inductor	2	2	2	4
Number of Diode	2	3	5	8
Number of capacitor	2	3	4	6

Therefore, the proposed converter is rather suitable for use in applications requiring high step-up voltage gain. The proposed converter achieves reduced voltage stress for the active switches and the diodes. As a result high efficiency can be achieved with proper design, and reduced switch components.

5. Simulation results

The proposed converter is analyzed for a power rating of 1700 W with an input voltage of 32 V and 1024 V output**,** as shown in Fig. 1. The switching frequency is chosen to be 40 kHz. The duty ratios of S_1, S_2, S_3 and S_4 equal to 0.75 and the corresponding component parameters can be obtained in Table 2.

Due to the low switch voltage stress of the proposed converter, four power MOSFETs rating of 150 V and conductive resistance of 0.1Ω, is used. Similarly, eight diodes with low forward voltage drop of 0.8 volts are chosen. The interleaved structure can effectively increase the switching frequency with reduced ripples in the input and output and so is the size of the energy storage inductors.

Table 2: Component parameters of the proposed converter

Components	Specification
Boost Inductors L_1, L_2, L_3, L_4	323.9 µH
Blocking Capacitors C_A,C_B,C_C,C_D	31.19 µH
Output Capacitor C_1,C_2	769.2 µH

The measured input voltage is 32 V, and the output voltage is 1024 V. The pulse patterns of the switches S_1, S_2, S_3 and S_4 are shown in Fig. 6. It can be observed that S_1 and S_3 are fired at same time whereas S_2 and S_4 are triggered at 180 ° phase shift. Fig.6 shows the switching pulses to all the four switches. The gating signals are given with 180° phase shift.

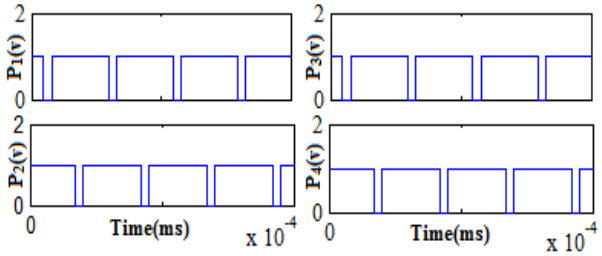

Fig.6. Pulse pattern to the Switches S_1, S_2, S_3 and S_4

Fig. 7 shows the four-phase inductor current waveforms of the simulation results. Since input current I_{in} is equal to the sum of I_{L1}, I_{L2}, I_{L3}, I_{L4} it is obvious that with the four-phase interleaving control, both input current ripples and switch conduction losses can be reduced.

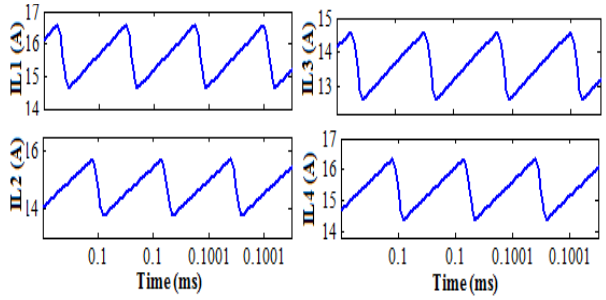

Fig.7. Waveforms of inductors current I_{L1}, I_{L2}, I_{L3} and I_{L4}

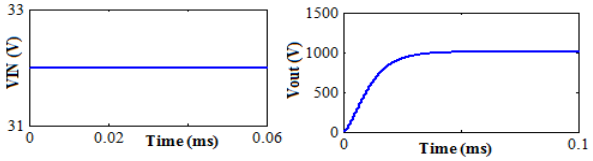

Fig.8. Waveforms of Input and Output Voltages

Fig. 8 shows the input and output voltage waveforms of the proposed converter. To check the validity of the capacitor voltage stress, waveforms of output capacitors and blocking capacitors are recorded as shown in Fig. 9 and 10.

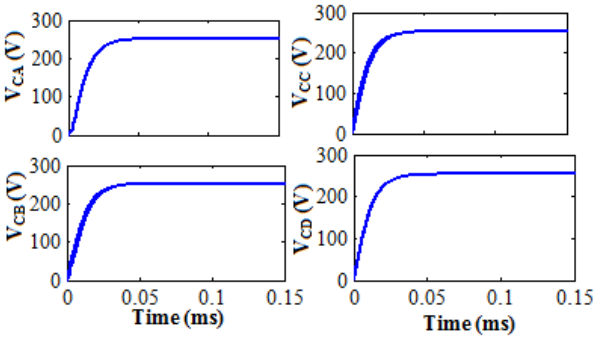

Fig.9. Waveforms of the voltage across the blocking capacitors (a) C_A (b) C_B (c) C_C (d) C_D

From Figure 9 and 10, it can be seen that, with the proposed converter, the voltage stresses of the output capacitors and blocking capacitors are indeed equal to one half and one fourth of the output voltage, respectively.

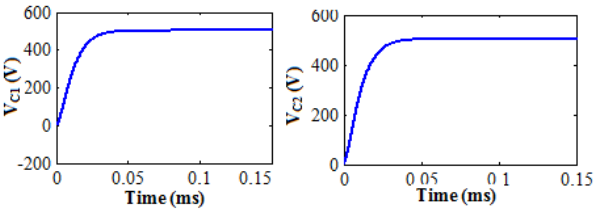

Fig.10. Waveforms of the voltage across the output capacitors

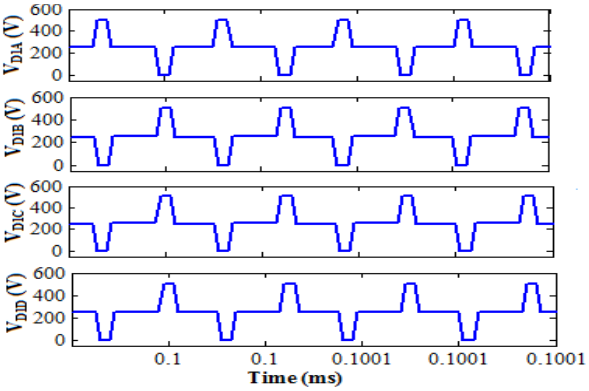

Fig.11. Waveforms of the voltage stress of V_{D1A}, V_{D1B}, V_{D1C} and V_{D1D}

Also, to check the voltage stress of blocking capacitors, one can see when the proposed converter is operated in modes 2 and 4, the voltages of capacitors C_A and C_B are clamped at $Vin\ (1-D)$, and when the proposed converter is operated in modes 1 and 3, all diodes are OFF, and capacitors C_A, C_B, C_C and C_D are isolated as open circuits; hence, the

voltages of capacitors C_A, C_B, C_C and C_D are kept constant. Also, the output loading is mainly supplied by capacitors C_1 and C_2.

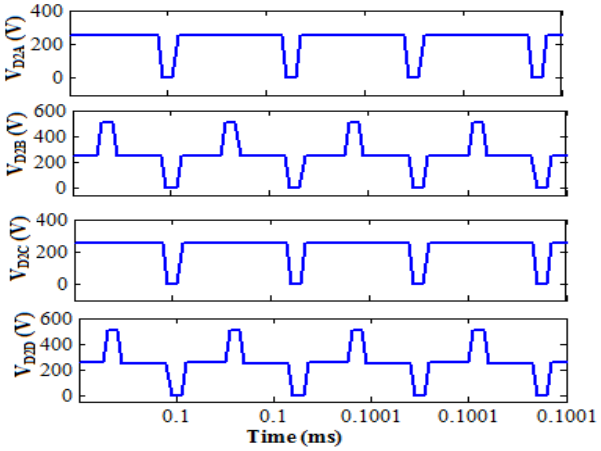

Fig.12. Waveforms of the voltage stress of V_{D2A}, V_{D2B}, V_{D2C} and V_{D2D}

The diode voltage waveforms of the simulation results are shown in Fig. 11 and 12, which indicates that the maximum voltage cross diodes V_{D1A}, V_{D1B}, V_{D1C},V_{D1D},V_{D2D} and V_{D2B} equals 200 V which is indeed equal to one-half of the output voltage. The maximum voltage crosses diode V_{D2A} *and* V_{D2C} is 100 V which is equal to one fourth of the output voltage as expected. Therefore, the voltages across C_A, C_B, C_C and C_D can be maintained at constant values though C_A, C_B, C_C and C_D are with rather small capacitance.

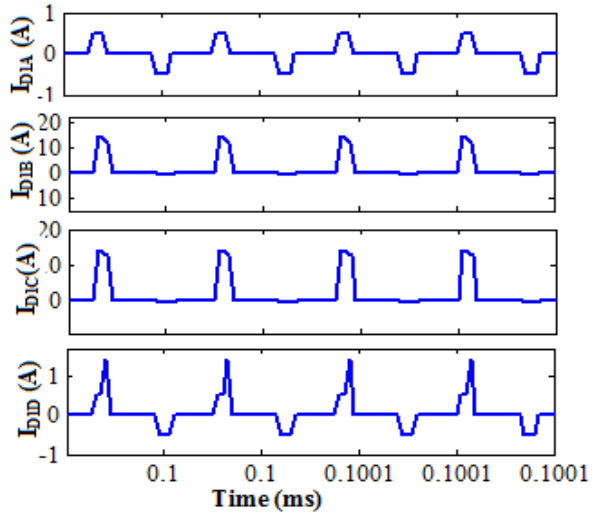

Fig.13. Waveforms of the current flowing through of I_{D1A}, I_{D1B}, I_{D1C} *and* I_{D1D}

The diode current waveforms of the simulation results are shown in Fig. 13 and 14. In the proposed topology, low-voltage-rating rectifier diodes are used to reduce the conduction loss. Due to the help of the blocking capacitor, the output current ripples are reduced. By analyzing the power losses distribution, it can be concluded that the major losses come from the active switches, the diodes, and the input inductors

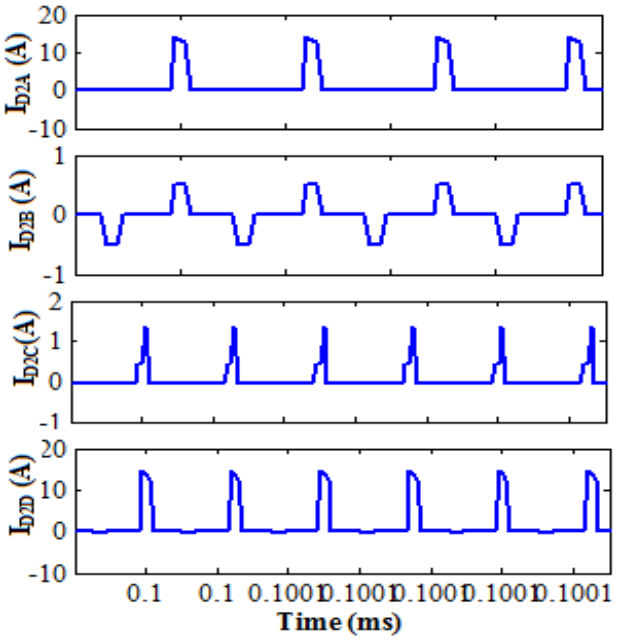

Fig.14. Waveforms of the current flowing through of I_{D2A}, I_{D2B}, I_{D2C} and I_{D2D}

From Fig. 15, it is observed that the voltage stress of the active switches is equal to one fourth of the output voltage

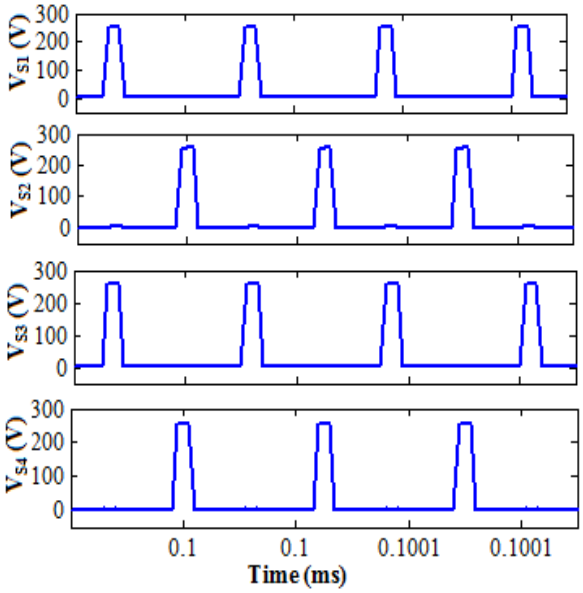

Fig.15. Waveforms of the voltage stress of switches V_{S1}, V_{S2}, V_{S3} and V_{S4}

6. Conclusion

In this paper, a four phase transformer-less adjustable voltage quadrupler DC–DC converter with high voltage transfer gain without adopting an extreme large duty cycle and reduced semiconductor voltage stress is proposed. The proposed topology

utilizes input-parallel output-series configuration. The proposed converter not only reduces the voltage stress of the switches and diodes but also achieves high step-up voltage gain. Both switching and conduction losses are reduced by choosing lower voltage rating MOSFETs and diodes. In addition, there is an automatic uniform current sharing characteristic due to the charge balance of the blocking capacitor, without adding any additional complex circuits. The operation principle with detailed steady analysis is presented. With many good features such as high gain, reduced voltage stress, reduced ripples and high efficiency, it can be concluded that the proposed converter is highly suitable for high step-up voltage gain applications. The results of simulations run by Matlab software validate the performance of the converter. The proposed system with advanced control algorithm can be used for interfacing with PV applications.

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