A Novel High Performance CMOS Cascoded Operational Amplifier for Process Instrumentation Based Applications

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Abstract— In this contribution, we present an efficient CMOS based operational amplifier which uses an arrangement to provide an extra bias current into a conventional CMOS differential input signals. This technique enhances the slew rate of an operational amplifier for a given quiescent current. The design of a high performance CMOS operational amplifier (op-amp) with level 3 parameters at 0.2µm CMOS technology, that makes the use of stacked (cascode) current source techniques. This innovative approach benefits the chances operated by full complementary implementations of well known sub-circuits, to enhance the speed of such an operational amplifier and to better organize and economize layout generation. Unlike conventional techniques such as the cascoding, which increases the gain by increasing the output resistance, the replica-amp technique increases the gain by matching the main and the replica amps. Among the advantages of the replica op-amp technique are low supply, high swing, and effectiveness with resistive loads. The maximum operating clock frequency of the sample-and-hold sub-module increases from 290 kHz to 1 MHz with a hold capacitor of 1 nF and dissipates a static power of 7.5 mW. The PSpice simulations of the op-amp shows a unity gain bandwidth of 40 MHz and a DC gain of 72 dB, when using a bias current of 100 µA and a load capacitance of 15 pF.

Keywords: *Standard CMOS op-amp, Circuit, design methodology, transistor sizing, optimization,Op-Amp, Slew Rate, Optimized Amplifier, CMOS, Cascoded,PSpice Simulation,*

I. INTRODUCTION

The settling time of an operational amplifier is one of its key parameters. Although it is difficult to be determined analytically, it can be stated that the settling time is a composite parameter, which is affected by the slew rate and the frequency response [1, 2]. For a specified capacitive load, input voltage step, and power dissipation, there always appears to be a physical limit to the settling time in a given technology. Above all, this is true for the part determined by the frequency response, which is usually the final part of the step response before the amplifier completely settles and where the small-signal behavior prevails [3]. The initial part of the step response behavior is, however, governed by the large-signal properties of the amplifier: the amplifier slews after a differential step has been applied to its input. The slewing rate is given by the maximum available current to charge up all the capacitances (including load and compensation capacitors):

$$S_R = \frac{I_{max}}{C_{tot}} \quad (1)$$

Thus, for a given capacitance, the power consumption imposes a definite limit to the slew rate. A possible solution to circumvent this limit is to use some kind of class-B input stage [4], controlled input stage [5], adaptive biasing [6], or dynamic biasing [7].

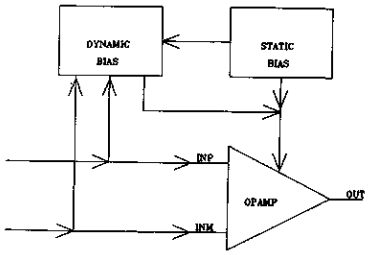


Figure 1: Basic Schematic Approach of Op-Amp

If a large differential signal has been detected, the bias current is temporarily increased in order to enhance the slew rate. This technique necessarily requires some extra circuitry, and this circuitry must fulfill the following requirements i.e. a small chip area, low power dissipation, and no degradation of the electrical characteristics of the underlying operational amplifier (noise, input impedance, offset, etc.). It is the last requirement that is especially hard to meet [8, 9]. The static-biasing circuit supplies the current during the small-signal operation and thus determines the small-signal properties of the operational amplifier (the dynamic bias is OFF). Only large differential signals at the input can turn the dynamic bias ON. Hence, the small-signal characteristics remain unaffected except for the input capacitance, which is slightly increased owing to the additional input differential stage. As it will be seen later, the load of this stage is low impedance when the dynamic bias is OFF, and thus there is no Miller effect [10, 12].

A high performance op-amp was developed by merging the single-ended stacked mirror op-amp and the high drive class AB output stage described above. The complete transistor schematic of the enhanced op-amp. It comprises the circuit which has a large output resistance and thus a high gain, and the output buffer stage [13]. The dominant pole p_1 is located at a frequency ω_1 determined by the total output resistance R_o and the load capacitance C_L. The ω_1 frequency is determined as:

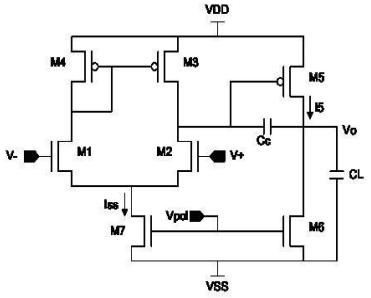
$$\omega_1 = \frac{1}{R_o C_L} \quad (2)$$

The non-dominant pole p_2 is determined by the first stage input resistance R_i, and the input capacitance to the current gain stage C_i. The non-dominant pole frequency ω_2 is approximately determined by [14]:

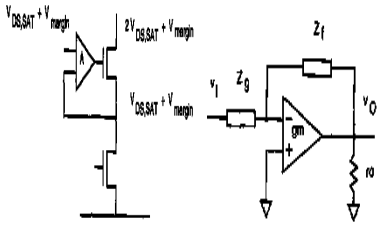
$$\omega_2 = \frac{1}{R_i C_i} \tag{3}$$

provided $r_o >> R_i$, where r_o is the output resistance of the input stage.

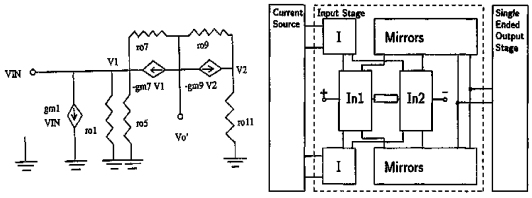
II. BASIC OPERATIONAL AMPLIFIERS CIRCUITS& OPERATION



(a)



(b)



(c)

Figure 2 Possible Configurations of Op-Amp (a) Standard Op-Amp (b) Active Cascode Circuit & Inverting Op-Amp (c) Folded Cascoded Circuit & Standard Block of Op-Amp

The figure (1a) shows the schematic arrangement of a standard operational amplifier, figure (1b), shows the possible combinations of the active cascode circuit of operational amplifier with the inverting configuration and figure (1c) shows the folded low frequency model & the block representation of the traditional operational amplifier. The low frequency small signal model of the folded-cascode approach is shown in fig (1c), whose DC gain is given as [15, 16]:

$$\begin{aligned} A_v &= -g_{m1}(r_{011} r_{09} g_{m9} \| r_{07} g_{m7} (r_{01} \| r_{05})) \\ A_v &= -g_{m1} R'_{out} \end{aligned} \tag{4}$$

And the transfer function of this approach of the operational amplifier is given as:

$$\frac{V_o(S)}{V_{in}(S)} = \frac{-g_{m1} g_{m12} (1 + SC_c R_c)}{(SC_L + g_{m12} g_{o13})(SC_c (1 + G'_{out} R_c) + G'_{out})} \tag{5}$$

On solving this above expression, the zero which is added to the system's transfer function so as to improve the phase margin of the operational amplifier is given as [17]:

$$Z = -\frac{1}{C_c R_c} \tag{6}$$

and the two possible poles are:

$$P_1 = -\frac{1}{R'_{out} C_c (1 + \frac{R_c}{R'_{out}})} \approx -\frac{1}{R'_{out} C_c} \tag{7}$$

$$P_2 = -\frac{(g_{m12} + g_{o13})}{C_L} = -\frac{1}{R'_{out} C_L} \approx -\frac{g_{m12}}{C_L} \tag{8}$$

Also the slew rate of the standard operational amplifier is given by the maximum available current to charge up all the capacitances i.e. [18]

$$S_R = \frac{I_{max}}{C_c} \tag{9}$$

The dynamic analysis of the standard operational amplifier gives the mathematical behavior of various parameters say dc gain, bandwidth and the slew rate [19, 20].

$$A_o \cong \frac{g_{m1,2} g_{m5}}{(g_{ds1,2} g_{ds3,4})(g_{ds5} + g_{ds6})} \tag{10}$$

$$GB \cong \frac{g_{m1,2}}{C_c} \tag{11}$$

where the compensating capacitor is given as:

$$C_c \cong \frac{C_L}{Q^2} \frac{g_{md} g_{m5}}{(g_{m5} - g_{md})^2} \tag{12}$$

And Q is the resonance factor of the op-amp with a unity gain feedback.

III. PROPOSED HIGH PERFORMANCE OPERATIONAL AMPLIFIER

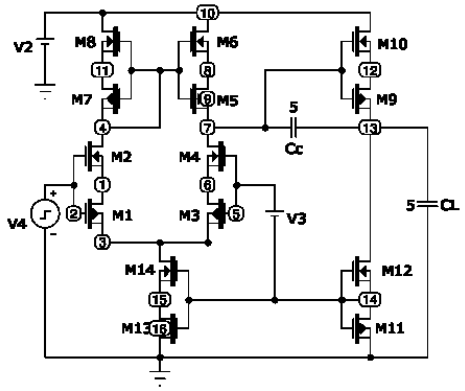


Figure 3 Proposed Circuit of High Performance Operational Amplifier

A high performance op-amp circuit has been designed and put forward with its best performance. The complete schematic arrangement of the circuit is shown in above figure 3. It comprises of the CMOS devices, which has a large output resistance and thus a high gain. The transistors M17 and M20 are used to bias M18 and M19 which drive the push-pull output stage, where as M22, M21 and M23 transistors has a low W/L ratio and thus, acts as a large linear resistor. The output stage of the circuit is biased such that the current flowing through M22 is matched by the current in M21 during quiescent operation. The biasing transistors are controlled by the high frequency gain stage and provide the necessary inputs for the push-pull output stage. The minimum value for the load capacitance which provides the dominant pole compensation is given as [21, 25]

$$C_L = C_i R_i g_{m1} A_i \tag{13}$$

where gm1 is the transconductance of the input stage and Ai is the current gain. Generally, some of the dominant parameters of the circuit such as power consumption are imposed and must be fixed during the design and implementation process. The designing steps and procedure of sizing of the transistors are classically obtained after determining the saturation drain source voltage determined by V_{ONi} for transistor (T_i). Based on this concept, one can determine the most required and dominant parameters of the op-amp as [26, 28]:

$$I_{ss} \cong \frac{P}{(V_{DD} - V_{SS})(1+m)} \tag{14}$$

where m is the bias current modulation factor between the differential and the gain stage of the circuit.

$$m = \frac{I^{bias}_{5}}{I_{ss}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_7} \tag{15}$$

The slewing-rate of the op-amp is determined as the maximum available current required to charge up all capacitances (i.e. the compensation capacitance load C_C) i.e. [29, 30]

$$S_R = \frac{\mathrm{I}_{max}}{C_C} \tag{16}$$

Thus , based on this above relation, the value and the performance of the I_{max} can be easily enhanced and improved since the C_C is always kept constant for this particular approach and design.

$$\mathrm{I}_{max} = I_{D4}(V_{G4\max}) = \frac{K_4}{2}\left((V_{DD} - V_{Th3}) - V_{Th2}\right)^2 \tag{17}$$

The variation in the capacitive load will vary the unity gain bandwidth as desired by the circuit design and performance of the 3 dB gain amplifier. The differential input stage of the circuit performs the differential-to-single ended conversion with the help of the transistors M6, M7 [31, 32].

The output stage of the circuit is based on a novel approach of design that provides solution so as to provide the driven capability of a simple inverter stage with an accurate current control. In quiescent condition, the transistors M17, M18 are in cut-off mode, and M 16, M19 are in saturation region, which perform a highly linear operation of the amplifier. As the gate of the transistor M13 increases, say in the positive direction, the current i_{DM13} becomes equal to bias current, and the transistor M14 and M16 turns off and the gate of M16 is driven close to V_{SS}. Thus, transistor the transistor M17 turns on and delivers a high current to the output load [33, 35].

IV. SIMULATION RESULTS & DISCUSSION

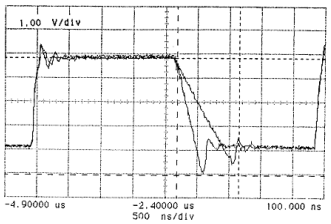


Figure 4 Step Response of the Op-amp

The simulation of the proposed ciruit has been done by using pSPICE software with 0.18µn CMOS technology with level 3 modeled parameters for the best possible performance. The above figure 4 shows the step response of the proposed op-amp with and without effetct of the enhancement circuit having the total load capacitance of approximately 10pF i.e functioning as the feedback loop and the load of the circuit. The average positive slew rate for both circuits is about 55V/µs and the negative slew rate is 54V/µsec with 5pF capacitor and 8.5V/µs and 9.0V/µs for a capacitive load of 10pF. This behaviour of the high performance op-amp simulation results is shown in figure 5 (a & b).

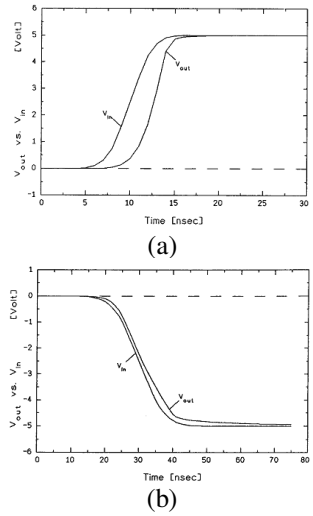


Figure 5 Slew Rate of the Op-amp (a) Positive (b) Negative

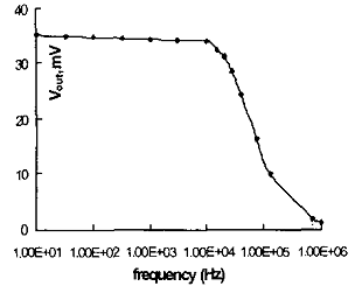


Figure 6 Frequency Response

The above figure 6 shows the frequency response of the high performance op-amp circuit with a bandwith of approx 3 db that provides a approx value of frequency as 30 KHz.

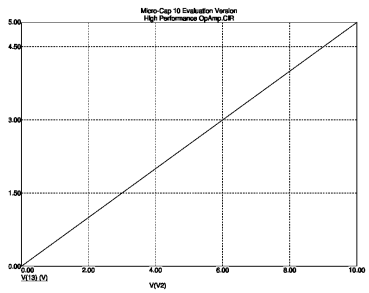


Figure 7 DC Analysis of Op-amp

The above figure 7 shows the dc analyzing behavior of the proposed circuit which reflects that the amplifier has got minimized or almost optimized noise or distortion free performance since it replicated the input at the put with minimum possible noise and delay.

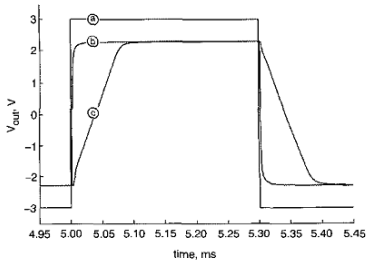


Figure 8 Time Response of Op-amp

The above figure 8 shows the transient or simply time response of the circuit with different possible capacitive loads. It reflects clearly that the behavior of the signal at the capacitive load output almost follow the step input applied at the input with minimum possible distortion.

V. CONCLUSION

In this discussion an innovative approach and methodology has been proposed using CMOS. The proposed approach of performance is basically depends upon the mathematical modeling of the parameters of the CMOS and then simulation of the same using level 3 pSPICE model of 0.18µn CMOS technology. The key advantages of this proposed circuit is to implement a high performance op-amp circuit that can be most suitably used in the design of analog integrated circuits and high frequency switch-capacitor filters. The main and the desired features of this innovative circuit is that it performs as per the modeled parameters and provides the results as shown in table 1.

TABLE I. **MODELED PARAMETERS FOR PROPOSED CIRCUIT**

Op-amp Parameters	Without Dynamic Bias		With Dynamic Bias	
Supply Voltage (V)	±2.7		±2.7	
Static Power (mW)	13.0		14.0	
Power Supply Rejection Ratio at DC (db)	100 for VDD 115 for VSS		100 for VDD 115 for VSS	
CMRR at DC (db)	94		94	
Input Bias Current (pA)	2.1		2.1	
Input Common-Mode Range	-1.72 to +2.2 V		-1.72 to +2.2 V	
Maximum Output Swing (V)	±2.0		±2.0	
Output Impedance (Ω)	205		205	
Open Loop DC gain (db)	100.5		100.5	
Offset Voltage (mV)				
Load Capacitance →	05 pF	10 pF	05 pF	10 pF
Slew Rate (V/µs) (Positive) (Negative)	55 54	8.5 9.0	2665 2100	415 430
Unity Gain Bandwidth (MHz)	52	29.3	54	29

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