A Simple and Generalized SVPWM Control of Cascaded H-Bridge Multilevel Inverters

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***Abstract* – This paper presents an automatic switching pattern generation for multilevel cascaded H-Bridge inverters with equal dc voltage sources, based on the space-vector pulse width modulation (SVPWM) techniques. The proposed switching strategy generates a voltage vector with very low harmonic distortion and reduced switching frequency. This new control method is an attractive alternative to the classic multilevel pulse width modulation techniques considering the following aspects, mainly, minimization of voltage and current total harmonic distortion (THD), extension of range of linear operation; and least number of commutations. To solve the problem of computational complexity in multilevel inverters due to the large number of space vectors and redundant switching states, a simple and general space vector PWM algorithm is proposed. Based on this algorithm, the location of the reference voltage vector can be easily determined and the calculation of dwell times becomes very simple. It is also mentioned that this method requires lower memory spaces as there is no need of any look-up table. To verify the algorithms, a seven-level cascaded H-bridge inverter drive system was constructed and simulation results are present here.**

Keywords: Multi-level inverter, SVPWM, redundant states, Diode clamped inverter, THD, Cascaded H-Bridge inverter, PWM.

I. INTRODUCTION

MULTILEVEL power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concern, and low switching losses. The research on the multilevel inverter has been receiving wide attention mainly due to its capability of high voltage operation without switching devices connected in series. In addition, with the increase of voltage levels, the inverter output contain less harmonics and will eventually approach a desired sinusoidal waveform. Therefore, the multilevel inverters have been selected as a preferred power converter topology for high voltage and high power applications. Among all the switching algorithms proposed in the literature for multilevel converters, space vector modulation (SVM) seems most promising since it offers a great flexibility in optimizing switching pattern design and it is also well suited for digital implementation. The space vector modulation for more than three-level inverters is very complex due to the high number of space vectors and redundant switching states. The total number of switching states (N_s) for general N level inverter is $N_s = N^P$ where P is number of phases. The actual number of voltage space vectors called active voltage vectors given by NV = $N^3 - (N-1)^3$ and the remaining switching states are redundant switching states.

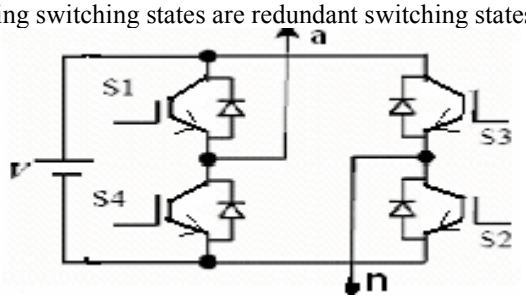

Fig.1. Power circuit of single H-Bridge cell

For example, there are 343 switching states in a three phase, 7-level inverter, which correspond to 127 active voltage vectors. *N*. Celanovic has proposed a fast SVM algorithm [7], but the dwell time calculations seem complex due to the use of Euclidean vector space representation. In addition, the selection of the switching states in the inverters of higher than three levels seems not well documented. B.S. Suh proposed a good PWM calculation method for three-level inverter [6], but it is difficult to apply it to higher level inverters. Sanmin Wei and Bin Wu also proposed a good generalized algorithm but large, small and medium switching state determination techniques is not easy and well documented. In this paper, a general space vector algorithm is proposed, which has unique features. As space vector in m-n axis is decomposed in integer scale, which makes an angle of pi/3, it is easy to find out coordinates of any space vectors. The unique features of the proposed algorithm are:

- The algorithm is very simple, effective and easy to implement. The location of the reference voltage vector and the dwell times of the space vectors can be calculated very easily.
- For a particular reference voltage it is easy to determine all the redundant switching states and automatically determine

the status of switching states whether it is large, small or medium.

- More interesting is that to obtain minimum harmonics distortion proper switching pattern selection is very important. The proposed algorithm automatically generates that pattern which need not require any look-up table, hence minimizing the memory requirement.
- The proposed algorithm is general and can be used in any high-level cascaded H-bridge inverters with least modifications.

II. CASCADED H-BRIDGE INVERTER

A. Working Principle

Fig. 1 shows the single cell of multilevel-cascaded H- Bridge configuration. The output of this cell will have three levels namely *+V, 0* and *–V*. The switch position and the output voltage and the state of the H-Bridge are given in table I. using one single H-Bridge, a three level inverter can be realized. These H-Bridge cells can be connected in cascade to obtain multilevel-cascaded H-Bridge inverter. The power circuit of seven-level cascaded H-Bridge inverter is shown in fig.2. If *V* is the dc voltage of each H-Bridge cell, then a five level inverter phase voltage will have five levels, namely *+2V, +V, 0, -V* and *–2V*. Similarly, seven level inverter will have *+3V, +2V, +V, 0, -V, -2V* and *-3V*. A five-level cascaded H-Bridge inverter requires two H-Bridges. A seven-level cascaded H-Bridge inverter requires three H-Bridges. In general a *N*-level inverter requires *(N-1)/2* H-Bridge cells in each phase and phase voltage will have *N* levels.

TABLE I. SWITCH STATUS AND STATE OF H-BRIDGE

Switch status	Output voltage (Volts)	State
S1 and S2 ON; S3 and S4 OFF	V	+1
S1 and S3 ON; S2 and S4 OFF OR S2 and S4 ON; S1 and S3 OFF	0	0
S3 and S4 ON; S1 and S2 OFF	-V	-1

B. Features of Cascaded H-Bridge Inverter

- Higher voltage levels can be synthesized using devices of low voltage rating. If *V* is the dc voltage of each of the H-Bridge cell, then each device will experience a off-state voltage of *V* volts and a *N*-level cascaded H–Bridge can synthesize peak-to-peak voltage of *(N*V)* volts. Phase voltage of an *N*–level cascaded H-Bridge will have *N* levels; hence wave shape will be improved and will result in improved THD. Improved wave shape can be obtained even with fundamental frequency switching and step modulation.
- Low switching frequency will result in reduced switching loss in the devices. The switching angle of each cell can be selected to eliminate some of the lower order harmonics.
- In the above explanation, each cascaded H-bridge with equal voltage is employed. However cells with different voltages

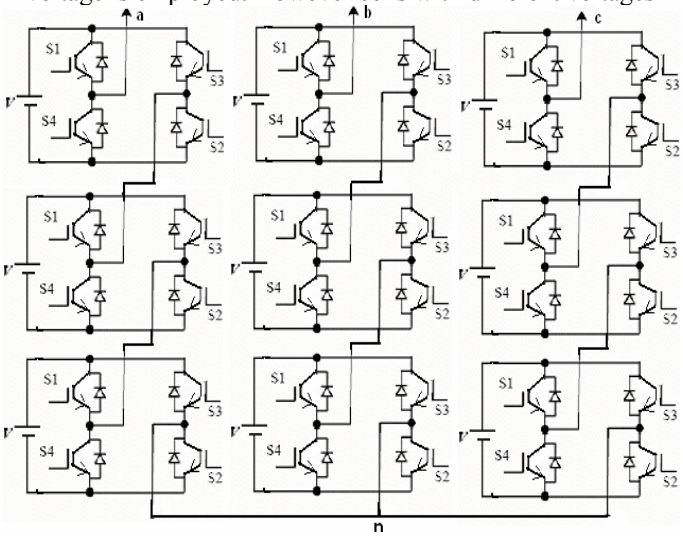

Fig.2. Power Circuit of seven –level cascaded H-Bridge inverter

can also be used. By proper selection of the voltage levels, some of the lower order harmonics can be eliminated.

- Modular structure makes the power circuit design simple and reliable. Under fault conditions, faulty cells can be bypassed and still the inverter will function with reduced output voltage levels. Since the cells are identical, faulty unit can be replaced quickly and downtime of the inverter can be reduced; hence high reliability can be achieved [3].
- Since the voltage across each cell is *V* volt, voltage upto *N*V* volts with large number of steps are available with lower harmonics content and *dv/dt* stress on switches are also decreased.
- The main disadvantage of this topology is that each H-Bridge cell requires an isolated dc source. The isolated sources are typically provided from transformer/rectifier arrangements.

C. Pre-treatment of the Basic Vectors

A typical seven-level cascaded H-bridge inverter is shown in Fig.2, where a separate dc power supply is used for each H-Bridge. Its corresponding space voltage vector diagram is illustrated in Fig.3, in which the vectors for the 3, 5, and 7-level inverters are also illustrated. For the 7-level inverter, there are 216 small triangles and the vertex of each triangle represents a space vector.

The hexagonal vectors can be divided into six major triangular sectors (*I* to *VI*). Only the first sector of the coordinate is used because the vectors located in the other sectors can be transformed to first sector by clockwise rotating by an angle of *k*(pi/3) k* = (1,2,3,4,5 for sector 2 to 6). As all the

sectors are identical, only details of sector I is given in Fig.4. Usually, a *(M+1)*-level inverter is discussed here as shown in Fig.4. By decomposing V_{ref} into m and n axis it is easy to obtain the *m* and *n* axis component of V_{ref} as V_{rm} and V_{rn} as given next:

$$Vrm = (2*M*Vref/3Vdc)\ \sin(\pi/3 - \theta) \quad (1)$$

$$Vrn = (2*M*Vref/3Vdc)\ \sin(\theta) \quad (2)$$

Where θ is speed of rotating reference vector.

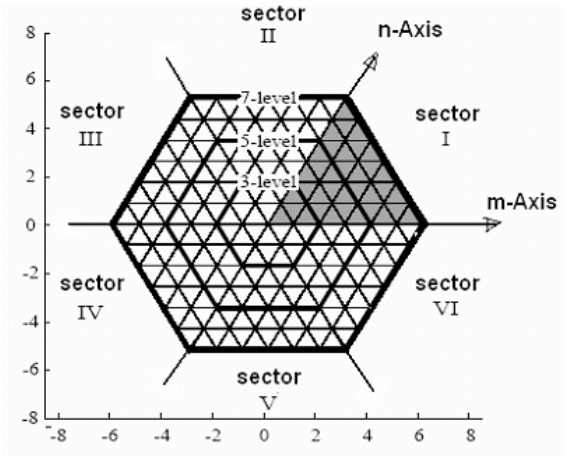

Fig. 3. Voltage vectors of 3,5 and 7-level voltage source inverters.

III. PROPOSED ALGORITHM

A. *Determination of Location of Reference Vector:*

As the number of levels is increased, the number of triangle increases in this way: $N_T = 6(N-1)^2$.

For example a 7-level inverter, total number of triangle is 216, but the selection of triangle by the proposed method is very simple and generalized. Any space vector located in any sector and in any triangle can be calculated easily from θ and the value *Vrm* and *Vrn* explained below. Assuming *Vref* and θ should be such that it lies in the rectangular area specified by DEGF shown in Fig. 4. After calculating V_{rm} and V_{rn}, calculate the lower rounded integer value (*m* and n) as shown below:

Say, V_{rm} = 2.6 & V_{rn} = 1.85.

Assuming m= int (2.6) = 2 & n = int (1.85) = 1

These m and n are defined by vector (m , n) in m-n axis. If (V_{rm} + V_{rn}) <= (m+n+1) then *Vref* located in the left bottom triangle DEF, otherwise the triangle EFG.

B. *Dwelling Time Calculation*

The dwelling time calculation for each switching state is very simple and generalized. Suppose at any instant the *Vref* located in the Triangle GEF shown in Fig.4. The corresponding three nearest space vectors are (m_1, n1), (m_2, n2) and (m_3, n3). According to voltage-time balance equation it can be solve three dwelling time T_1, T_2, and T_3 as follows:

$$n_1*T_1 + n_2*T_2 + n_3*T_3 = T_{pwm}*V_{rn} \quad (3)$$

$$m_1*T_1 + m_2*T_2 + m_3*T_3 = T_{pwm}*V_{rm} \quad (4)$$

Where T_{PWM} is PWM time period.

The method demonstrated how simple it is to determine the triangle that reference voltage falls in and to calculate the dwell times. More importantly, the algorithm has another few features:

a) It is a general algorithm, which can be used for inverters with any number of voltage levels up to seven level and eventually can extend beyond seven level with some modification of inverter power circuit;

b) There are only two sets of equations for dwell time calculation. Compared with the Cartesian coordinate system where there are many sets of different equations for the Calculation of the dwell time.

c) The proposed algorithm considers over-modulation case also. It is easy to judge whether SVPWM is in over-modulation region or not, simply by checking the following inequality:

if (V_{rm} + V_{rn}) > *M*, it becomes over-modulation.

A useful method to handle this situation is to multiply the original vector say V_{rm} and V_{rn} by a factor $M / (V_{rm} + V_{rn})$ and the consequent steps are same as discussed.

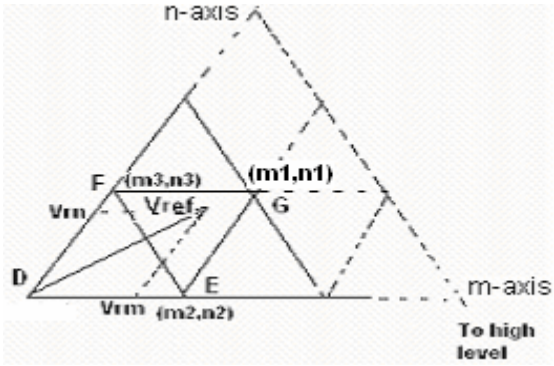

Fig.4. Decomposition of Reference voltage in m-n axis

C. G*eneral Relationship between Space Vector and Switching States*

In the multilevel inverters, a space voltage vector can be represented by more than one switching state. For instance, space vector (1, 1) in Fig. 5. has five redundant switching states composed [-1,-2,-3], [0,-1,-2], [1,0,-1],[2,1,0] and [3,2,1], all of which produce an output voltage with the same magnitude and phase angle. With the increase in the voltage levels, there exist more redundant switching states. It is

desirable to find a general expression which describes the relationship between space vectors and their corresponding switching states for any cascaded H-Bridge multilevel inverter. Space vectors in the 60°coordinate system shown in Fig. 4 can be generally expressed by (*m, n*), where *m = 1, 2, ….., 2p,*

and *n = 1, 2…, 2p*. The integer number p is defined by,

p = (N – 1) /2, where *N* is the number of phase voltage levels of the inverter, which is always an odd number for the cascaded H-bridge inverter.

The relationship between a space vector *(m, n)* and its switching states for three phases [*Sa*, *Sb*, *Sc*] is obtained by a detailed study on all the possible states in a multilevel inverter.

The results are given by

$$S_a = \ -p,\ -p+1, -p+2,\ \ldots\ldots\ldots,\ p \tag{6}$$

$$S_b = S_a - m \tag{7}$$

$$S_c = S_b - n \tag{8}$$

For a given space vector *(m, n)* the number of switching states can be obtained by

$$N_{SW} = N - (m + n) \tag{9}$$

These equations are the general expression of switching states and can be applied to any cascaded multi-level inverter up to seven levels.

Alternatively for a given space vector (*m, n*), all of its switching states can also be calculated by

$$S_a = (m+n-p),(m+n-p+1),\ldots\ldots,p \tag{10}$$

$$S_b = (n-p),(n-p+1),\ldots\ldots\ldots,(p-m) \tag{11}$$

$$S_c = (-p),(-p+1),\ldots\ldots\ldots\ldots(p-m-n) \tag{12}$$

TABLE II: RELATIONSHIP BETWEEN SWITCHING STATES IN VARIOUS SECTORS

Sector	Switching states of Phase A,B and C		
	Sa	Sb	Sc
I	Sa	Sb	Sc
II	- Sb	-Sc	-Sa
III	Sc	Sa	Sb
IV	-Sa	-Sb	-Sc
V	Sb	Sc	Sa
VI	-Sc	-Sa	- Sc

IV. SELECTION OF SWITCHING STATES

In the multilevel inverter, the redundant switching states increase with the voltage level. For example, the 5, 7, and 9-level inverters have the redundant states of 4, 6 and 8, respectively for zero voltage vectors. In the diode clamped multilevel inverters, the redundant switching states can be utilized to balance the voltage of capacitors in the dc link. The cascaded H-Bridge inverter inherently does not have this problem. In this paper, the redundancy is employed to minimize the voltage harmonic distortion only.

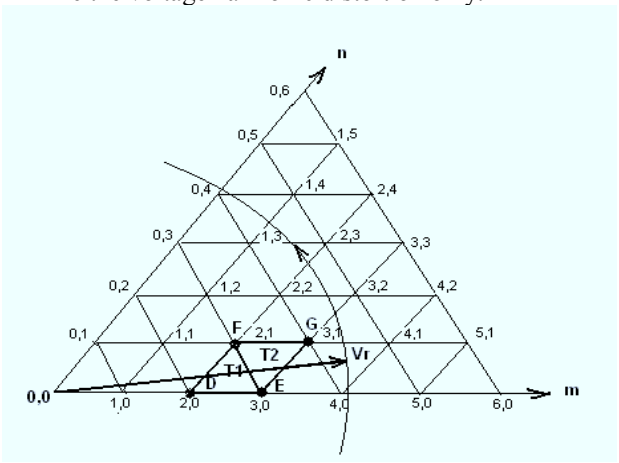

Fig.5. Graphical Representation of proposed Algorithm

A. Determinations of Mean, Small and Large Switching States

Any space vectors *(m, n)* in Fig. 5.can be classified into the following two categories:

Category 1: *even vector* – the sum of its coordinates (m, n) is an even number;

If both m and n are even number or both is odd then the corresponding switching state is mean state and this switching states can be expressed as:

$$S_{am} = \{(m+n-p)+p\}/2 = (m+n)/2 \tag{13}$$

$$S_{bm} = \{(n-p)+(p-m)\}/2 = (n-m)/2 \tag{14}$$

$$S_{cm} = \{(-p)+(p-m-n)\}/2 = -(m+n)/2 \tag{15}$$

Where S_{am}, S_{bm} and S_{cm} are mean switching states for phase A, B, and C.

For an even vector, each component of its mean switching state is an integer, and the state can be implemented. For instance, space vector (1,1) in Fig.5 has five states: [−1,−2,−3], [0,−1,−2], [1,0,−1], [2,1,0] and [3,2,1]. It is a mean state and its mean state is [1, 0, −1], which can be realized by the inverter with output voltages of, $S_a = 1$, $S_b = 0$ and $S_c = -1$. However, for an odd vector where *(m + n)* and *(m - n)* is an odd number, its mean state cannot be implemented since the inverter cannot produce half-level voltages. In this case, a small or large switching state can be used.

Category 2: *odd vector* – the sum of its coordinates (*m* and *n*) is an odd number.

Case 1: If m is odd and n is even it should be large state, can be expressed as

$$S_{al} = (m+n+1)/2 \tag{16}$$

$$S_{bl} = (n - m + 1)/2 \quad (17)$$

$$S_{cl} = -(m + n - 1)/2 \quad (18)$$

Case 2: If m is even and n is odd it should be small states expressed as:

$$S_{as} = (m + n - 1)/2 \quad (19)$$

$$S_{bs} = (n - m - 1)/2 \quad (20)$$

$$S_{cs} = (m + 1 + 1)/2 \quad (21)$$

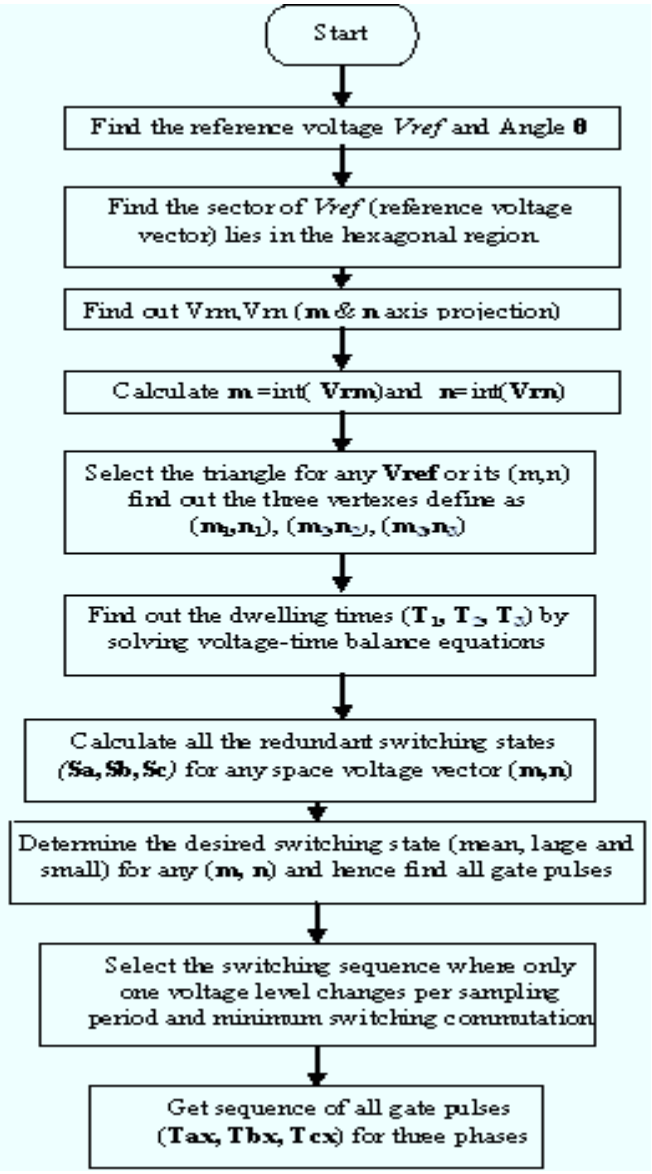

Fig. 6. Flowchart of proposed algorithm

B. Selection of Switching States

To minimize the voltage harmonic distortion, the arrangement of switching states is as follows:

According to the value of three nearest space vector (m_1, n_1), (m_2, n_2) and (m_3, n_3) of a triangle, the corresponding switching states are automatically selected from large number of redundant state, which is extremely simple and easy to implement and also gives excellent harmonic performance. Simulation results shown later illustrate the inverter phase voltage as well as line voltage which obviously contain much less harmonics compared to other existing multi-level techniques.

C. Switching Sequence Design

The switching sequence design has to meet a number of requirements such as:

a) Minimize the number of switching per sampling period,

b) One voltage level change per commutation of switching devices, and

c) Adoption of the above mentioned method. For example, when the reference vector lies in triangles T_1 and T_2 of a particular rectangular area DEGF, shown in Fig. 5, switching sequence for T_1 and T_2 are given in Fig.6, where D, E, F and G are the vertexes (space vectors) of the triangles DEF and EFG. The number in each column in Fig.7 (a). represents the switching states of a given space vector at F,D and E point and T_F,T_D and T_E are the dwelling time of those point respectively for three-phases.

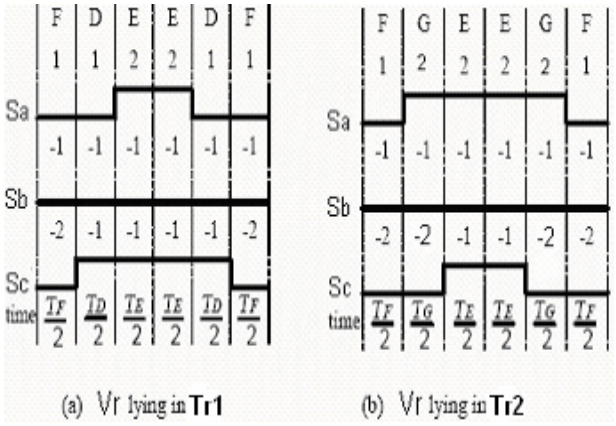

Fig. 7. Switching Pattern for reference Voltage Vector V_r Located in the Triangle DEF and Triangle EFG

V. SIMULATION RESULTS AND DISCUSSION

The simulation results are presented. The proposed algorithm has several attractive features. The output voltage is compatible with load as different voltage ranges are obtained by simply changing the modulation index (m_i). Fig.8 and Fig.9 show the output phase voltage and IM stator current at modulation index (mi) of 0.8. Fig. 10 shows the line voltage for m_i = 0.8. For equal dc voltage in the input, maximum output has of seven levels and wave shape is near sinusoidal.

The same can be verified even for lower modulation index of m_i = 0.4. It shows that the exixting seven level inverter now behaves as a four level inverter and simulation results of line voltage, phase voltage and line current are shown in the figure 11, 12 and 13. From the simulation results it is clear that the proposed cascaded seven level inverter work satisfactorily even for very small modulation indexes. Though the THD increases and some distortion in phase voltage generates.

The V_{LTHD} of line voltage has value 5.74 % only, for m_i = 0.8.From Fig.10, it is clear that except fundamental other lower order harmonics has lower magnitude. Hence there is no need of filter circuit.

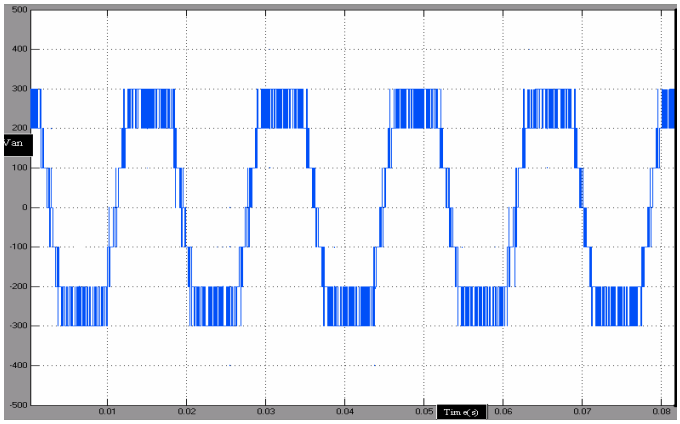

Fig.8. Output Phase Voltage of Seven-level inverter for modulation index (mi) = 0.8

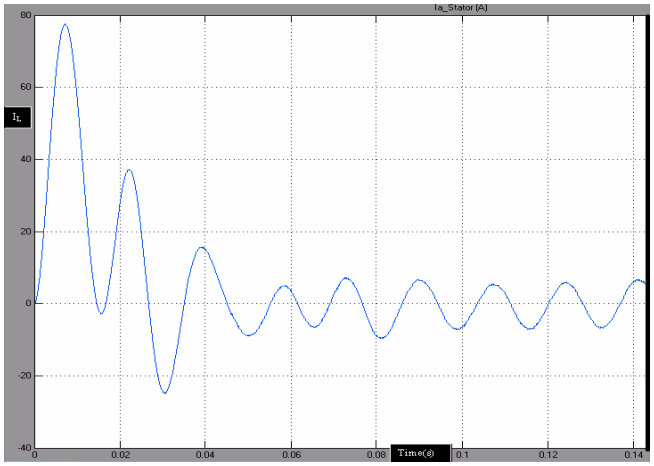

Fig.9. Output line current to IM load for m_i = 0.8 of seven-level inverter

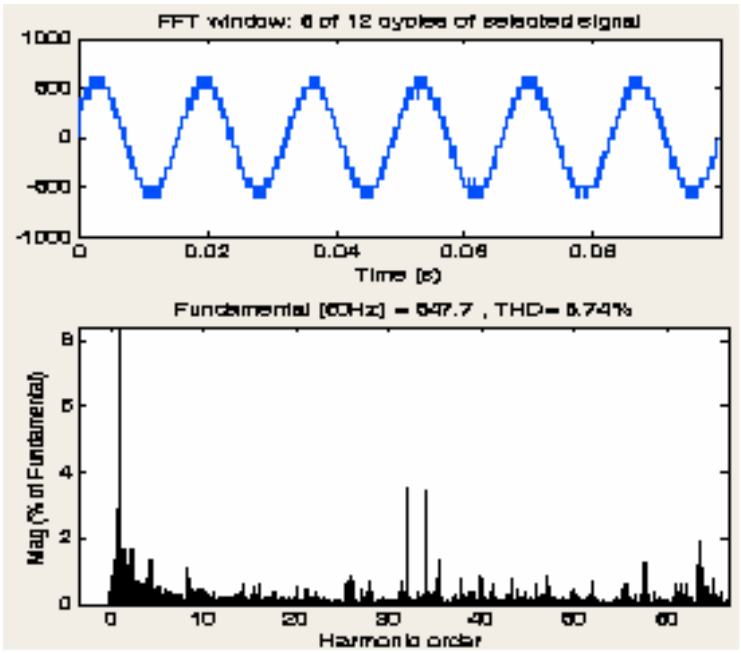

Fig.10. Output Line Voltage of Seven Level Inverter and its FFT analysis for m_i = 0.8

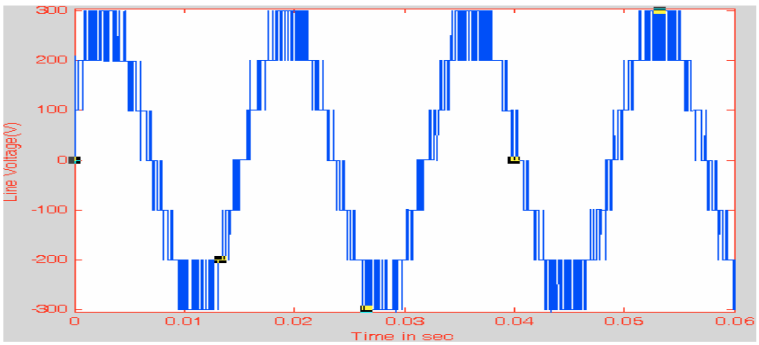

Fig.11. Output Line Voltage of seven Level Inverter for mi=0.4

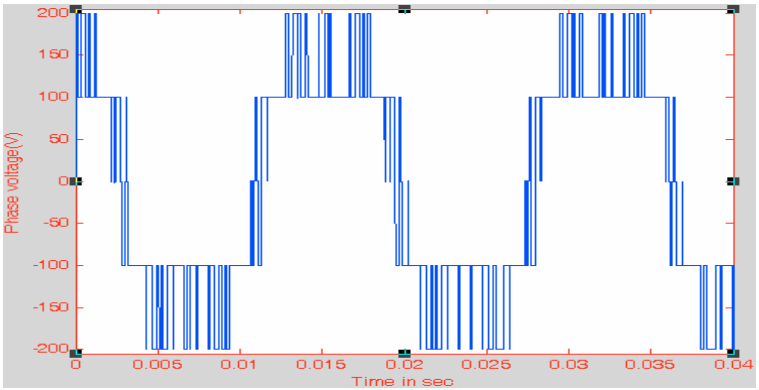

Fig.12. Output Phase Voltage of seven Level Inverter for mi=0.4

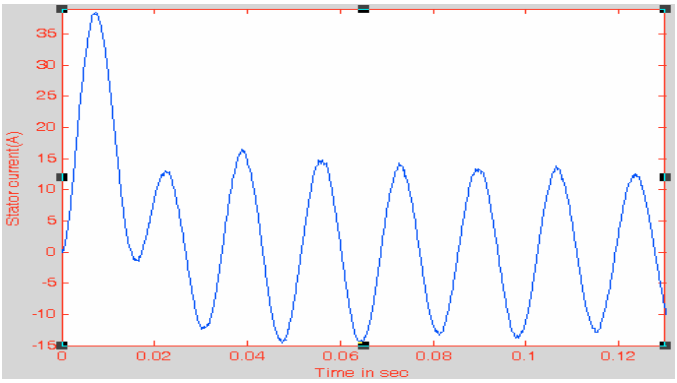

Fig.13. Output line current to IM of seven Level Inverter for mi=0.4

VI. CONCLUSIONS

A simple and general space vector PWM algorithm has been proposed in this paper. The power circuit is designed to have modular structure. All the H-Bridge units are identical. So replacing the faulty units will be easy and quick. The proposed algorithm substantially simplifies the calculation of space vectors and their corresponding dwell times. Based on the proposed algorithm, the generation of automatic switching pattern for the cascaded H-Bridge multilevel inverters has been developed. This algorithm features easy implementation and more importantly, minimum harmonic content in the inverter output voltage and current of the Induction Motor Load. The most important aspect of the proposed algorithm lies in its generality. This can be used in any high-level cascaded H-bridge inverters. This algorithm is verified through MATLAB/SIMULINK simulations.

INDEX:

Type of Load: IM
Rating of Load: 5 HP, 460 V, 60 Hz, 1750 rpm
Stator Resistance and Inductance: 0.01965 p.u and 0.0397 p.u.
Rotor Resistance and Inductance: 0.01909 p.u and 0.0397 p.u.
Mutual Inductance: 1.359 p.u.
Sampling time Ts=2e-6 sec
Switching frequency Fc=1980 Hz.

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***Abstract* – This paper presents an automatic switching pattern generation for multilevel cascaded H-Bridge inverters with equal dc voltage sources, based on the space-vector pulse width modulation (SVPWM) techniques. The proposed switching strategy generates a voltage vector with very low harmonic distortion and reduced switching frequency. This new control method is an attractive alternative to the classic multilevel pulse width modulation techniques considering the following aspects, mainly, minimization of voltage and current total harmonic distortion (THD), extension of range of linear operation; and least number of commutations. To solve the problem of computational complexity in multilevel inverters due to the large number of space vectors and redundant switching states, a simple and general space vector PWM algorithm is proposed. Based on this algorithm, the location of the reference voltage vector can be easily determined and the calculation of dwell times becomes very simple. It is also mentioned that this method requires lower memory spaces as there is no need of any look-up table. To verify the algorithms, a seven-level cascaded H-bridge inverter drive system was constructed and simulation results are present here.**

Keywords: Multi-level inverter, SVPWM, redundant states, Diode clamped inverter, THD, Cascaded H-Bridge inverter, PWM.

I. INTRODUCTION

MULTILEVEL power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concern, and low switching losses. The research on the multilevel inverter has been receiving wide attention mainly due to its capability of high voltage operation without switching devices connected in series. In addition, with the increase of voltage levels, the inverter output contain less harmonics and will eventually approach a desired sinusoidal waveform. Therefore, the multilevel inverters have been selected as a preferred power converter topology for high voltage and high power applications. Among all the switching algorithms proposed in the literature for multilevel converters, space vector modulation (SVM) seems most promising since it offers a great flexibility in optimizing switching pattern design and it is also well suited for digital implementation. The space vector modulation for more than three-level inverters is very complex due to the high number of space vectors and redundant switching states. The total number of switching states (N_s) for general N level inverter is $N_s = N^P$ where P is number of phases. The actual number of voltage space vectors called active voltage vectors given by NV = $N^3 - (N-1)^3$ and the remaining switching states are redundant switching states.

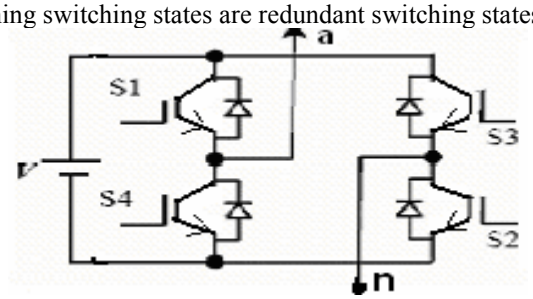

Fig.1. Power circuit of single H-Bridge cell

For example, there are 343 switching states in a three phase, 7-level inverter, which correspond to 127 active voltage vectors. *N*. Celanovic has proposed a fast SVM algorithm [7], but the dwell time calculations seem complex due to the use of Euclidean vector space representation. In addition, the selection of the switching states in the inverters of higher than three levels seems not well documented. B.S. Suh proposed a good PWM calculation method for three-level inverter [6], but it is difficult to apply it to higher level inverters. Sanmin Wei and Bin Wu also proposed a good generalized algorithm but large, small and medium switching state determination techniques is not easy and well documented. In this paper, a general space vector algorithm is proposed, which has unique features. As space vector in m-n axis is decomposed in integer scale, which makes an angle of pi/3, it is easy to find out coordinates of any space vectors. The unique features of the proposed algorithm are:

- The algorithm is very simple, effective and easy to implement. The location of the reference voltage vector and the dwell times of the space vectors can be calculated very easily.
- For a particular reference voltage it is easy to determine all the redundant switching states and automatically determine

the status of switching states whether it is large, small or medium.

- More interesting is that to obtain minimum harmonics distortion proper switching pattern selection is very important. The proposed algorithm automatically generates that pattern which need not require any look-up table, hence minimizing the memory requirement.
- The proposed algorithm is general and can be used in any high-level cascaded H-bridge inverters with least modifications.

II. CASCADED H-BRIDGE INVERTER

A. Working Principle

Fig. 1 shows the single cell of multilevel-cascaded H- Bridge configuration. The output of this cell will have three levels namely *+V, 0* and *–V*. The switch position and the output voltage and the state of the H-Bridge are given in table I. using one single H-Bridge, a three level inverter can be realized. These H-Bridge cells can be connected in cascade to obtain multilevel-cascaded H-Bridge inverter. The power circuit of seven-level cascaded H-Bridge inverter is shown in fig.2. If *V* is the dc voltage of each H-Bridge cell, then a five level inverter phase voltage will have five levels, namely *+2V, +V, 0, -V* and *–2V*. Similarly, seven level inverter will have *+3V, +2V, +V, 0, -V, -2V* and *-3V*. A five-level cascaded H-Bridge inverter requires two H-Bridges. A seven-level cascaded H-Bridge inverter requires three H-Bridges. In general a *N*-level inverter requires *(N-1)/2* H-Bridge cells in each phase and phase voltage will have *N* levels.

TABLE I. SWITCH STATUS AND STATE OF H-BRIDGE

Switch status	Output voltage (Volts)	State
S1 and S2 ON; S3 and S4 OFF	V	+1
S1 and S3 ON; S2 and S4 OFF OR S2 and S4 ON; S1 and S3 OFF	0	0
S3 and S4 ON; S1 and S2 OFF	-V	-1

B. Features of Cascaded H-Bridge Inverter

- Higher voltage levels can be synthesized using devices of low voltage rating. If *V* is the dc voltage of each of the H-Bridge cell, then each device will experience a off-state voltage of *V* volts and a *N*-level cascaded H–Bridge can synthesize peak-to-peak voltage of *(N*V)* volts. Phase voltage of an *N*–level cascaded H-Bridge will have *N* levels; hence wave shape will be improved and will result in improved THD. Improved wave shape can be obtained even with fundamental frequency switching and step modulation.
- Low switching frequency will result in reduced switching loss in the devices. The switching angle of each cell can be selected to eliminate some of the lower order harmonics.
- In the above explanation, each cascaded H-bridge with equal voltage is employed. However cells with different voltages

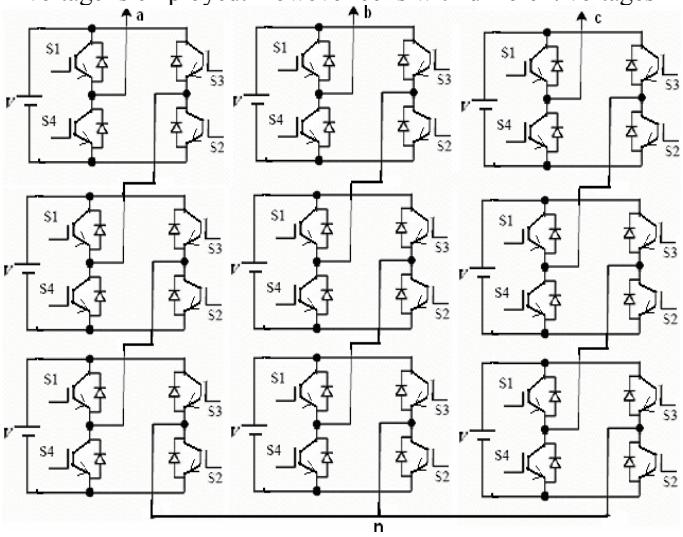

Fig.2. Power Circuit of seven –level cascaded H-Bridge inverter

can also be used. By proper selection of the voltage levels, some of the lower order harmonics can be eliminated.

- Modular structure makes the power circuit design simple and reliable. Under fault conditions, faulty cells can be bypassed and still the inverter will function with reduced output voltage levels. Since the cells are identical, faulty unit can be replaced quickly and downtime of the inverter can be reduced; hence high reliability can be achieved [3].
- Since the voltage across each cell is *V* volt, voltage upto *N*V* volts with large number of steps are available with lower harmonics content and *dv/dt* stress on switches are also decreased.
- The main disadvantage of this topology is that each H-Bridge cell requires an isolated dc source. The isolated sources are typically provided from transformer/rectifier arrangements.

C. Pre-treatment of the Basic Vectors

A typical seven-level cascaded H-bridge inverter is shown in Fig.2, where a separate dc power supply is used for each H-Bridge. Its corresponding space voltage vector diagram is illustrated in Fig.3, in which the vectors for the 3, 5, and 7-level inverters are also illustrated. For the 7-level inverter, there are 216 small triangles and the vertex of each triangle represents a space vector.

The hexagonal vectors can be divided into six major triangular sectors (*I* to *VI*). Only the first sector of the coordinate is used because the vectors located in the other sectors can be transformed to first sector by clockwise rotating by an angle of *k*(pi/3) k* = (1,2,3,4,5 for sector 2 to 6). As all the

sectors are identical, only details of sector I is given in Fig.4. Usually, a *(M+1)*-level inverter is discussed here as shown in Fig.4. By decomposing V_{ref} into m and n axis it is easy to obtain the *m* and *n* axis component of V_{ref} as V_{rm} and V_{rn} as given next:

$$Vrm = (2*M*Vref/3Vdc)\ \sin(\pi/3 - \theta) \quad (1)$$

$$Vrn = (2*M*Vref/3Vdc)\ \sin(\theta) \quad (2)$$

Where θ is speed of rotating reference vector.

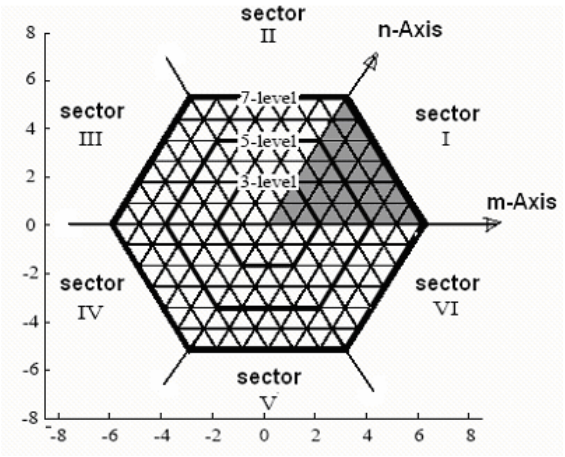

Fig. 3. Voltage vectors of 3,5 and 7-level voltage source inverters.

III. PROPOSED ALGORITHM

A. Determination of Location of Reference Vector:

As the number of levels is increased, the number of triangle increases in this way: $N_T = 6(N-1)^2$.

For example a 7-level inverter, total number of triangle is 216, but the selection of triangle by the proposed method is very simple and generalized. Any space vector located in any sector and in any triangle can be calculated easily from θ and the value *Vrm* and *Vrn* explained below. Assuming *Vref* and θ should be such that it lies in the rectangular area specified by DEGF shown in Fig. 4. After calculating V_{rm} and V_{rn}, calculate the lower rounded integer value (*m* and n) as shown below:

Say, V_{rm} = 2.6 & V_{rn} = 1.85.

Assuming m= int (2.6) = 2 & n = int (1.85) = 1

These m and n are defined by vector (m , n) in m-n axis. If (V_{rm} + V_{rn}) <= (m+n+1) then *Vref* located in the left bottom triangle DEF, otherwise the triangle EFG.

B. Dwelling Time Calculation

The dwelling time calculation for each switching state is very simple and generalized. Suppose at any instant the *Vref* located in the Triangle GEF shown in Fig.4. The corresponding three nearest space vectors are (m_1, n1), (m_2, n2) and (m_3, n3). According to voltage-time balance equation it can be solve three dwelling time T_1, T_2, and T_3 as follows:

$$n_1*T_1 + n_2*T_2 + n_3*T_3 = T_{pwm}*V_{rn} \quad (3)$$

$$m_1*T_1 + m_2*T_2 + m_3*T_3 = T_{pwm}*V_{rm} \quad (4)$$

Where T_{PWM} is PWM time period.

The method demonstrated how simple it is to determine the triangle that reference voltage falls in and to calculate the dwell times. More importantly, the algorithm has another few features:

a) It is a general algorithm, which can be used for inverters with any number of voltage levels up to seven level and eventually can extend beyond seven level with some modification of inverter power circuit;

b) There are only two sets of equations for dwell time calculation. Compared with the Cartesian coordinate system where there are many sets of different equations for the Calculation of the dwell time.

c) The proposed algorithm considers over-modulation case also. It is easy to judge whether SVPWM is in over-modulation region or not, simply by checking the following inequality:

if (V_{rm} + V_{rn}) > *M*, it becomes over-modulation.

A useful method to handle this situation is to multiply the original vector say V_{rm} and V_{rn} by a factor $M / (V_{rm} + V_{rn})$ and the consequent steps are same as discussed.

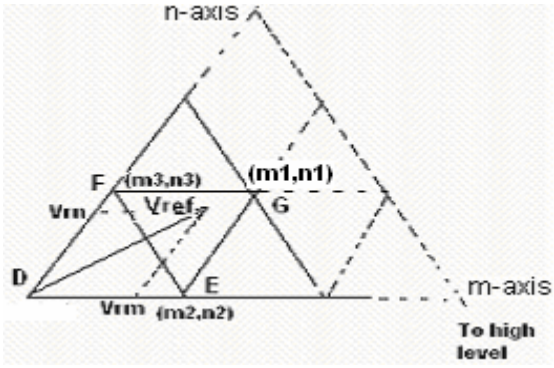

Fig.4. Decomposition of Reference voltage in m-n axis

C. General Relationship between Space Vector and Switching States

In the multilevel inverters, a space voltage vector can be represented by more than one switching state. For instance, space vector (1, 1) in Fig. 5. has five redundant switching states composed [-1,-2,-3], [0,-1,-2], [1,0,-1],[2,1,0] and [3,2,1], all of which produce an output voltage with the same magnitude and phase angle. With the increase in the voltage levels, there exist more redundant switching states. It is

desirable to find a general expression which describes the relationship between space vectors and their corresponding switching states for any cascaded H-Bridge multilevel inverter. Space vectors in the 60°coordinate system shown in Fig. 4 can be generally expressed by (*m, n*), where *m = 1, 2, ….., 2p,*

and *n = 1, 2…, 2p*. The integer number p is defined by,

p = (N – 1) /2, where *N* is the number of phase voltage levels of the inverter, which is always an odd number for the cascaded H-bridge inverter.

The relationship between a space vector *(m, n)* and its switching states for three phases [*Sa*, *Sb*, *Sc*] is obtained by a detailed study on all the possible states in a multilevel inverter.

The results are given by

$$S_a = \ -p,\ -p+1, -p+2,\ \ldots\ldots\ldots,\ p \tag{6}$$

$$S_b = S_a - m \tag{7}$$

$$S_c = S_b - n \tag{8}$$

For a given space vector *(m, n)* the number of switching states can be obtained by

$$N_{SW} = N - (m + n) \tag{9}$$

These equations are the general expression of switching states and can be applied to any cascaded multi-level inverter up to seven levels.

Alternatively for a given space vector (*m, n*), all of its switching states can also be calculated by

$$S_a = (m+n-p),(m+n-p+1),\ldots\ldots,p \tag{10}$$

$$S_b = (n-p),(n-p+1),\ldots\ldots\ldots,(p-m) \tag{11}$$

$$S_c = (-p),(-p+1),\ldots\ldots\ldots\ldots(p-m-n) \tag{12}$$

TABLE II: RELATIONSHIP BETWEEN SWITCHING STATES IN VARIOUS SECTORS

Sector	Switching states of Phase A,B and C		
	Sa	Sb	Sc
I	Sa	Sb	Sc
II	- Sb	-Sc	-Sa
III	Sc	Sa	Sb
IV	-Sa	-Sb	-Sc
V	Sb	Sc	Sa
VI	-Sc	-Sa	- Sc

IV. SELECTION OF SWITCHING STATES

In the multilevel inverter, the redundant switching states increase with the voltage level. For example, the 5, 7, and 9-level inverters have the redundant states of 4, 6 and 8, respectively for zero voltage vectors. In the diode clamped multilevel inverters, the redundant switching states can be utilized to balance the voltage of capacitors in the dc link. The cascaded H-Bridge inverter inherently does not have this problem. In this paper, the redundancy is employed to minimize the voltage harmonic distortion only.

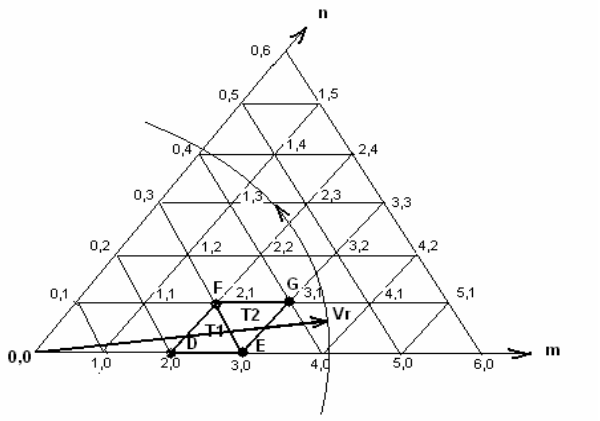

Fig.5. Graphical Representation of proposed Algorithm

A. Determinations of Mean, Small and Large Switching States

Any space vectors *(m, n)* in Fig. 5.can be classified into the following two categories:

Category 1: *even vector* – the sum of its coordinates (m, n) is an even number;

If both m and n are even number or both is odd then the corresponding switching state is mean state and this switching states can be expressed as:

$$S_{am} = \{(m+n-p)+p\}/2 = (m+n)/2 \tag{13}$$

$$S_{bm} = \{(n-p)+(p-m)\}/2 = (n-m)/2 \tag{14}$$

$$S_{cm} = \{(-p)+(p-m-n)\}/2 = -(m+n)/2 \tag{15}$$

Where S_{am}, S_{bm} and S_{cm} are mean switching states for phase A, B, and C.

For an even vector, each component of its mean switching state is an integer, and the state can be implemented. For instance, space vector (1,1) in Fig.5 has five states: [−1,−2,−3], [0,−1,−2], [1,0,−1], [2,1,0] and [3,2,1]. It is a mean state and its mean state is [1, 0, −1], which can be realized by the inverter with output voltages of, $S_a = 1$, $S_b = 0$ and $S_c = -1$. However, for an odd vector where *(m + n)* and *(m - n)* is an odd number, its mean state cannot be implemented since the inverter cannot produce half-level voltages. In this case, a small or large switching state can be used.

Category 2: *odd vector* – the sum of its coordinates (*m* and *n*) is an odd number.

Case 1: If m is odd and n is even it should be large state, can be expressed as

$$S_{al} = (m+n+1)/2 \tag{16}$$

$$S_{bl} = (n - m + 1)/2 \quad (17)$$

$$S_{cl} = -(m + n - 1)/2 \quad (18)$$

Case 2: If m is even and n is odd it should be small states expressed as:

$$S_{as} = (m + n - 1)/2 \quad (19)$$

$$S_{bs} = (n - m - 1)/2 \quad (20)$$

$$S_{cs} = (m + 1 + 1)/2 \quad (21)$$

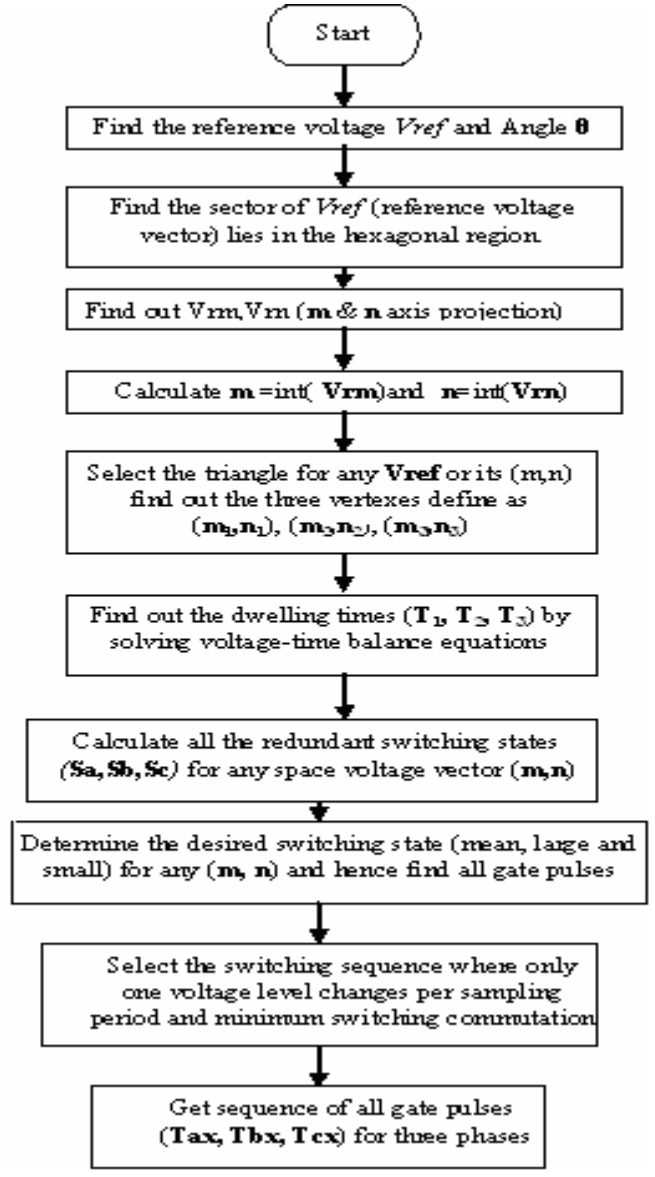

Fig. 6. Flowchart of proposed algorithm

B. Selection of Switching States

To minimize the voltage harmonic distortion, the arrangement of switching states is as follows:

According to the value of three nearest space vector (m_1, n_1), (m_2, n_2) and (m_3, n_3) of a triangle, the corresponding switching states are automatically selected from large number of redundant state, which is extremely simple and easy to implement and also gives excellent harmonic performance. Simulation results shown later illustrate the inverter phase voltage as well as line voltage which obviously contain much less harmonics compared to other existing multi-level techniques.

C. Switching Sequence Design

The switching sequence design has to meet a number of requirements such as:

a) Minimize the number of switching per sampling period,

b) One voltage level change per commutation of switching devices, and

c) Adoption of the above mentioned method. For example, when the reference vector lies in triangles T_1 and T_2 of a particular rectangular area DEGF, shown in Fig. 5, switching sequence for T_1 and T_2 are given in Fig.6, where D, E, F and G are the vertexes (space vectors) of the triangles DEF and EFG. The number in each column in Fig.7 (a). represents the switching states of a given space vector at F,D and E point and T_F,T_D and T_E are the dwelling time of those point respectively for three-phases.

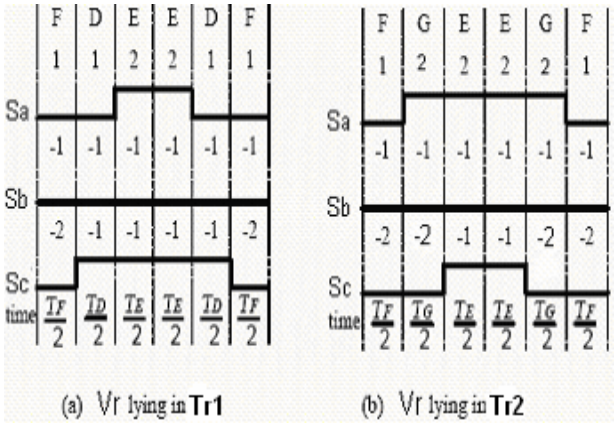

Fig. 7. Switching Pattern for reference Voltage Vector V_r Located in the Triangle DEF and Triangle EFG

V. SIMULATION RESULTS AND DISCUSSION

The simulation results are presented. The proposed algorithm has several attractive features. The output voltage is compatible with load as different voltage ranges are obtained by simply changing the modulation index (m_i). Fig.8 and Fig.9 show the output phase voltage and IM stator current at modulation index (mi) of 0.8. Fig. 10 shows the line voltage for m_i = 0.8. For equal dc voltage in the input, maximum output has of seven levels and wave shape is near sinusoidal.

The same can be verified even for lower modulation index of m_i = 0.4. It shows that the exixting seven level inverter now behaves as a four level inverter and simulation results of line voltage, phase voltage and line current are shown in the figure 11, 12 and 13. From the simulation results it is clear that the proposed cascaded seven level inverter work satisfactorily even for very small modulation indexes. Though the THD increases and some distortion in phase voltage generates.

The V_{LTHD} of line voltage has value 5.74 % only, for m_i = 0.8.From Fig.10, it is clear that except fundamental other lower order harmonics has lower magnitude. Hence there is no need of filter circuit.

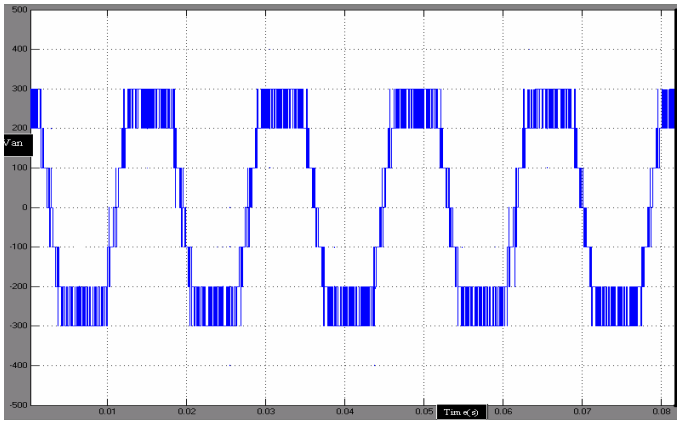

Fig.8. Output Phase Voltage of Seven-level inverter for modulation index (mi) = 0.8

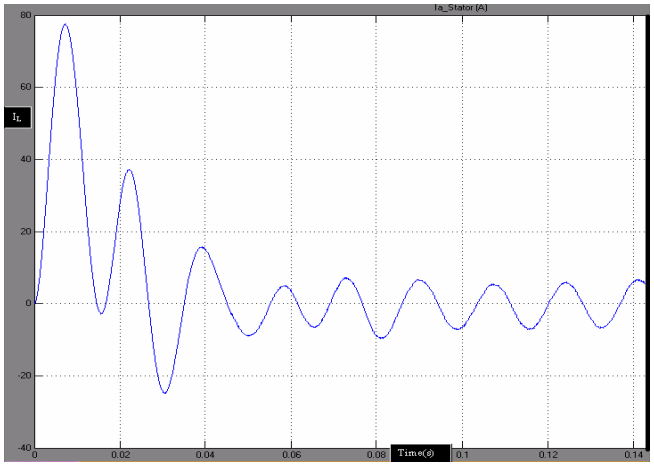

Fig.9. Output line current to IM load for m_i = 0.8 of seven-level inverter

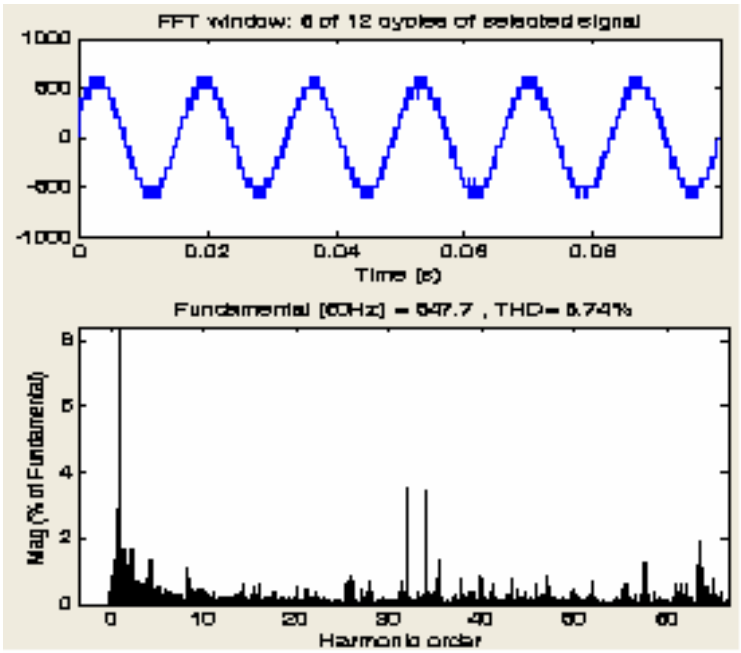

Fig.10. Output Line Voltage of Seven Level Inverter and its FFT analysis for m_i = 0.8

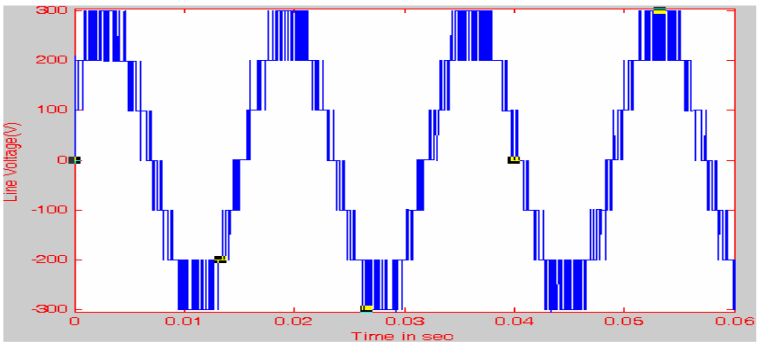

Fig.11. Output Line Voltage of seven Level Inverter for mi=0.4

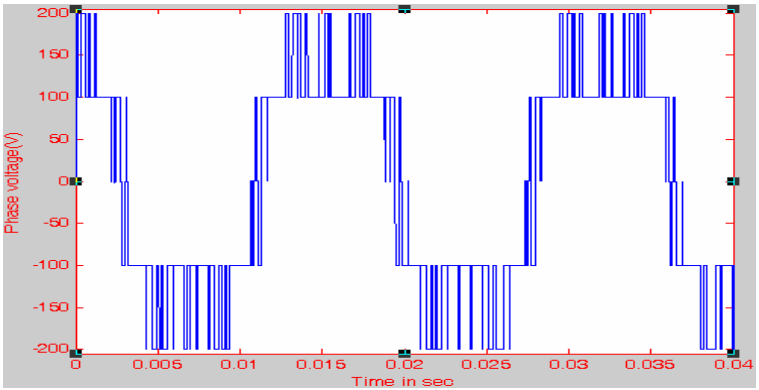

Fig.12. Output Phase Voltage of seven Level Inverter for mi=0.4

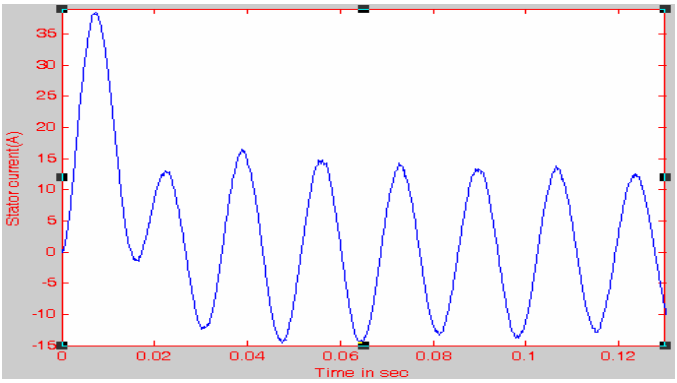

Fig.13. Output line current to IM of seven Level Inverter for mi=0.4

VI. CONCLUSIONS

A simple and general space vector PWM algorithm has been proposed in this paper. The power circuit is designed to have modular structure. All the H-Bridge units are identical. So replacing the faulty units will be easy and quick. The proposed algorithm substantially simplifies the calculation of space vectors and their corresponding dwell times. Based on the proposed algorithm, the generation of automatic switching pattern for the cascaded H-Bridge multilevel inverters has been developed. This algorithm features easy implementation and more importantly, minimum harmonic content in the inverter output voltage and current of the Induction Motor Load. The most important aspect of the proposed algorithm lies in its generality. This can be used in any high-level cascaded H-bridge inverters. This algorithm is verified through MATLAB/SIMULINK simulations.

INDEX:

Type of Load: IM
Rating of Load: 5 HP, 460 V, 60 Hz, 1750 rpm
Stator Resistance and Inductance: 0.01965 p.u and 0.0397 p.u.
Rotor Resistance and Inductance: 0.01909 p.u and 0.0397 p.u.
Mutual Inductance: 1.359 p.u.
Sampling time Ts=2e-6 sec
Switching frequency Fc=1980 Hz.

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