ANALYSIS OF NEW H-BRIDGE BASED CASCADED MULTILEVEL INVERTER

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***Abstract*—This paper deals with the design and analysis of new h-bridge based single and three phase cascaded multilevel inverter. It has two types of sources: symmetric and asymmetric source. In this topology asymmetric source is preferred because it provides large number of output voltage level with minimum number of switches. This new H-bridge based cascaded multilevel inverter is able to increase output voltage levels with reduced number of power electronic device drive circuits, and DC voltage sources. In this paper generated 31 level output voltage and the main objective is to reduce harmonics with multilevel voltage without increasing number of switches this cascaded multilevel inverter is simulated using MATLAB /SIMULINK for single phase and three phase circuits.**

***Index term*: H-bridge cascaded multilevel inverter, asymmetric source, Harmonics.**

I. INTRODUCTION

In general the cascaded multilevel inverter consist of series h-bridge unit in each of its three phase .Each bridge consist of its own dc source. The cascaded multilevel inverter has two types of source such as symmetric and asymmetric dc source. The symmetric source is equal dc voltage applied to an inverter and the asymmetric source has unequal dc source. The cascaded multilevel inverter is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches, power diodes, driver circuits, and dc voltage sources that lead to reduction in installation space and cost of the inverter. The main aim of this paper is to reduce harmonics with multilevel output voltages without increasing number of switches.

This topology is to increase number output voltage and also to reduce harmonic with reduces no of the switches. The advantage of the cascaded multilevel inverter is reduces lower order harmonic, high power quality, better electromagnetic consistence. Lower dv/dt, lower switching losses. The new H-bridge based cascaded multilevel inverters are also classified into two types such that are symmetric and asymmetric. In this paper cascaded multilevel inverter are used as asymmetric dc source and power electronic devices such as (IGBT, MOSFET), power diodes and drive circuit are used for generating the specific output voltage. The bidirectional power switches have been used in earlier topologies. Each bidirectional power switch includes two IGBTs, two power diodes, and one driver circuit if the common emitter configuration is used. Therefore, in these topologies, the installation space and total cost of the inverter increase. As a result, several asymmetric cascaded multilevel inverters have been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them.

Each unidirectional switch consists of an IGBT with an antiparallel diode. Two of these topologies have been presented in [1] and [6]. Two other algorithms for the H-bridge cascaded multilevel inverter have been also presented in [3] and [8].the symmetric also consist of equal dc source there the level of generating voltage is low this is major disadvantage of this source. Therefore asymmetric dc source are used.

The application of this inverter is mainly used in industries and in used in facts devices to the power quality of the power the power system. While these inverters are used there is no need of transformer and filters. Therefore installation cost and harmonic are reduced.

II. PROPOSED CASCADED MULITLEVEL INVERTER

The basic unit of proposed cascaded multilevel is shown in figure 1.

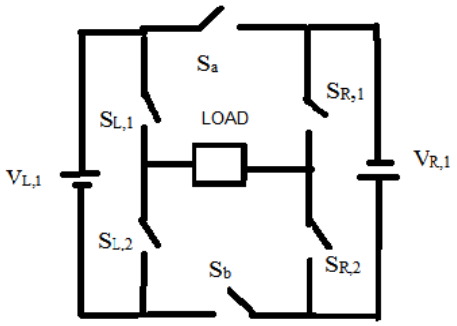

Fig 1.shows the basic unit of cascaded multilevel inverter.

The circuit consists of six unidirectional power switches ($S_{L,1}$,$S_{L,2}$,$S_{R,1}$ $S_{R,2}$,S_a, and S_b) and two insulated dc voltage

sources ($V_{L,1}$, $V_{R,1}$) .The voltage source in the basic unit are asymmetric dc sources.

This basic unit is able to generate seven levels, (i.e.) three positive levels, three negative levels, and one zero level at the output . In addition, in each switching pattern, one power switches from each leg ($S_{L,1}$,or $S_{L,2}$),($S_{R,1}$or$S_{R,2}$) and either Sa or S_b are turned on simultaneously.

Table 1

The switching patteren for this basic circuit unit is shown in table 1

STATE	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_A	S_B	V_O
1	1	0	0	1	0	1	$V_{L,1}$
2	0	1	1	0	0	1	$V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0
5	0	1	1	0	1	0	$-V_{L,1}$
6	1	0	0	1	1	0	$-V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}+V_{R,1})$

If the magnitudes of the dc voltage source are unequally considered, the proposed basic unit can generate seven levels at the output:

$V_{R,1}=V_{dc}$ .....(1)

$V_{L,1}=2V_{dc}$ .....(2)

No of levels (m) =7,

$Vo_1 (t) = V_{R,1+} V_{L,1}$ .....(3)

In order to generate more number of the output levels at the output, the basic units are connected in series.

Fig 2 shows the two new H- bridges are connected in series. In this series connected H-bridges, the units are triggered according to switching pattern.

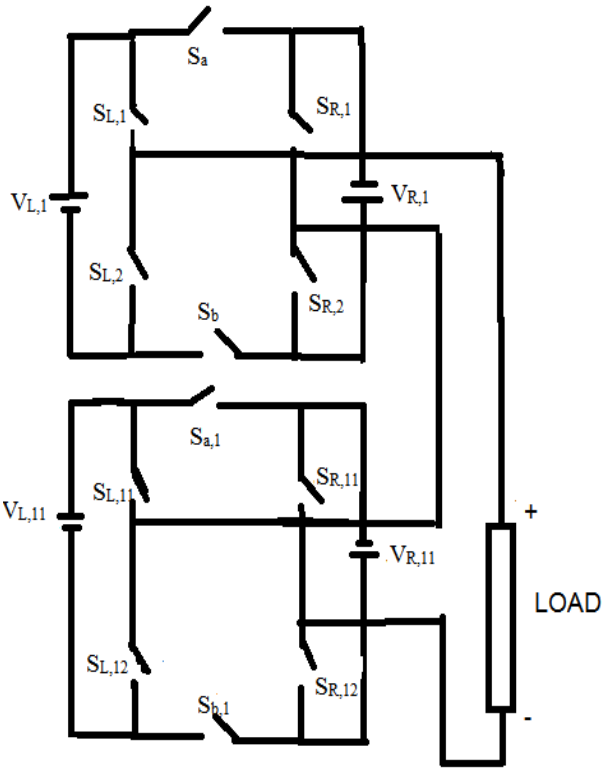

Fig 2.shows cascaded multilevel inverter with two bridge in series.

The magnitude of the dc voltage source of this cascaded multilevel inverter, No of output voltage level, Maximum output voltage are using the formula

The individual unit voltage sources are

$V_{R,j}= V_{dc}$

$V_{L,j}=2V_{dc}$

For j=1, 2,3……n

Therefore,

$V_{L,1}=V_{dc}$, ...(6)

$V_{R,1}=2V_{dc}$. .....(7)

$V_{L,2}=V_{dc}$, ...(8)

$V_{R,2}=2V_{dc}$. .....(9)

$V_{o,2}(t)= V_{L,1+} V_{R,1+} V_{L,2} + V_{R,2}$

$V_O (t) =V_{o,1}(t)+V_{o,2}(t)$ .....(10)

No of level (m) =13,

This new cascaded multilevel inverter is extended to m levels by connecting n number of h-bridge basic unit in series. Then cascaded multilevel inverter connect the n-number series h-bridge unit according to their design of the level of the inverter.

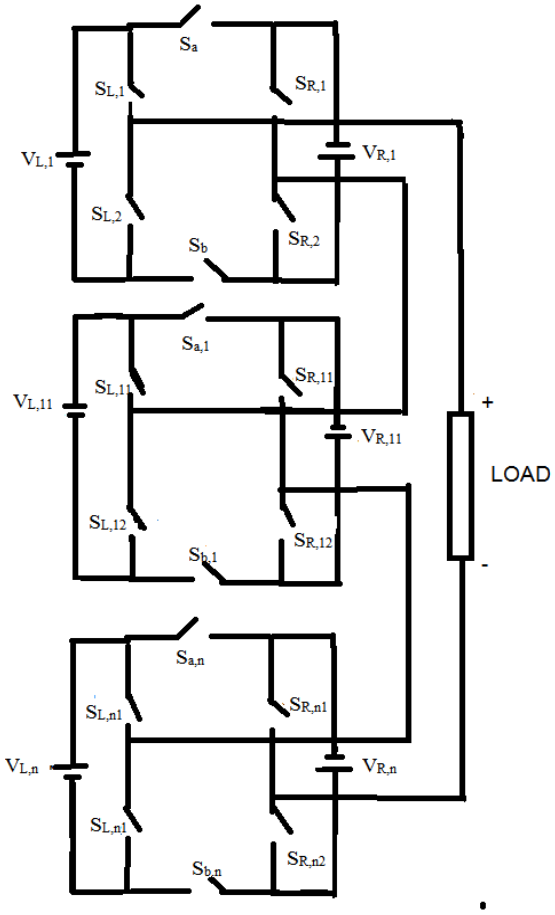

Fig 3 shows n-level output of Proposed cascaded multilevel inverter

$$V_{L,1}=V_{dc} \quad , \ldots\ldots\ldots\ldots(12)$$
$$V_{R,1}=2V_{dc}. \quad ,\ldots\ldots\ldots\ldots(13)$$
$$V_{L,n}=nV_{dc}, \quad \ldots\ldots\ldots\ldots(14)$$
$$V_{R,n}=nV_{dc} \quad \ldots\ldots\ldots\ldots(15)$$
$$V_{o,n}(t)= V_{L,1+} V_{R,1+} V_{L,2} + V_{R,2+}\ldots\ldots\ldots V_{L,n} +V_{R,n} \quad \ldots.(16)$$

The output voltage of the proposed cascaded multilevel inverter is equal to adding the output level of different units is given by

$V_O(t)=V_{o,1}(t)+V_{o,2}(t)+\ldots\ldots\ldots\ldots..+V_{o,n}(t)$ …....(17)

While adding output voltage of the inverter then the level of the inverter is increased.

The number of the switches (Nswitch), drive circuits (N driver), and dc voltage are calculated as follows

$N_{switches}=N_{drives}=6n$ ……..(18)

$N_{source}=2n.$

The total cost of the proposed inverter is estimated with the help of these parameters.

III THREE PHASE CASCADED MULTILEVEL INVERTER

The proposed cascaded multilevel inverter is extended for three phase application .the circuit diagram shown in figure 4

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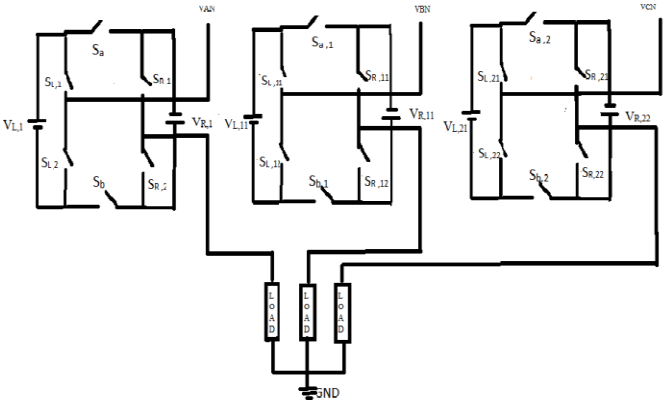

Fig 4 shows new h-bridge three phase cascaded multilevel inverter

The advantage of three phase cascaded multilevel inverter are reduce the THD .it is reduces the THD better then single phase and other conventional cascaded multilevel inverter.

IV PWM MODULATION STRATEGIES

Sinusoidal Pulse Width Modulation uses the conventional sinusoidal as reference signal and an triangular as carrier signal that helps to maximize the output voltage for a given modulation index.

For an ‗m'level inverter, (m-1) carrier waves are required. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal.

Amplitude modulation index

In amplitude modulation index, modulation index depends on the amplitude of carrier signal and the reference signal used. In general the value of modulation index varies between 0 and 1. Amplitude modulation index (ma) can be defined as

$$ma = Ar/(m-1)Ac$$

where, Ar -Amplitude of reference signal

Ac -Amplitude of carrier signal

Frequency modulation index

In frequency modulation index, the modulation index depends on the frequency of the reference signal and the carrier signal used.

The frequency modulation index of the mf of the multilevel inverter can be defined as

$$mf = fc/fr$$

Where,

fc- frequency of carrier signal

fr- frequency of reference signal

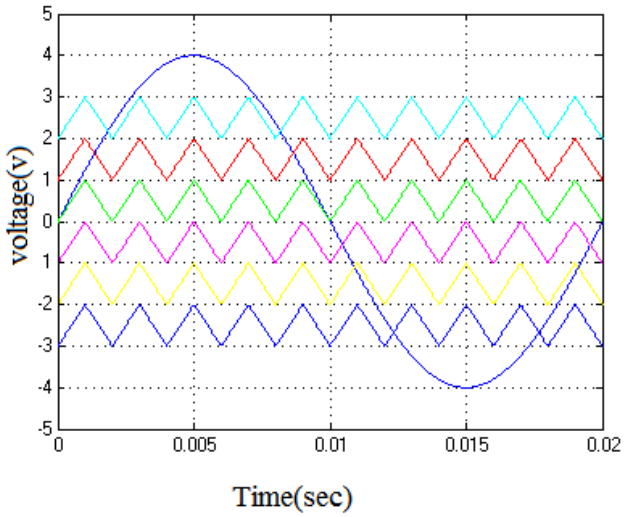

Fig 5 shows Reference and carrier signals for 7 level inverter

IV SIMULATION AND RESULT

Simulink is a block diagram environment for multidomain simulation and Model-Based Design. It supports simulation, automatic code generation, and continuous test and verification of embedded systems. Simulink provides a graphical editor, customizable block libraries, and solvers for modeling and simulating dynamic systems.

Simulation of Single phase inverter circuit

The basic unit is simulated in matlab and the 7 level output is shown in the figure 6

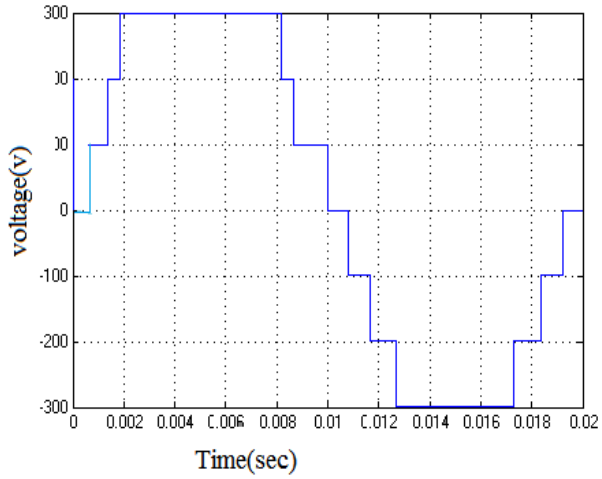

Fig 6 shows 7 level output wave form

FFT analysis

Figure 7 shows harmonic spectrum of basic unit

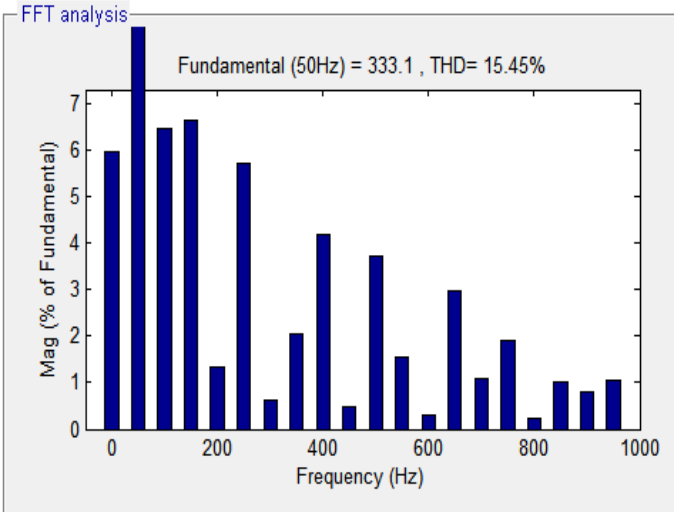

Fig 7 show FFT Analysis for 7 level inverter

The single phase two bridge inverter is simulated. The applied input voltage sources are $V_{dc,1}$=1v, $V_{dc,2}$=2v, $V_{dc,3}$=1v, $V_{dc,4}$=2v. 13 level output waveform as shown in figure 8

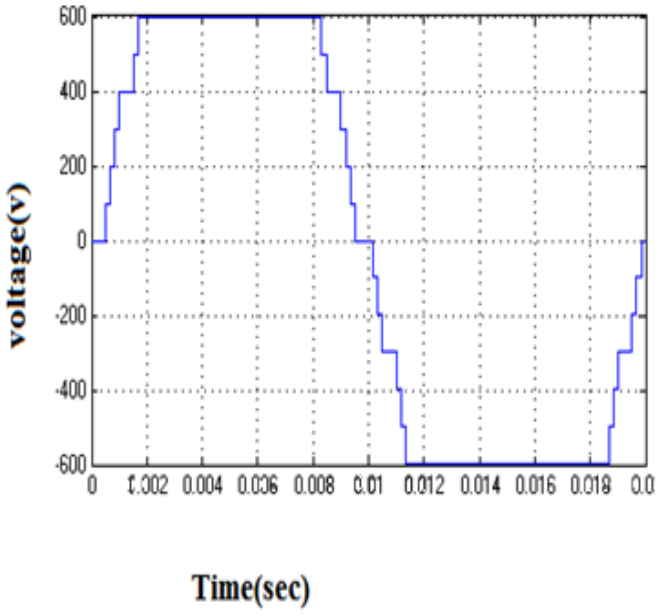

Fig.8shows 13 level output waveform

FFT analysis

The FFT analysis for 13 level output waveform is shown in fig 9

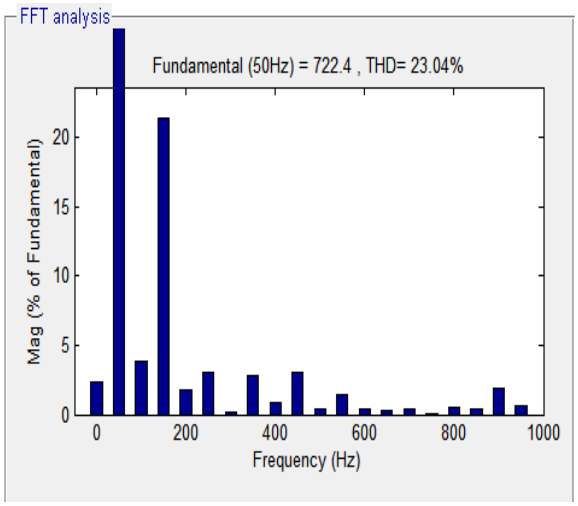

Fig 9 shows FFT analysis for 13 level invert

FFT Analysis

FFT analysis for 19 level inverter is shown in figure 11

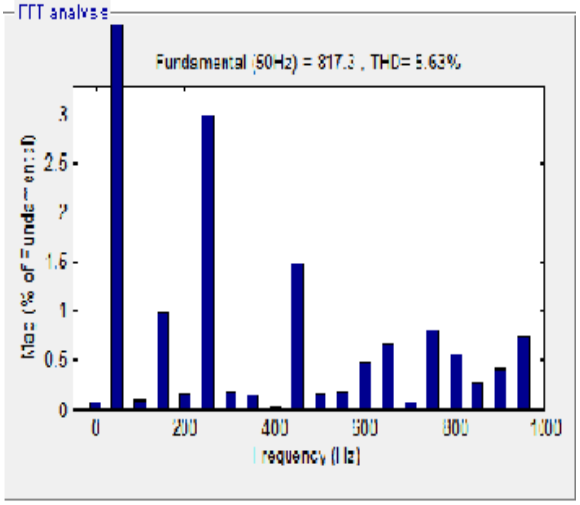

Fig 11 shows FFT analysis for 19 level inverter

19level inverter

Similarly 19 level output waveform is generated using three bridge and six source .The input voltage sources are $V_{dc,1}$=1v,,$V_{dc,2}$=2v,$V_{dc,3}$=1v,$V_{dc,4}$=2v,$V_{dc,5}$=1v,,$V_{dc,6}$=2v. And the 19 level output waveform was shown in figure 10

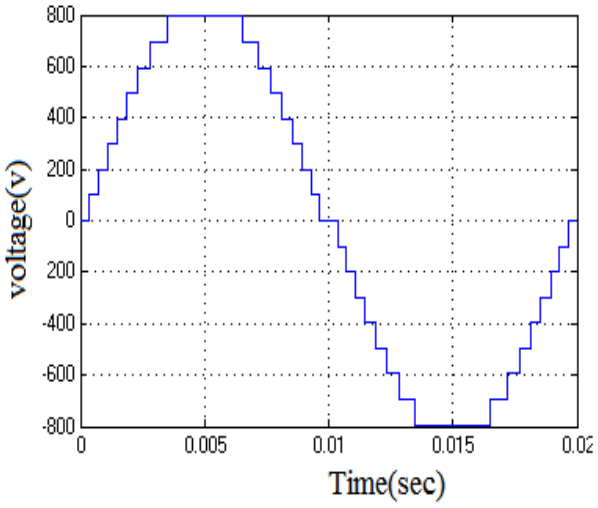

Fig 10 shows 19 level output waveform

19level inverter

Similarly 31 level output waveform is generated using three bridge and six source .The input voltage sources are $V_{dc,1}$=1v,,$V_{dc,2}$=2v,$V_{dc,3}$=2v,$V_{dc,4}$=2v,$V_{dc,5}$=4v,,$V_{dc,6}$=4v. And the 31 level output waveform was shown in figure 12.

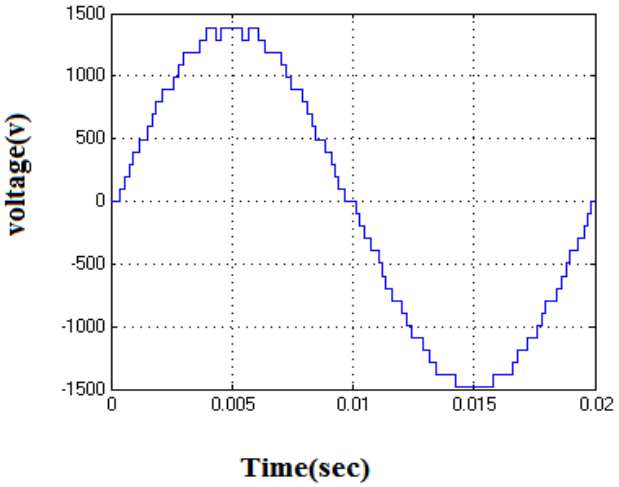

Fig 12 shows 31 level output waveform

FFT Analysis

FFT analysis for 13 level inverter is shown in figure 13

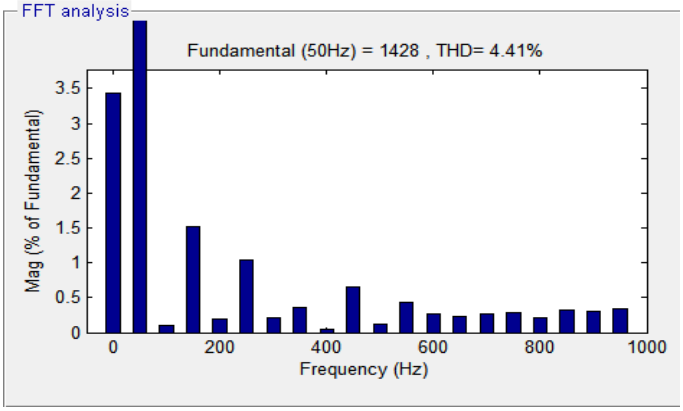

Fig 13 shows FFT analysis for 13 level inverter

Table 2

THD value for single phase obtained level inverter

No of H-bridges	Number of levels (Hz)	No of switches	% THD value
1	7 level	6	15.45
2	13 level	12	23.04
3	19 level	18	5.63

Table 2 shows the THD value of single phase cascaded multilevel inverter.

Form this analysis, when the input voltage increases then the level of the output voltage are increase without increasing switches. Then THD values are also reduces when increasing the level of output voltage

Three phase cascaded multilevel inverter

The three phase inverter is with two bridge are connect in series. The 13 level output waveform in three phase circuit is shown in figure 14.

13level

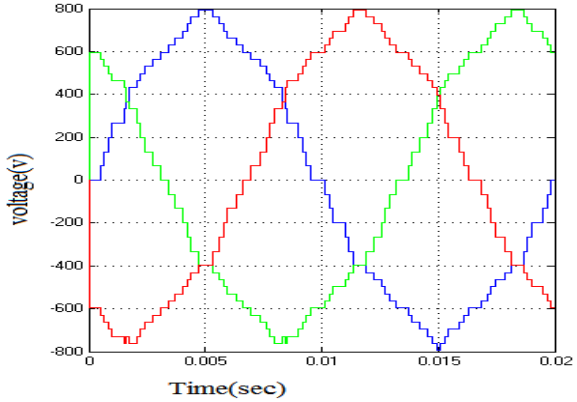

Fig 14 shows 13 level output waveform

FFT Analysis

FFT analysis for 13 level inverter is shown in figure 15

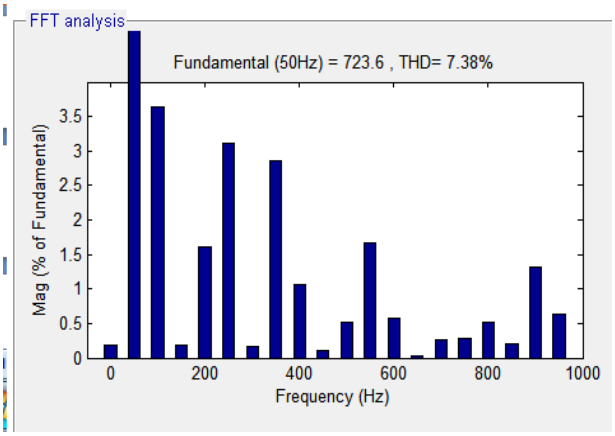

Fig 15 shows FFT analysis for 13 level inverter

The three phase inverter has three bridges and it has six sources.

19 level

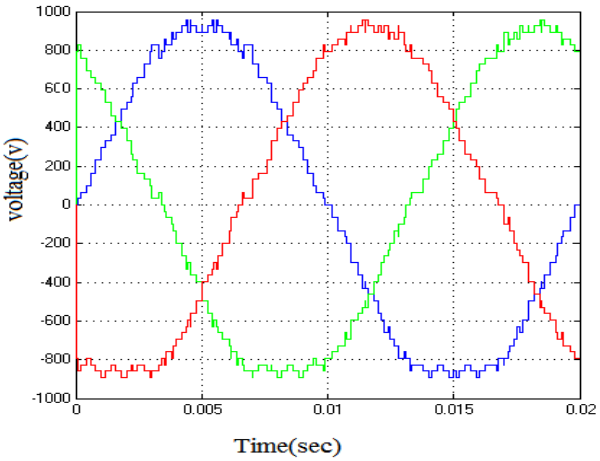

Fig 16 shows19 level output waveform

FFT Analysis

FFT analysis for 19 level inverter has shown in fig 17

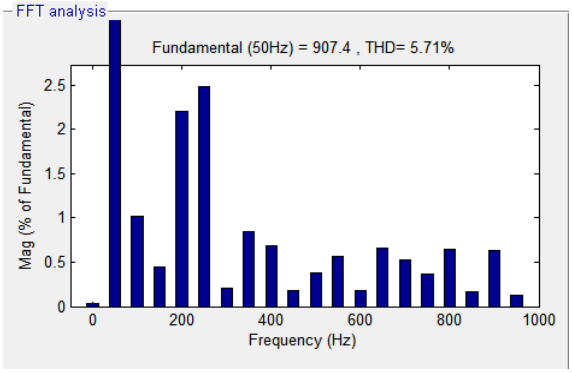

Fig 17 shows FFT analysis for 19 level inverter

31 level

Fig 14 shows 31 level output waveform

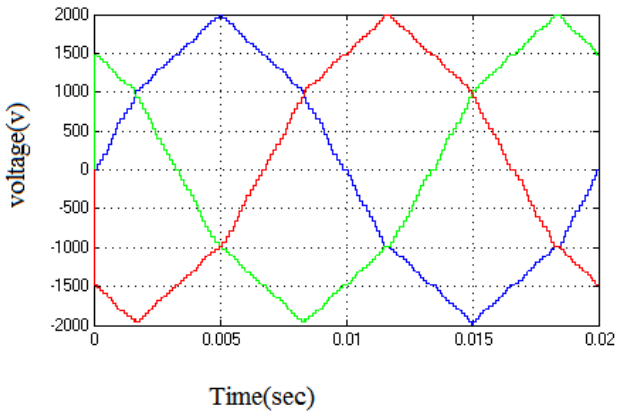

Fig 18 shows 31 level output waveform

FFT Analysis

FFT analysis for 19 level inverter has shown in fig 19

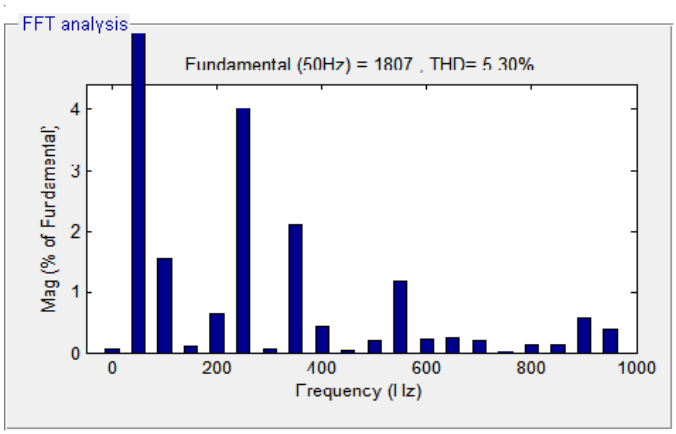

Fig 19shows FFT analysis for 19 level inverter

Table 3

THD value for three phase obtained level inverter

Number of levels(Hz)	%THD value
13 level	7.38
19 level	5.71
31level	5.30

Table 3 shows that THD value of three phase cascaded multilevel inverter.

V Conclusion

Multilevel inverters are very interesting for high voltage application and asymmetric states. The main advantages of multilevel inverter of the cascaded multilevel are improve the output voltage quality, reduces the number of switching devices ,operates in asymmetric states. In this paper cascaded multilevel inverter is designed and simulated for single phase and three phase circuits. The main achievement of this control techniques are the reduction in their total harmonic distortion (THD), closer to sinusoidal waveform without the usage of an output filter. This inverter reduces the switching losses by reducing number of switches and provides improved output voltage capability

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