ESTIMATING POWER LOSSES IN THREE-PHASE TO THREE-PHASE (AC-AC) CONVERTER USING MINIMUM IGBTS

Md. Ziaul Hoque[1], Benu Lal Nath[2]

Research Scholar/Department of EEE, International Islamic University Chittagong, Bangladesh
Email: ziaulieee@yahoo.com[1] anik.com66@yahoo.com[2]

Dr. Md. Delawer Hossain[3]

Professor/Department of EEE, International Islamic University Chittagong, Bangladesh
Email: niniandgork@yahoo.com[3]

Abstract— *Nowadays we have seen various AC-AC converters using IGBTs (Insulated Gate Bipolar Transistor) where various number of IGBTs switches are used. This type of converter is connected grid to the connected load. There are huge amount of losses if a large number of IGBT switches is used. Using reduced-switch-count converters in power electronic systems is necessary for the numerous advantages such as low cost, low weight and volume, and high reliability offered by them. In this thesis paper, we proposed a Three-Phase to Three-Phase (AC-AC) Converter which we used minimum number of switches. Here we use few active switches and few diodes and we can find out the lowest number of active switches among three-phase to three-phase AC/AC converters that offers sinusoidal input and output, unity power factor and more importantly, low manufacturing cost. Due to minimize the voltage ripple of the DC link the analysis of sizing of the DC link capacitors is performed and capacitor sizes are chosen. The analysis and simulations demonstrate the effectiveness of the proposed AC/AC converter.*

Keywords
IGBT Switches, DC Link Capacitors, AC/AC Convertor, Three-Phase Rectifier, Three-Phase Inverter, Grid Voltage Sag.

I. INTRODUCTION

Converter systems with either a voltage or current DC-link are mainly used today. In the case of the voltage DC-link, the mains coupling can be implemented by a diode bridge. Despite the fact that this configuration features low cost and reliable operation due to using diode rectifier, it suffers some disadvantages such as highly distorted input current, low input power factor and lacking the capability of working in regenerative or dynamic braking modes.

To accomplish braking operation of the load, a pulse-controlled braking resistor must be placed in the DC-link or an anti parallel thruster bridge be provided on the mains side.The six-switch three-phase to three-phase AC/AC converter is depicted in Fig. 1. As it can be seen in the figure, it has two legs with three power switches in each one.The proposed structure is comparable to a B4 rectifier as the active front end of a three-phase B4 inverter though a row of switches is shared between them. Two phases of the three-phase AC source and two phases of the three-phase AC load are connected to the two converter legs and the remaining phase of the source and load is connected to the joint of the split capacitor bank. In Fig. 4, the four upper switches work as a B4 rectifier and the four lower switches work as a B4 inverter. Compared to its counterpart in Fig. 2, the proposed structure not only retains all the desirable features, but also reduces the number of required switches by 25% and hence proves more attractive in low voltage and power ratings applications. Two modes of operation are defined for the proposed converter: 1- Variable frequency (VF) mode in which frequency and amplitude of the inverter output and rectifier input voltages can be different and 2- Constant frequency mode (CF) in which frequency of grid and load is similar whereas the amplitudes of the input or output voltages may vary. The amount of DC link capacitors' voltage are dependent on three factors of a, b and c. These coefficients are determined so as to provide balanced three-phase outputs without any DC offset.

$$V_{Cd1} = aV_{DC} \quad (1)$$

$$V_{Cd2} = bV_{DC} \quad (2)$$

$$V_{Cd3} = cV_{DC} \quad (3)$$

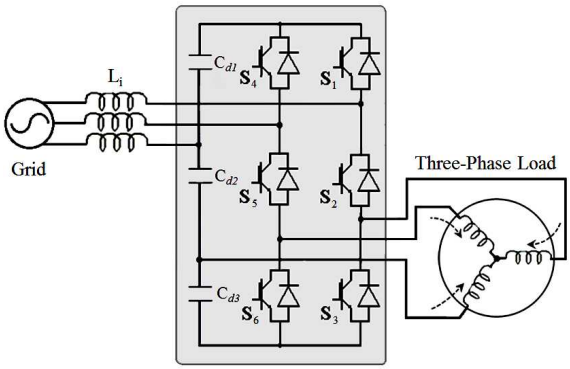


Figure 1: Proposed six-switch AC/AC converter

II. INSULATED GATE BIPOLAR TRANSISTOR (IGBT) BASICS

A. IGBT Fundamental

The Insulated Gate Bipolar Transistor (IGBT) is a minority-carrier device with high input impedance and large bipolar current-carrying capability. Many designers view IGBT as a device with MOS input characteristics and bipolar output characteristic that is a voltage-controlled bipolar device. To make use of the advantages of both Power MOSFET and BJT, the IGBT has been introduced. It's a functional integration of Power MOSFET and BJT devices in monolithic form. It combines the best attributes of both to achieve optimal device characteristics [2].The IGBT is suitable for many applications in power electronics, especially in Pulse Width Modulated (PWM) servo and three-phase drives requiring high dynamic range control and low noise. It also can be used in Uninterruptible Power Supplies (UPS), Switched-Mode Power Supplies (SMPS), and other power circuits requiring high switch repetition rates. IGBT improves dynamic performance and efficiency and reduced the level of audible noise. It is equally suitable in resonant-mode converter circuits. Optimized IGBT is available for both low conduction loss and low switching loss. The main advantages of IGBT over a Power MOSFET and a BJT are:

- It has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density. So smaller chip size is possible and the cost can be reduced.
- Low driving power and a simple drive circuit due to the input MOS gate structure. It can be easily controlled as compared to current controlled devices(thyristor, BJT) in high voltage and high current applications
- Wide SOA. It has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking capabilities

B. Basic Structure

The basic schematic of a typical N-channel IGBT based upon the DMOS processes as shown in figure 2. This is one of several structures possible for this device. It is evident that the silicon cross-section of an IGBT is almost identical to that of a vertical Power MOSFET except for the P+ injecting layer. It shares similar MOS gate structure and P wells with N+ source regions. The N+ layer at the top is the source or emitter and the P+ layer at the bottom is the drain or collector. It is also feasible to make P-channel IGBTs and for which the doping profile in each layer will be reversed. IGBT has a parasitic thyristor comprising the four-layer NPNP structure. Turn-on of this thyristor is undesirable.

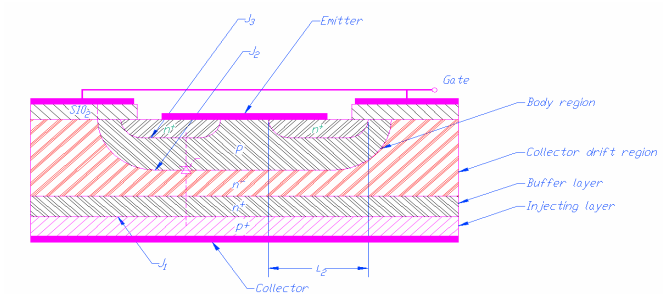


Figure 2: Schematic view of a generic N-channel IGBT [2]

Some IGBTs, manufactured without the N+ buffer layer, are called non-punch through (NPT) IGBTs whereas those with this layer are called punch-through (PT) IGBTs. The presence of this buffer layer can significantly improve the performance of the device if the doping level and thickness of this layer are chosen appropriately. Despite physical similarities, the operation of an IGBT is closer to that of a power BJT than a power MOSFET. It is due to the P+ drain layer (injecting layer) which is responsible for the minority carrier injection into the N--drift region and the resulting conductivity modulation.

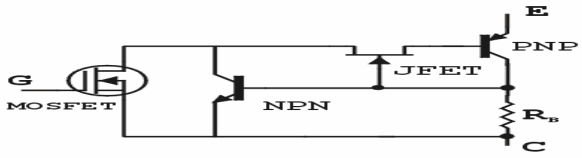


Figure 3: Equivalent circuit model of an IGBT [2]

Based on the structure, a simple equivalent circuit model of an IGBT can be drawn as shown in Figure 3. It contains MOSFET, JFET, NPN and PNP transistors. The collector of the PNP is connected to the base of the NPN and the collector of the NPN is connected to the base of the PNP through the JFET. The NPN and PNP transistors represent the parasitic thyristor which constitutes a regenerative feedback loop. The resistor RB represents the shorting of the base-emitter of the NPN transistor to ensure that the thyristor does not latch up, which will lead to the IGBT latch up. The JFET represents the constriction of current between any two neighboring IGBT cells. It supports most of the voltage and allows the MOSFET to be a low voltage type and consequently have a low RDS (on) value. A circuit symbol for the IGBT is shown in Figure 4. It has three terminal scaled Collector (C), Gate (G) and Emitter (E).

Figure 4: IGBT Circuit Symbol

IGBTs, which have equal forward and reverse breakdown voltage, are suitable for applications. The PT IGBTs, which have less reverse breakdown voltage than the forward breakdown Voltage, applicable for DC circuits where devices are not required to support voltage in the reverse direction.

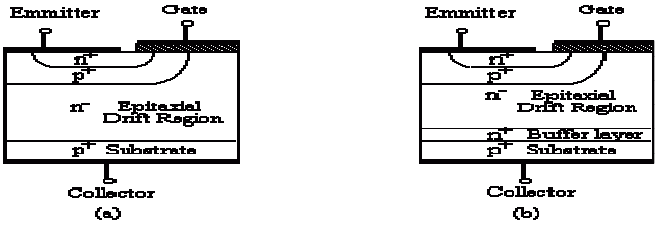


Figure 5: Structure (a) NPT-IGBT and (b) PT-IGBT [2]

Table 1: Characteristic comparison NPT and PT IGBT

	NPT	PT
Switching Loss	Medium Long, low amplitude tail current. Moderate increase in Eoff with temperature	Low Short tail current Significant increase in Eoff with temperature
Conduction loss	Medium Increases with temperature	Low Flat to slight decrease with Temperature
Paralleling	Easy Optional sorting Recommend share heat	Difficult Must sort on VCE(on)
Short circuit rated	Yes	Limited High gain

C. Transfer Characteristics

The transfer characteristic is defined as the variation of ICE with VGE values at different temperatures, namely, 25oC, 125oC, and -40oC. A typical transfer characteristic is shown in Figure 6. The gradient of transfer characteristic at a given temperature is a measure of the trans conductance (gfs) of the device at that temperature.

$$g_{fs} = \frac{\partial Ic}{\partial V_{GE}} \Big| V_{CE} = \text{Constant}$$

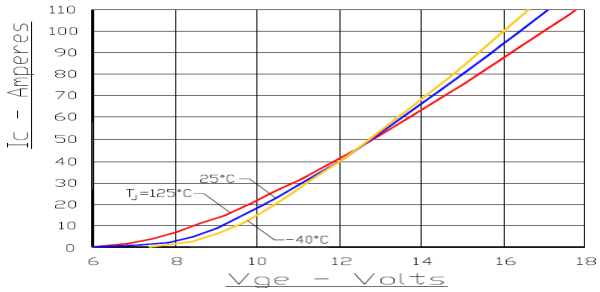


Figure 6: IGBT Transfer Characteristics

A large gfs is desirable to obtain a high current handling capability with low gate drive voltage. The channel and gate structures dictate the gfs value. Both gfs and RDS(on) (on resistance of IGBT) are controlled by the channel length which is determined by the difference in diffusion depths of the P base and N+ emitter. The point of intersection of the tangent transfer characteristic determines the threshold voltage (VGE(th)) of the device.

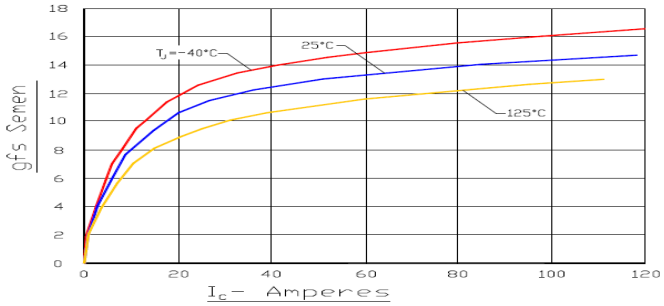


Figure 7: Tran's conductance Characteristics of an IGBT

D. Switching Characteristics

The switching characteristics of an IGBT are very much similar to that of a Power MOSFET. The major difference from Power MOSFET is that it has a tailing collector current due to the stored charge in the N--drift region. The tail current increases the turnoff loss and requires an increase in the dead time between the conduction of two devices in a half-bridge circuit. The Figure 8 shows a test circuit for switching characteristics and the Figure 7 shows the corresponding current and voltage turn-on and turn-off waveforms. IXYS IGBTs are tested with a gate voltage switched from +15V to 0V. To reduce switching losses, it is recommended to switch off the gate with a negative voltage (-15V).

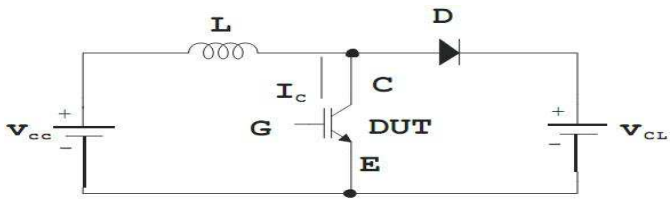


Figure 8: IGBT Switching Time Test Circuit

The turn-off speed of an IGBT is limited by the lifetime of the stored charge or minority carriers in the N--drift region which is the base of the parasitic PNP transistor. The base is not accessible

physically thus the external means cannot be applied to sweep out the stored charge from the N-drift region to improve the switching time. The only way the stored charge can be removed is by recombination within the IGBT. Traditional lifetime killing techniques or an N+ buffer layer to collect the minority charges at turn-off are commonly used to speed-up recombination time.

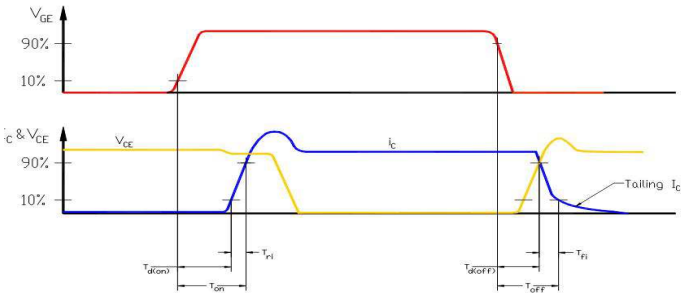


Figure 9: IGBT Current and Voltage Turn-off Waveforms.

The turn-on energy Eon is defined as the integral of IC .VCE within the limit of 10% I Cerise to 90% VCE fall. The amount of turn on energy depends on the reverse recovery behavior of the freewheeling diode, so special attention must be paid if there is a freewheeling diode within the package of the IGBT (Co-Pack).The turn-off energy Eoff is defined as the integral of IC .VCE within the limit of 10% VCE rise to 90% IC fall. Eoff plays the major part of total switching losses in IGBT.

E. Latch-up

During on-state, paths for current flow in an IGBT are shown in Figure 10. The holes are injected into the N--drift region from the P+ collector form two paths. Part of the holes disappear by recombination with electrons came from MOSFET channel. Other part of holes are attracted to the vicinity of the inversion layer by the negative charge of electrons, travel laterally through the P-body layer and develops a voltage drop in the ohmic resistance of the body. This voltage tends to forward bias the N+P junction and if it's large

enough, substantial injection of electrons from the emitter into the body region will occur and the parasiric NPN transistor will be turned-on. If this happens, both NPN and PNP parasitic transistors will be turned-on and hence the thyristor composed of these two transistors will latch on and the latch up condition of IGBT will have occurred. Once in latch up, the gate has no control on the collector current and the only way to turn-off the

IGBT is by forced commutation of the current, exactly the conventional thyristor.

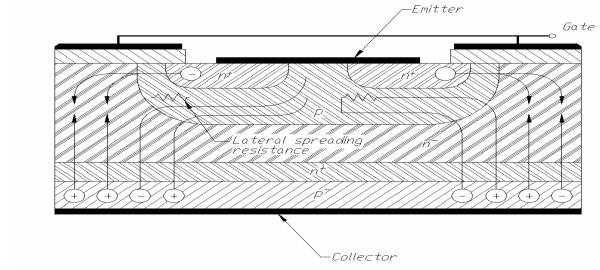


Figure 10: ON-state current flow path of an IGBT

If latch up is not terminated quickly, the IGBT will be destroyed by the excessive power dissipation. IGBT has a maximum allowable peak drain current (ICM) that can flow without latch up. Device manufacturers specify this current level in the datasheet. Beyond this current level, a large enough lateral voltage drop will activate thyristor and the latch up of IGBT.

F. Safe Operating Area (SOA)

The safe operating area (SOA) is defined as the current-voltage boundary within which a power switching device can be operated without destructive failure. For IGBT, the area is defined by the maximum collector-emitter voltage VCE and collector current IC within which the IGBT operation must be confined to protect it from damage. The IGBT has the following types of SOA operations: forward-biased safe operating area (FBSOA), reverse-biased safe operating area (RBSOA) and short-circuit safe operating area (SCSOA).

III. CARRIER-BASED PWM SCHEME FOR THE AC/AC CONVERTER

The carrier based pulse-width modulation scheme of the proposed converter can be seen in Fig. 11. In each leg, there are two modulating waveforms, one for the rectifier side (Vxr) and one for the inverter side (Vxi), (x=A, B). The key point in the modulation of the proposed converter is that the interference ofthe rectifier and inverter reference waveforms should be avoided, i.e. Vxr > Vxi. This is achieved by adding two offset signals to the reference signals of both sides and limiting their modulation indices to prevent over-modulation [17]. Calculating the suitable offset values and adding them to the inverter and rectifier side reference waveforms, the two modulating waveforms of each leg are obtained. The modulating waveforms are then compared with a common triangular carrier signal. Gate signals of the upper switches (S1and S4) are resulted from comparing the rectifier modulating signal with the carrier signal. Gate signals of the lower switches S3 and S6) are the logical NOT of the values obtained by comparing the inverter modulating signals with the carrier signal. Gate signals of the middle switches (S2 and S5) are generated by logical XOR of the upper and lower gate signals in each leg. Applying this scheme, there are always two ON switches in each leg. The converter acceptable switching states and the resultant output and input phase voltages of the proposed converter are shown in Table I. Since the two phases of the three-
phase AC source and the two phases of the three-phase load are connected to the converter legs and the third remaining phase of them is connected to the joint of the split capacitor bank, the voltage references of rectifier and inverter should be chosen so as to achieve three-phase balanced voltage at the input and output terminals of the converter. Assume that the three-phase voltages of source are given in a balanced set as

$$v_{As} = Vm \sin\omega_r t \quad (1)$$

$$v_{Bs} = Vm \sin(\omega_r t - 2\pi/3) \quad (2)$$

$$v_{Cs} = Vm \sin(\omega_r t + 2\pi/3) \quad (3)$$

where V_m and ω_r are respectively the source voltage amplitude and its angular frequency. The final modulating waveforms of rectifier should be (1) and (2) to achieve three-phase balanced voltage at the input of rectifier.

$$v^*Ar = m_r \sin(\omega_r t + \delta_r) + offset_r \quad (4)$$

$$v^*Br = m_r \sin(\omega_r t + \delta_r - \varphi_r) + offset_r \quad (5)$$

where m_r and $offset_r$ are respectively the rectifier reference amplitude and its offset value, δ_r is the phase difference between the voltage references of rectifier and three-phase voltages of source and φ_r is the phase difference between voltage reference of the rectifier.

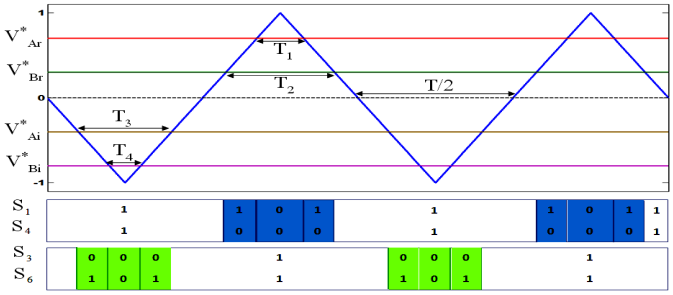


Figure 11: Carrier-based PWM modulation scheme of the proposed converter

Considering the similarity of the triangles in Fig.14, the switching time can be calculated as:

$$T_1 = T_s/2\,(1 - V^*_{Ar}) \quad (6)$$

$$T_2 = T_s/2\,(1 - V^*_{Br}) \quad (7)$$

Using Table 2, the average of the input phase voltage V_{Ar} over one switching period is calculated

as:

$$V_{Ar} = \{(T_s - T_2)(aV_{DC}/3) + (T_2 - T_1)(2a+b+c)(V_{DC}/3) - T_1(b+c)(V_{DC}/3)\}/T_s \quad (8)$$

$$= V_{DC}\,[V^*_{Ar}(a/3 + b/3 + c/3) - V^*_{Br}(a/6 + b/6 + c/6) + a/6 - b/6 - c/6]$$

Following the same method for the other two phase voltages (V_{Br} and V_{Cr}) and replacing v^*_{Ar} and v^*_{Br} with their equivalents from (4) and (5), yield the fundamental values of the rectifier input phase voltages (9-11).

$$V_{Ar} = V_{dc}\,[(a/3 + b/3 + c/3)\, m_r \sin(\omega_r t + \delta_r) - (a/6 + b/6 + c/6)\, m_r \sin(\omega_r t + \delta_r - \varphi_r) + a/6 - b/6 - c/6 + (a/6 + b/6 + c/6)\, offset_r] \quad (9)$$

$$V_{Br} = V_{dc}\,[-(a/6 + b/6 + c/6)\, m_r \sin(\omega_r t + \delta_r) + (a/3 + b/3 + c/3)\, m_r \sin(\omega_r t + \delta_r - \varphi_r) + a/6 - b/6 - c/6 + (a/6 + b/6 + c/6)\, offset_r] \quad (10)$$

$$V_{Cr} = V_{dc}\,[-(a/6 + b/6 + c/6)\, m_r \sin(\omega_r t + \delta_r) - (a/3 + b/3 + c/3)\, m_r \sin(\omega_r t + \delta_r - \varphi_r) - a/6 - b/6 - c/6 - (a/6 + b/6 + c/6)\, offset_r] \quad (11)$$

Considering the above equations, in order to produce balanced voltages, there should be $\varphi_r = \pi/3$. Moreover, a, b and c coefficients are determined so as to remove DC offset of the input voltages of rectifier. For instant if $offset_r$=0.5, then a =1/4 ,b =1/2 and c =1/4. Fig. 12 illustrates the DC link voltage coefficient values versus rectifier offset variation.

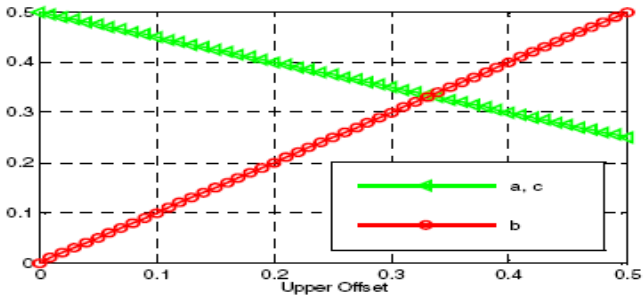


Figure 12: Dc link voltage coefficients versus rectifier offset, first strategy

Assuming the DC component being eliminated, rectifier input voltages would be:

$$v_{Ar} = \sqrt{3/6}\, m_r\, V_{dc} \sin(\omega_r t + \delta_r + \pi/6) \quad (12)$$

$$v_{Br} = \sqrt{3/6}\, m_r\, V_{dc} \sin(\omega_r t + \delta_r - \pi/2) \quad (13)$$

$$v_{Cr} = \sqrt{3/6}\, m_r\, V_{dc} \sin(\omega_r t + \delta_r + 5\pi/6) \quad (14)$$

For the inverter side of the proposed converter, again using the similarity of triangles in Fig. 13 and assuming the voltage references to be as (15) and (16), switching times are obtained as (17) and (18).

$$V^*_{Ai} = m_i \sin(\omega_i t) + offset_i \quad (15)$$

$$V^*_{Br} = m_i \sin(\omega_i t + \varphi_i) + offset_i \quad (16)$$

$$T_3 = T_s/2\,(1 + V^*_{Ai}) \quad (17)$$

$$T_4 = T_s/2\,(1 + V^*_{Bi}) \quad (18)$$

With applying the above method to the inverter side of proposed converter and assuming φ_r be equal to $\pi/3$ and the DC component being eliminated, the fundamental values of the inverter output phase voltages would be:

$$v_{Ai} = \sqrt{3/6}\, m_i\, V_{dc} \sin(\omega_i t + \pi/6) \quad (19)$$

$$v_{Bi} = \sqrt{3/6}\, m_i\, V_{dc} \sin(\omega_i t - \pi/2) \quad (20)$$

$$v_{Ci} = \sqrt{3/6}\, m_i\, V_{dc} \sin(\omega_i t + 5\pi/6) \quad (21)$$

IV. OPERATION MODES OF THE AC/AC CONVERTER

Two modes of operation are defined for the proposed converter. Each mode employs two different strategies for eliminating DC component from output voltage; the first strategy results in constant DC link voltages and the second makes them vary according to rectifier and inverter modulation indices. These

modes and their particular strategies are described in the following and pros and cons of each one are discussed.

A. Mode of operation

Input and outputs of the proposed converter can have different frequencies and amplitude in this mode independent from each other. To eliminate DC component and to obtain balanced input and output, two strategies are suggested:

A.First strategy

To prevent rectifier and inverter modulating waves interference and also to avoid over-modulation, rectifier and inverter offsets should always fulfill the following criteria

$$0 \leq offset_r \leq 1 \quad (22)$$

$$1 \leq offset_i \leq 0 \quad (23)$$

$$offset_r = offset_i \quad (24)$$

Furthermore, considering (8) to (11) and (24), to eliminate DC component from input and output of the converter without using extra capacitors, DC link voltage coefficients are determined by (25) to (27).

$$a = (1 - offsetr) / 2 \quad (25)$$

$$b = offset_r \quad (26)$$

$$c = (1 - offset_r) / 2 \quad (27)$$

This figure illustrates the DC link voltage coefficient values versus offset variation in the first strategy

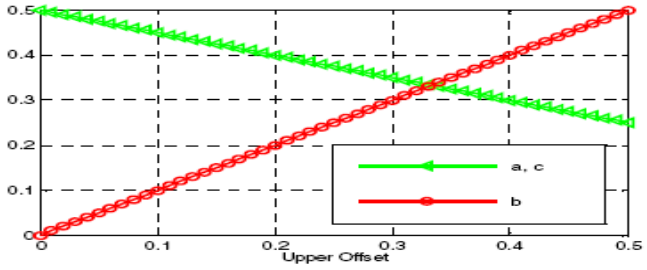


Figure13: Dc link voltage coefficients versus rectifier offset, first strategy

Second strategy

This strategy is in fact a method for enhancing DC bus utilization by increasing the maximum limit of modulation index. For this purpose, $offset_r$ and $offset_i$ are determined according to rectifier (28).This factor specifies the rectifier utilization of DC link voltage.

$$\alpha = \frac{mr}{mr + mi} \quad (28)$$

Limits of $offset_r$, $offset_i$, *mr* and *mi* and also DC link voltage coefficients are tabulated in Table 2 or both strategies.

	First strategy	Second strategy
Dc link voltage coefficients	$a = (1 - offset_i)/2$ $b = offset_r$ $c = (1 - offset_i)/2$	$a = -offset_i/2$ $b = 1/2$ $c = offset_r/2$
Rectifier and inverter offset limits	$0 \leq offset_r \leq 1$ $-1 \leq offset_i \leq 0$ $offset_r = -offset_i$	$offset_r + offset_i \leq 1$ $offset_r = 1 - \alpha$ $offset_i = -\alpha$
Modulation indices limits	$m_r + m_i \leq \lvert offset_r \rvert + \lvert offset_i \rvert$ $m_r \leq 1 - \lvert offset_r \rvert$ $m_i \leq 1 - \lvert offset_i \rvert$	$m_r + m_i \leq 1$ $m_r \leq 1$ $m_i \leq 1$

Table 3. Operation Details Using Two Strategies of DC Component lamination VF Mode

B.CF mode of operation

In CF mode, the voltage amplitudes of input and output of the proposed six-switch converter can change independently though they must have similar frequency and phase difference. Again, to eliminate DC component from input and output voltages, two strategies are employed. Operation details of these strategies in CF mode are tabulated in Table 4.Using the first strategy in CF mode, variation of *a*, *b* and *c* coefficients versus offset value are depicted in Fig. 13.

	First strategy	Second strategy
Dc link voltage coefficients	$a = (1 - offset_i)/2$ $b = offset_r$ $c = (1 - offset_i)/2$	$a = (1 - offset_r)/2$ $b = 1 + (offset_r - offset_i)/2$ $c = (offset_i - 1)/2$
Rectifier and inverter offset limits	$0 \leq offset_r \leq 1$ $-1 \leq offset_i \leq 0$ $offset_r = -offset_i$	$offset_r = 1 - m_r$ $offset_i = m_i - 1$
Modulation indices limits	$\lvert m_r - m_i \rvert \leq \lvert offset_r \rvert + \lvert offset_i \rvert$ $m_r \leq 1 - \lvert offset_r \rvert$ $m_i \leq 1 - \lvert offset_i \rvert$	$m_r \leq 1$ $m_i \leq 1$

Table 4 : Operation Details Using Two Strategies of DC Component Elimination, CF Mode

C. Sizing of the DC-Link Capacitors

In this paper, a method for minimizing the DC-link voltage ripple of the proposed converter is presented. Using this method, the size of DC-link capacitors are determined so as to minimize DC-link voltage ripple. It is possible to calculate the three capacitor-currents as a function of input and output current of the converter.

$$i_{C1} = d_{11} i_{As} + d_{12} i_{Ao} + d_{44} i_{Bs} + d_{45} i_{Bo} \quad . \quad (29)$$

$$i_{C2} = i_{C1} + i_{Cs} \quad (30)$$

$$i_{C3} = i_{C2} + i_{Co} \quad (31)$$

Where,

ixs (x=A,B,C) =input currents of the converter

ixo (x=A,B,C) =output currents of the converter

dij (*i*,*j*=1,2,…,6 and *i*≠*j*)=duty cycle for switch S*i* and switch S*j*

dii(*i*=1,2,…6) =duty cycle for switch S*i*\

Considering the similarity of the triangles in Fig. 14, the duty cycles in (30) can be expressed as

$$d_{11} = \frac{1}{2}(1 + V^*_{Ar} \quad (32)$$

$$d_{12}=\frac{1}{2}(1+V^*_{Ai}) \quad (33)$$

$$d_{44}=\frac{1}{2}(1+V^*_{Ar}) \quad (34)$$

$$d_{45}=\frac{1}{2}(1+V^*_{Ai} \quad (35)$$

If the grid currents are controlled to be sinusoidal and also in phase with the phase voltages of the grid as

$$i_{As}= Ism \sin \omega_r t \quad (36)$$

$$i_{Bs}= Ism \sin(\omega_r t- 2\pi/ 3) \quad (37)$$

$$i_{Cs}= Ism \sin(\omega_r t- 2\pi/ 3) \quad (38)$$

and the output currents of the converter to be sinusoidal and phase-lagged in relation to output phase voltages of the converter by the angle φ as

$$i_{Ao}=Iom \sin(\omega_{it} - \pi/6-\varphi) \quad (39)$$

$$i_{Bo}=Iom \sin(\omega_{it} - \pi/2 - \varphi) \quad (40)$$

$$i_{Co}=Iom \sin(\omega it - 5\pi/6 - \varphi) \quad (41)$$

Then, the three capacitor-currents can be calculated as (42) to (44)

$$i_{C1} = -1/2\,(1+ offset_r)\, I_{sm}\, \sin(\omega_r t +2\pi/3)+ 1/2\,(1+ offset_i)\, I_{om} \sin(\omega_i t + 5\pi/6 - \varphi) + \sqrt{3}/4\, m_r\, I_{sm} \sin(\delta_r +2\pi/3) - \sqrt{3}/4\, m_i\, I_{om} \cos \Phi \quad (42)$$

$$i_{C2} = -1/2\,(offset_r -1)\, I_{sm}\, \sin(\omega_r t +2\pi/3)+ 1/2\,(1+ offset_i)\, I_{om} \sin(\omega_i t + 5\pi/6 - \varphi) + \sqrt{3}/4\, m_r\, I_{sm} \sin(\delta +2\pi/3) - \sqrt{3}/4\, m_i\, I_{om} \cos \Phi \quad (43)$$

$$i_{C3} = i_{C2} - i_{co} - 1/2(offset_r -1)\, I_{sm}\, \sin(\omega_r t +2\pi/3)+ 1/2\,(offset_i - 1)\, I_{om} \sin(\omega_i t + 5\pi/6 - \varphi) + \sqrt{3}/4\, m_r\, I_{sm} \sin(\delta +2\pi/3) - \sqrt{3}/4\, m_i\, I_{om} \cos \Phi \quad (44)$$

In the case of power balance between the input and output side the following have to be fulfilled

$$\sqrt{3}/4\, m_r\, I_{sm} \sin(\delta +2\pi/3) - \sqrt{3}/4\, m_i\, I_{om} \cos \Phi = 0$$

$$m_r\, I_{sm} \sin(\delta +2\pi/3) = m_i\, I_{om} \cos \Phi \quad (45)$$

Integrating the voltages across the capacitors it is possible to end up with equations for the voltage across C_{d1}, C_{d2} and C_{d3} as

$$V_{Cd1} = (I_{sm}/2C_{d1}\,\omega_r)\,(1+ offset_r)\cos(\omega_r t +2\pi/3) - (I_{om}/2C_{d1}\,\omega_i)\,(1+ offset_i)\cos(\omega_i t + 5\pi/6 - \varphi) + [(\sqrt{3}/4\, C_{d1})\, m_r\, I_{sm} \sin(\delta_r +2\pi/3) - (\sqrt{3}/4C_{d1})\, m_i\, I_{om} \cos \Phi]t + V_{Cd1}(0) \quad (46)$$

$$V_{Cd2} = (I_{sm}/2C_{d2}\,\omega_r)\,(offset_r -1)\cos(\omega_r t +2\pi/3) - (I_{om}/2C_{d2}\,\omega_i)\,(1+ offset_i)\cos(\omega_i t + 5\pi/6 - \varphi) + [(\sqrt{3}/4\, C_{d2})\, m_r\, I_{sm} \sin(\delta_r +2\pi/3) - (\sqrt{3}/4C_{d2})\, m_i\, I_{om} \cos \Phi]t + V_{Cd2}(0) \quad (47)$$

$$V_{Cd2} = (I_{sm}/2C_{d3}\,\omega_r)\,(offset_r -1)\cos(\omega_r t +2\pi/3) - (I_{om}/2C_{d3}\,\omega_i)\,(offset_i -1)\cos(\omega_i t + 5\pi/6 - \varphi) + [(\sqrt{3}/4\, C_{d3})\, m_r\, I_{sm} \sin(\delta_r +2\pi/3) - (\sqrt{3}/4C_{d3})\, m_i\, I_{om} \cos \Phi]t + V_{Cd3}(0) \quad (48)$$

Where $V_{Cd}1(0)$, $V_{Cd2}(0)$, $V_{Cd}3(0)$ = initial voltage across the capacitors

The total DC-link voltage ripple adds up

$$\Delta V_{DC} = \Delta V_{Cd1} + \Delta V_{Cd2} + \Delta V_{Cd3} = (I_{sm}/2\omega_r)(1/C_{d1} - 1/C_{d2} - 1/C_{d3} + offset_r\,(1/C_{d1} + 1/C_{d2} + 1/C_{d3}))\cos(\omega_r t +2\pi/3) - (I_{om}/2\omega_i)(1/C_{d1} - 1/C_{d2} - 1/C_{d3} + offset_i(1/C_{d1}+1/C_{d2}+1/C_{d3}))\cos(\omega_i t + 5\pi/6 - \varphi) \quad (49)$$

As it can be seen in (47), the total capacitor voltage ripple has two component with the input and output frequency of the converter. Considering (49), the capacitor sizes in different offset values should be chosen so as to minimize the DC link voltage ripple. For instant by considering *offsetr*=0.5 and *offseti*=-0.5, if *Cd1=Cd3=2Cd2*, then total DC link voltage ripple is eliminated. This method gives the possibility to reduce the capacitor sizes significantly. Fig. 14 shows the measured waveforms of the DC link voltage and voltage ripple in proposed converter. Simulation parameters are tabulated in Table IV and *offsetr* and $offset_i$ are respectively 0.5 and -0.5. As it is apparent in the figure, the proposed voltage ripple cancellation method reduces the voltage ripple even if the capacitor sizes are chosen smaller.

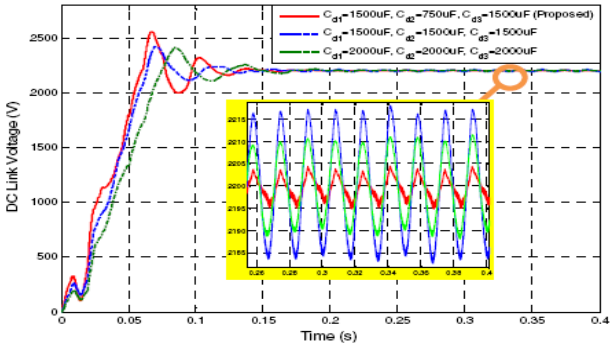


Figure 14: Waveforms of DC link voltage of proposed converter in different capacitor sizes

V. CONTROL OF THE AC/AC CONVERTER

The structure of the control system is shown in Figs. 18 and 19.The control system is composed of two parts: 1) Control of the three-phase rectifier, 2) control of the three-phase inverter. Since the modulation signals of the inverter and rectifier stages are produced independently, all the existing methods of controlling the DC bus voltage in three-phase rectifiers and three-phase inverters are applicable to the proposed structure. Control of the VSC is realized by DSP and FPGA systems. Due to the nature of a typical discrete time system, one control period delay is inevitable. As a result, delay effect compensation is an important factor of an acceptable converter controller. To solve this problem, dq0 current control method is
proposed for controlling the rectifier and inverter part of the converter.

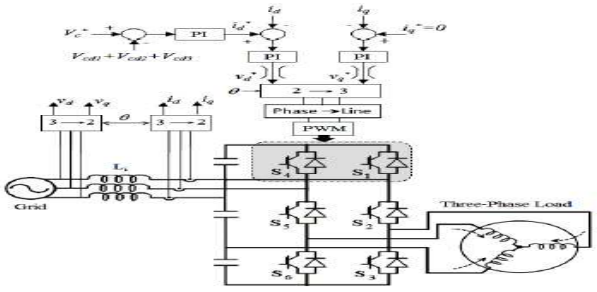


Figure 15: Block diagram of control method for rectifier side of proposed converter

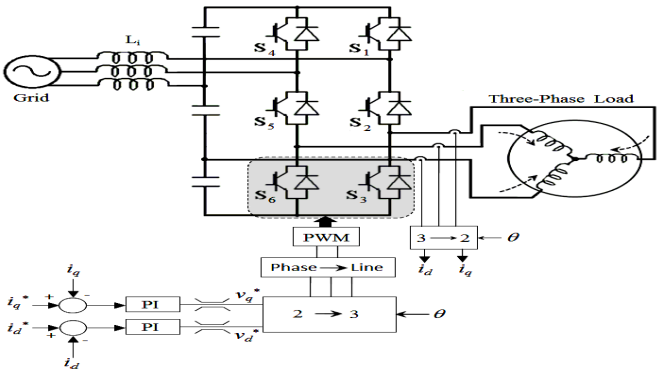


Figure 16: Block diagram of dq0 current control method for inverter part of proposed converter

A. Control of the three-phase rectifier

The control method of the rectifier side is the same as that analyzed in [17]. According to this method, active and reactive power control can be achieved by controlling direct and quadrature current components, respectively. DC voltage is set by controlling active power (Fig.16). The advantages of this method are constant switching frequency, low THD of input current, fast dynamic and unity power factor.

B. Control of the three-phase inverter

With applying the transformation method from three-phases system abc to rotating frame dq and using the block diagram shown in Fig. 16 we can control three-phase load current and therefore this algorithm can be easily implemented to control induction motors using vector control and direct torque control. The gate signal for mid switch is logic value generated by the logical XOR value of the gate signals for upper and lower switches.

VI. SIMULATION RESULT

To verify the performance of the proposed six-switch three phase to three-phase AC/AC converter, several simulation tests are performed by simulink ®software .The simulation parameters are listed in Tables 4. Because the input grid frequency is different from the output frequency variable frequency operation mode is selected. Furthermore, the modulation space is equally divided between the rectifier and inverter sides and hence $offset_r$ and $offset_i$ are set to 0.5 and -0.5, respectively and the DC link coefficients are set to a=1/4, b=1/2 and c=1/4. The proposed method in section V is used for calculating the DC-link capacitor sizes.

A. Normal operation of proposed system

In order to evaluate the performance of the proposed system, simulation is first performed in normal operation condition. Fig. 17 shows DC link capacitors' voltages. It can be seen that the voltages have low ripple and have followed their corresponding commands, i.e. *VCd1*= (1/4) *VDC*, *VCd2*= (1/2) *VDC* and *VCd3*= (1/4) *VDC*. Total DC link voltage of the converter was shown in Fig. 7 in this case. As Fig. 18 shows, the input reactive power is almost zero which means the reactive power compensation is achieved and the input power factor is corrected. This can also be seen from Fig. 19 in which the voltage and the current of first phase of grid are in phase. In Fig.18 the active power extracted from the grid is slightly higher than the active power delivered to the load due to the power losses of the proposed converter. Fig. 20 shows the grid currents and spectra of grid current with a fundamental frequency of 60Hz. Its total harmonic distortion is 4.23%.Fig. 21 shows the simulated waveforms of the rectifier input voltage $V_{AB}r$ and the inverter output voltage V_{ABi}. The three phase load currents are shown in Fig. 22. It is apparent in the figure that i_C is more distorted than the other two phase currents. It is because that i_C is produced by V_{CS} which has higher ripple than V_{AS} and V_{BS} .

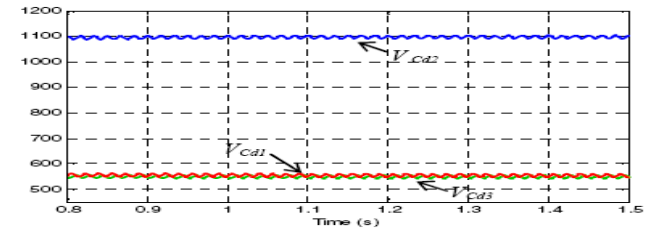


Figure 17: Capacitor voltages of DC-link

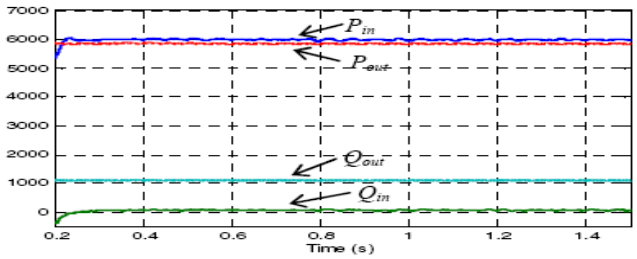


Figure 18: Active and reactive power extracted from grid and active and reactive power delivered to load

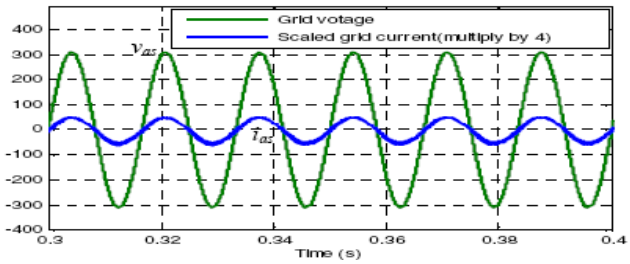
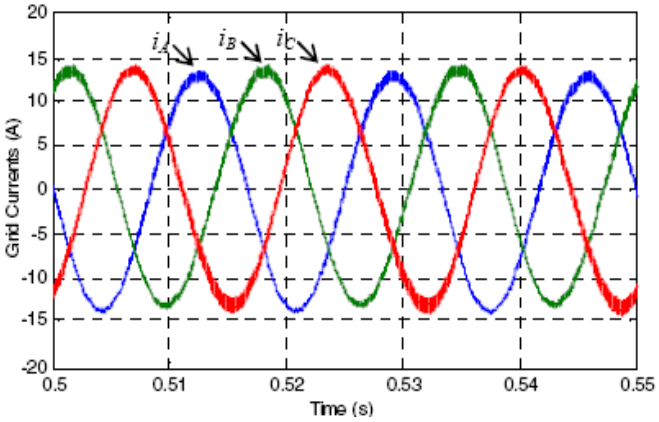
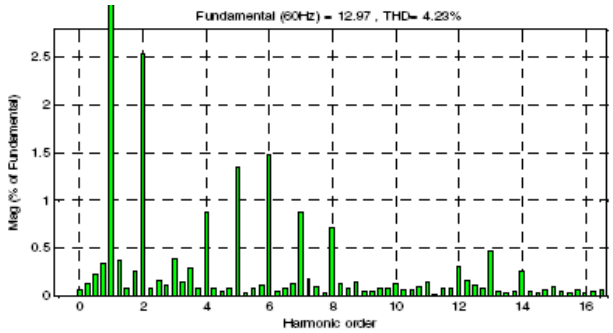


Figure 19: Grid voltage and extracted current from the grid



(a)



(b)

Figure 20: (a) Three phase currents of the grid, (b) Spectra of grid current

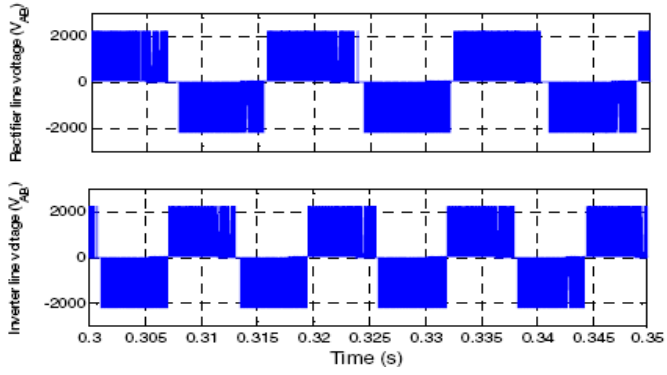


Figure 21: Rectifier line voltage and inverter line voltage (V_{BA})

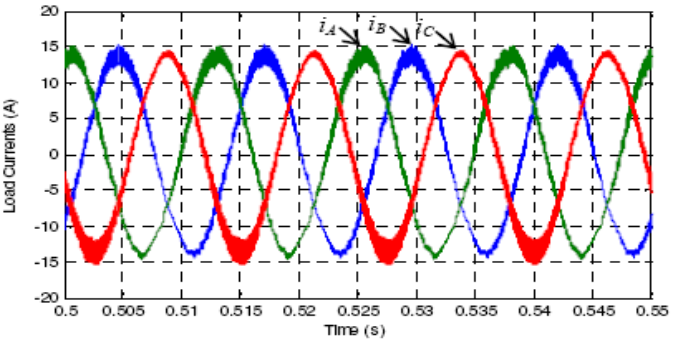


Figure 22. Load currents

B. System operation under grid voltage sag

To verify dynamics of the proposed system, the rms value of the grid line to line voltage has been varied from 380V to 270V in t=0.8 sec. The previous simulation was repeated under grid voltage sag operation. Fig. 23 shows DC link voltage which is almost constant. As seen in Fig. 24, the grid voltage sag has not affected the delivered power to the load Moreover, the reactive power is a gain compensated. To compensate for the sagged input voltage, the magnitude of input current has increased (Fig. 25).The load currents which have remained intact despite the grid voltage sag is shown in Fig. 26.

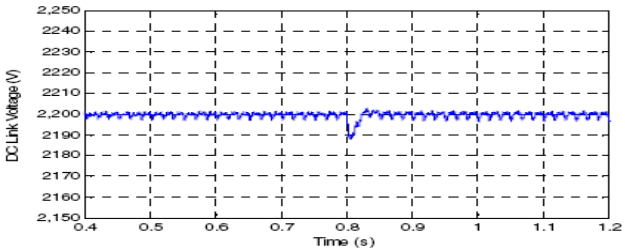


Figure 23: DC link voltage under grid voltage sag

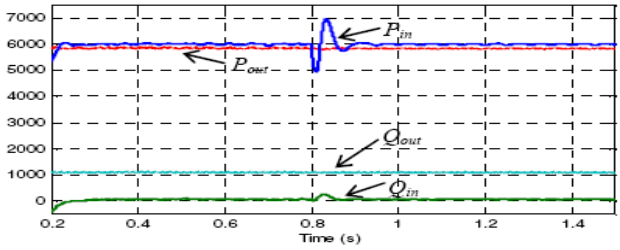


Figure 24: Active and reactive power extracted from grid and active and reactive power delivered to load under grid voltage sag

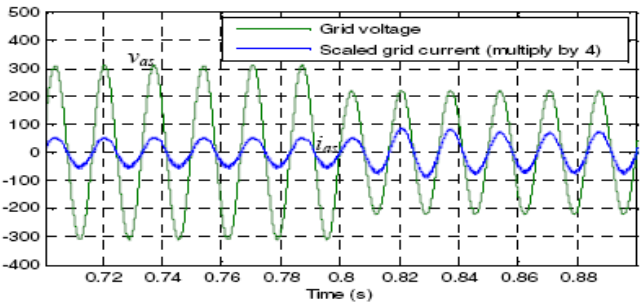


Figure 25: Grid voltage and extracted current from grid under grid voltage sag

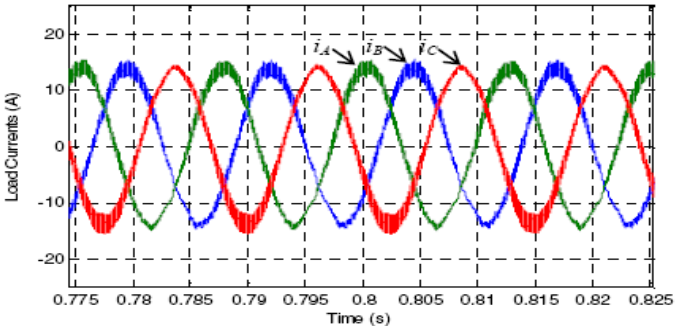


Figure 26: Load currents

VII. CONCLUSION

In this thesis paper, a three-phase to three-phase AC/AC converter with six active switches was proposed. It has the lowest number of active switches among three-phase to three phase AC/AC converters. The proposed converter topology was introduced and its modulation scheme was developed. Due to minimize the voltage ripple of the DC link the analysis of sizing of the DC link capacitors is performed and capacitor sizes are chosen It also led to the possibility of making al large reduction in the size of DC link capacitors. Compared to the conventional reduced switch count AC/AC converter which uses 8 active devices, the number of switches in the proposed converter is reduced by 25%. The number of switches and hence drive circuits is reduced.

- Despite higher voltage stress, manufacture cost can still
- Become lower especially in low voltage designs.
- High reliability
- Unity input power factor
- Less size and weight

REFERENCES

[1] M. H. Bierhoff and F. W. Fuchs, "Pulse Width Modulation for Current Source Converters – A Detailed Concept," in Proceedings of the 32nd IEEE IECON'06, Paris, France, Nov. 7–10, 2006.

[2] L. Wei and T. A. Lipo, "A Novel Matrix Converter Topology with Simple Commutation", in Proceedings of the 36th IEEE IAS'01, Chicago, USA, vol. 3, pp. 1749–1754, Sept. 30 – Oct. 4, 2001

[3] H. W. Van Der Broeck, and J. D .Van Wyk, "A comparative investigation of a three-phase induction machine drive with a component minimized voltage-fed inverter under different control options," IEEE Trans. on Industry Applications, vol. IA-20, no. 2, pp. 309–320, 1984.

[4] S. M. Dehghan, M. Mohamadian, and A. Yazdian, "Hybrid Electric Vehicle Based on Bidirectional Z-Source Nine-Switch Inverter," IEEE Trans. on Vehicular Technology, vol.59, pp.2641-2653, 2010.

[5] M. Heydari, A. Yazdian, M. Mohamadian and H. Zahedi, "A NovelVariable-Speed Wind Energy System Using Permanent-Magnet Synchronous Generator and Nine-Switch AC/AC Converter" 1st Power Electronic & Drive System Technologies Conference (PEDSTC), Tehran, Iran, pp.5 – 9, 2010.

[6] G. T. Kim and T. A. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," in Proc. IEEE IAS Annu. Meeting, pp. 2327–2332, 1995.

[7] Vinod Kumar Khanna, "Insulated Gate Bipolar Transistor (IGBT): Theory and Design" IEEE Press, Wiley-Interscience

[8] I. Takahashi and Y. Itoh, "Electrolytic Capacitor-Less PWM Inverter", in Proceedings of the IPEC'90, Tokyo, Japan, , pp.131–138, April 2–6, 1990.

[9] W. I. Popow, "Der zwangskommutierte Direktumrichter mit sinusförm Ausgangsspannung," Elektrie 28, No. 4, pp. 194 – 196, 1974

[10] K. Kuusela, M. Salo and H. Tuusa, "A Current Source PWM Converter Fed Permanent Magnet Synchronous Motor Drive with Adjustable DCLink Current", in Proceedings of the NORPIE'2000, Aalborg, Denmark, pp. 54 – 58, June 15 – 16, 2000.

[11] L. Gyugyi and B. R. Pelly, "Static Power Frequency Changers - Theory, Performance, & Application", New York: J. Wiley, 1976.

[12] J. Holtz and U. Boelkens, "Direct Frequency Converter with Sinusoidal Line Currents for Speed-Variable AC Motors", IEEE Transactions Electronics, Vol. 36, No. 4, pp. 475–479, 1989.

[13] L. Congwei, W. Bin, N. R. Zargari, and X. Dewei, "A Novel Three-Phase Three-Leg AC/AC Converter Using Nine IGBTs," IEEE Trans. on Power Electronics, vol. 24, no. 5, pp. 1151–1160, 2009.

[14] D. C. Lee and Y. S. Kim, "Control of Single-Phase-to-Three-Phase AC/DC/AC," IEEE Trans. on Aerospace and Electronic Systems, vol. 54, no. 2, pp. 797–804, APRIL 2007.

[15] M. D. Bellar, B. K. Lee, B. Fahimi, and M. Ehsani, "An ac motor drive with power fator control for low cost applications," IEEE-Applied Power Eletronics Conference – Piscataway, vol. 1, pp. 601–607, 2001.

[16] C. B. Jacobina, E. R. C. Silva, M. B. R. Corra, and A. M. Lima, "Ac motor drive systems with a reduced-switch-count converter," IEEE Trans. On Industry Applications, vol. 39, pp. 1333–1342, setember/october 2003.

[17] T. Kominami, and Y. Fujimoto, "A Novel Nine-Switch Inverter for Independent Control of Two Three-phase Loads," IEEE Industry Applications Society Annual Conference (IAS) , pp. 2346-2350, 2007.

[18] M. Heydari, A. Yazdian, M. Mohamadian, A. Fatemi, "A Novel Dual-Output Six-Switch Three-Phase Inverter"37th Annual Conference of IEEE Industrial Electronics Society(IECON'11),Melbourne,Australia, 2011.