Multilevel Direct Torque Balancing Control of Double Star Synchronous Machine

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***Abstract* –This paper deals with the direct torque control of the salient-pole double star synchronous machine drive fed by two five-level diode-clamped inverters. This approach combines the well-known advantages of the multilevel inverter with those of a direct torque control. The resulting control scheme presents enough degrees of freedom to control both torque and flux with very low ripple and high dynamics. Unfortunately, the diode-clamped inverter has an inherent problem of dc-link capacitors voltages variations. This drawback can be solved in satisfactory way by using multilevel direct torque control equipped by a balancing strategy. Simulations results are given to show the effectiveness of proposed control approach.**

Keywords – Double Star Synchronous Machine; Multi-level Diode Clamped Inverter; Direct Torque Control; Balancing Strategy.

I. INTRODUCTION

A multiphase drive has more than three phases in the stator and the same number of inverter legs is in the inverter side. The main advantages of multiphase drives over conventional three-phase drives include increasing the inverter output power, reducing the amplitude of torque ripple and lowering the DC link current harmonics. Furthermore, the multiphase drive system is able to improve the reliability. Indeed, the motor can start and run since the loss of one or many phases [1, 2]. Last two decades, the multiphase drive systems have been used in many applications, such as traction, electric/hybrid vehicles, and ship propulsion [3, 4].

The multiphase machine used in electrical drive systems are in principle the same as their three-phase counterparts. These include asynchronous and synchronous multiphase machines. Synchronous multiphase machines may be with permanent magnet excitation or with field winding excitation [5], among these types of machines; the salient-pole double star synchronous machine (DSSM) is one of the most useful of multiphase machines. This kind of machine contains double stators displaced by 30 degrees; the rotor is similar to the rotor of a simple synchronous machine and it's excited by constant current source.

The feeding of the DSSM is generally assured by two two-level inverters. However, for the high power; multilevel inverters are often required. Since the advantages of multilevel inverters and multiphase machines complement each other, it appears to be logical to try to combine them by realizing a multilevel multiphase drive.

Several topologies of multilevel inverters have been proposed in the technical literatures [6, 7]. The diode-clamped inverter (DCI) represents one of the most interesting solutions, to increase voltage and power levels and to achieve high quality voltage waveforms [8]. This makes the DCI an attractive solution to high power drive systems. However, a very important issue in using a DCI is the ability to guarantee the stability of the DC-link capacitors voltages [9]. Several methods are proposed to suppress the unbalance of DC-link capacitors voltages. Some of these methods are based on adding a zero sequence or a DC-offset to output voltage [10]. Auxiliary power electronics circuitry is added to redistribute charges between capacitors [11]. SVM based DC capacitors voltages balancing method, which exploits the SVM switching vector redundancy to mitigate DC capacitors voltages drift [12]. A method based on minimizing a quadratic parameter that depends on capacitor voltages is presented in [13].

In the other hand, many studies have been developed to find out different solutions for the DSSM control having the features of precise and quick torque response [14, 15, 16]. The direct torque control (DTC) has been recognized as the most promising solution to achieve these requirements. The DTC is based on the decoupled control of flux and torque providing a very quick and robust response [3]. Its simplicity, robustness and fast torque response are the major factors make it popular in industries [1]. In the classical DTC scheme using two-level inverter, due to the limited number of voltage vectors the torque and flux ripples are high. In order to overcome this problem, many contributions have been made that extent DTC to multilevel topologies [17, 18].

To improve the performances of a double star synchronous machine, a multilevel DTC with balancing strategy based on the redundancy of switching states is proposed in this paper in order to accomplish two objectives: balance the DC-link capacitors voltages, and ensure a high performance of the multiphase drive.

The present paper structure is as follows. The section II is dedicated to the modeling of the double star synchronous machine. A suitable transformation matrix is used to develop a simple dynamic model. The model of the five-level DCI is presented in the section III. In the section IV, the five-level DTC approach is presented. Comparative study between two-level DTC and five-level DTC for DSSM is presented in the

section V. The section VI is reserved to balancing analysis of the proposed control strategy. In the section VII, the simulation results related to the five-level DTC with and without balancing strategy are presented and discussed.

II. MODELING OF THE DOUBLE STAR SYNCHRONOUS MACHINE

The following assumptions have been made in deriving the machine model:

- The MMF in air-gap has a sinusoidal repartition.
- The saturation of the iron in machine is neglected.

The stator voltage equation for six-phase can be written as:

$$v_s = R_s i_s + \frac{d}{dt}\phi_s \tag{1}$$

The rotor voltage equation is given by:

$$v_f = R_f i_f + \frac{d}{dt}\phi_f \tag{2}$$

The original six dimensional system of the machine can be decomposed into three orthogonal subspaces (α,β), (z_1,z_2) and (z_3,z_4) [5], using the following transformation.

$$\left[X_\alpha \;\; X_\beta \;\; X_{z1} \;\; X_{z2} \;\; X_{z3} \;\; X_{z4}\right]^T = [A][X_s] \tag{3}$$

With

$$[X_s] = [X_{a1} \;\; X_{b1} \;\; X_{c1} \;\; X_{a2} \;\; X_{b2} \;\; X_{c2}]^T$$

Where: X_s represents stator currents (i_s), stator flux (ϕ_s), and stator voltages (v_s).

The matrix *A* is given by:

$$[A] = \frac{1}{\sqrt{3}}\begin{bmatrix} \cos(0) & \cos\left(\frac{2\pi}{3}\right) & \cos\left(\frac{4\pi}{3}\right) & \cos(\gamma) & \cos\left(\frac{2\pi}{3}+\gamma\right) & \cos\left(\frac{4\pi}{3}+\gamma\right) \\ \sin(0) & \sin\left(\frac{2\pi}{3}\right) & \sin\left(\frac{4\pi}{3}\right) & \sin(\gamma) & \sin\left(\frac{2\pi}{3}+\gamma\right) & \sin\left(\frac{4\pi}{3}+\gamma\right) \\ \cos(0) & \cos\left(\frac{4\pi}{3}\right) & \cos\left(\frac{2\pi}{3}\right) & \cos(\pi-\gamma) & \cos\left(\frac{\pi}{3}-\gamma\right) & \cos\left(\frac{5\pi}{3}-\gamma\right) \\ \sin(0) & \sin\left(\frac{4\pi}{3}\right) & \sin\left(\frac{2\pi}{3}\right) & \sin(\pi-\gamma) & \sin\left(\frac{\pi}{3}-\gamma\right) & \sin\left(\frac{5\pi}{3}-\gamma\right) \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix} \tag{4}$$

II.1. Machine model in $\alpha-\beta$ reference frame

The dynamic model describing the machine in $\alpha-\beta$ vector space can be given by:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = R_s \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} l_{fs}+3M_{ss} & 0 \\ 0 & l_{fs}+3M_{ss} \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \sqrt{3}M_{sf}\frac{d}{dt}\begin{bmatrix} \cos(\theta) \\ \sin(\theta) \end{bmatrix} i_f + M_{sfm}\begin{bmatrix} 3\cos(2\theta) & 3\sin(2\theta) \\ 3\sin(2\theta) & -3\cos(2\theta) \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5}$$

II.2. Machine model in z_1, z_2, z_3, z_4 reference frame

The stator voltages equation is

$$\begin{bmatrix} v_{z1} \\ v_{z2} \\ v_{z3} \\ v_{z4} \end{bmatrix} = R_s \begin{bmatrix} i_{z1} \\ i_{z2} \\ i_{z3} \\ i_{z4} \end{bmatrix} + \begin{bmatrix} l_{fs} & 0 & 0 & 0 \\ 0 & l_{fs} & 0 & 0 \\ 0 & 0 & l_{fs} & 0 \\ 0 & 0 & 0 & l_{fs} \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_{z1} \\ i_{z2} \\ i_{z3} \\ i_{z4} \end{bmatrix} \tag{6}$$

The harmonic currents i_{z1} and i_{z2} must be as low as possible to reduce the extra losses in the DSSM. These currents are only limited by stator resistance and leakage inductance.

The currents i_{z3} and i_{z4} are equal to zero because the two three-phase windings are connected with isolated neutrals.

II.3. Machine model in rotor reference frame d–q

To express the stator and rotor equations in the same stationary reference frame, the following rotation transformation is adopted

$$P(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \tag{7}$$

With this transformation, the components of the $\alpha-\beta$ plane can be expressed in the *d-q* plane as:

The electrical equations

$$\begin{cases} v_d = R_s i_d + \frac{d\phi_d}{dt} - \omega\phi_q \\ v_q = R_s i_q + \frac{d\phi_q}{dt} + \omega\phi_d \\ v_f = R_f i_f + \frac{d\phi_f}{dt} \end{cases} \tag{8}$$

The flux equations

$$\begin{cases} \phi_d = L_d i_d + M_{fd} i_f \\ \phi_q = L_q i_q \\ \phi_f = L_f i_f + M_{fd} i_d \end{cases} \tag{9}$$

The mechanical equation

$$J\frac{d\Omega}{dt} = T_{em} - T_L - f_r\Omega \tag{10}$$

The electromagnetic torque

$$T_{em} = p(\phi_d i_q - \phi_q i_d) \quad (11)$$

III. STRUCTURE OF FIVE-LEVEL INVERTER

Figure 1 shows a schematic diagram of a three-phase five-level diode-clamped VSI inverter. In this circuit, the DC-bus voltage is split into five levels by four series-connected bulk capacitors, C_1, C_2, C_3, and C_4. Ideally, each capacitor voltage is equal to $V_{cj}=(V_{dc}/4)$, $j = 1,\ldots ,4$ and each generated phase voltage has five levels with respect to the voltage of middle point ''*o*'': $-v_{dc}/2$, $-v_{dc}/4$, 0, $v_{dc}/2$ and $v_{dc}/4$ [9]. Gating signals S_{kx1}, S_{kx2}, S_{kx3} and S_{kx4} (with: *x=a, b or c*) are generated by DTC switching tables. There are four complimentary switch pairs in each phase. For a complimentary switch pair, turning on one of the switches excludes the other from being turned on. Using phase-a as an example, the four complementary pairs are (S_{ka1}, S_{ka5}), (S_{ka2}, S_{ka6}), (S_{ka3}, S_{ka7}), and (S_{ka4}, S_{ka8}). Gating signals S_{kx5}, S_{kx6}, S_{kx7} and S_{kx8} are simply generated by inverting S_{kx1}, S_{kx2}, S_{kx3} and S_{kx4}, respectively.

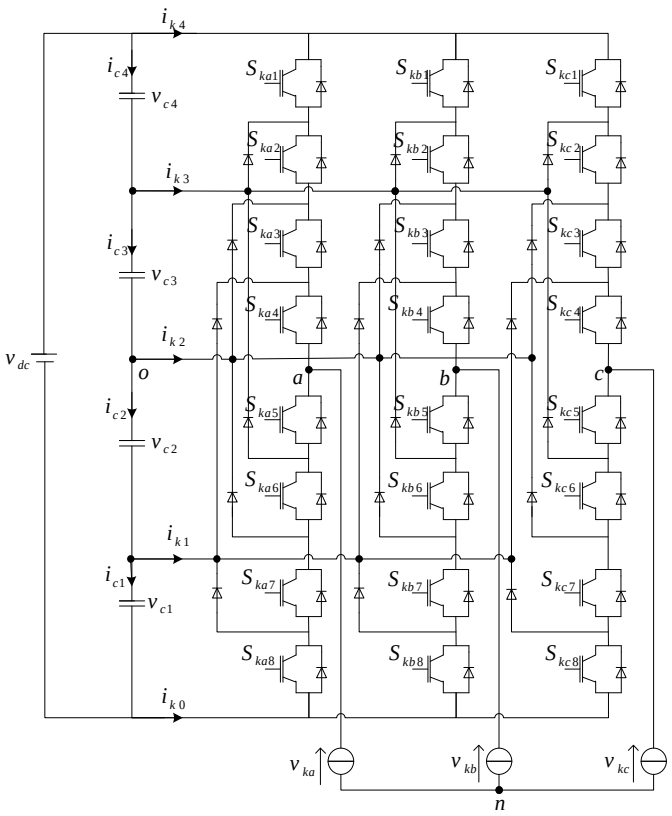

Fig. 1. Structure of five-level diode-clamped inverter (*k=1* for first inverter and *k=2* for second inverter).

Each leg of the inverter has five possible switching states:

- State 4: The upper switching devices S_{kx1}, S_{kx2}, S_{kx3} and S_{kx4} are closed. The output phase to neutral point voltage $v_{kxo} = v_{c3} + v_{c4}$.
- State 3: The switching devices S_{kx2}, S_{kx3}, S_{kx4} and S_{kx5} are closed. The output phase to neutral point voltage $v_{kxo} = v_{c3}$.
- State 2: The switching devices S_{kx3}, S_{kx4}, S_{kx5} and S_{kx6} are closed. The output phase to neutral point voltage $v_{kxo} = 0$.
- State 1: The switching devices S_{kx4}, S_{kx5}, S_{kx6} and S_{kx7} are closed. The output phase to neutral point voltage $v_{kx} = -v_{c2}$.
- State 0: The lower switching devices S_{kx5}, S_{kx6}, S_{kx7} and S_{kx8} are closed. The output phase to neutral point voltage $v_{kxo} = -(v_{c1} + v_{c2})$.

Projection of the vectors on *α-β* coordinates forms a four layer hexagon centered at the origin of the *α-β* plane. Zero voltage vectors are located at the origin of the plane. The switching states are illustrated by *0*, *1*, *2*, *3*, and *4* in the figure 2.

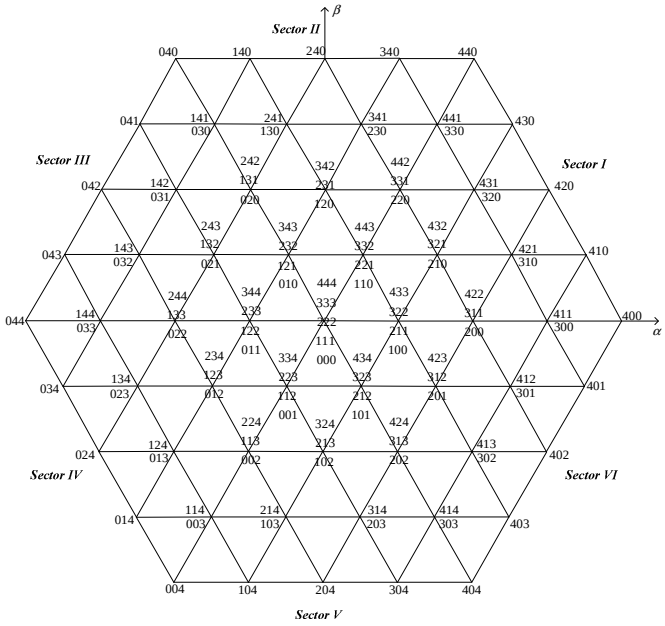

Fig. 2. Space voltage vectors for a five-level diode-clamped inverter.

For each switching device S_{kxi} (*k=1, 2, i= 1… 8, x*=a, b *or* c), a Boolean function F_{kxi} is defined by:

$$F_{kxi} = \begin{cases} 1 \; if \;\; S_{kxi} \;\; is \;\; ON \\ 0 \; if \;\; S_{kxi} \;\; is \;\; OFF \end{cases} \quad (12)$$

The complementarities between upper and lower switching devices of each leg impose the following equations:

$$F_{kxi} = 1 - F_{kx(i-4)} \quad (13)$$

For each leg of the inverter, five connection functions are defined as follow:

$$\begin{cases} F_{ckx1} = F_{kx1}F_{kx2}F_{kx3}F_{kx4} \\ F_{ckx2} = F_{kx2}F_{kx3}F_{kx4}F_{kx5} \\ F_{ckx3} = F_{kx3}F_{kx4}F_{kx5}F_{kx6} \\ F_{ckx4} = F_{kx4}F_{kx5}F_{kx6}F_{kx7} \\ F_{ckx5} = F_{kx5}F_{kx6}F_{kx7}F_{kx8} \end{cases} \quad (14)$$

The phase voltages v_{ka}, v_{kb}, v_{kc} can be written as:

$$\begin{pmatrix} v_{ka} \\ v_{kb} \\ v_{kc} \end{pmatrix} = \begin{pmatrix} F_{cka1} & F_{cka2} & F_{cka3} & F_{cka4} & F_{cka5} \\ F_{ckb1} & F_{ckb2} & F_{ckb3} & F_{ckb4} & F_{ckb5} \\ F_{ckc1} & F_{ckc2} & F_{ckc3} & F_{ckc4} & F_{ckc5} \end{pmatrix} \begin{pmatrix} v_{c3}+v_{c4} \\ v_{c3} \\ 0 \\ -v_{c2} \\ -(v_{c1}+v_{c2}) \end{pmatrix} \quad (15)$$

IV. DIRECT TORQUE CONTROL STRATEGY

The well-known DTC strategy is based on flux and torque control using hysteresis comparators. These controllers use the estimated errors of the control variables at each sampling time of operation. The considered flux and torque controllers ensure the separate control of these two variables, as for the DC drives. When the level of torque or stator flux passes to the high or low hysteresis limit, a suitable voltage vector is applied to bring back each variable in its corresponding band [5].

The DTC block diagram of DSSM supplied by five-level DCI in each star is represented by figure (3). It includes closed loop control of speed using PI controller.

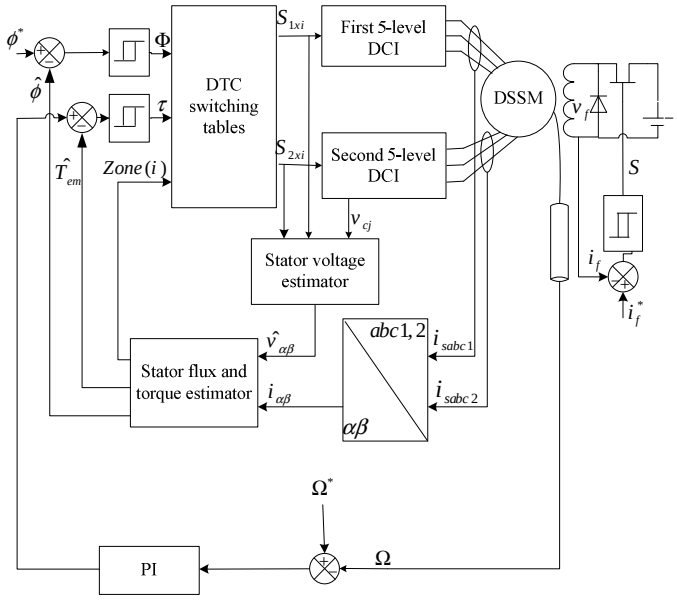

Fig. 3.Five-level DTC scheme without balancing strategy.

The stator voltage estimator is based on the following equation:

$$\begin{bmatrix} \hat{v}_\alpha \\ \hat{v}_\beta \end{bmatrix} = [A] \begin{bmatrix} \hat{v}_{s1} \\ \hat{v}_{s2} \end{bmatrix} \quad (16)$$

With: $\hat{v}_{s1} = [\hat{v}_{1a} \quad \hat{v}_{1b} \quad \hat{v}_{1c}]$ and $\hat{v}_{s2} = [\hat{v}_{2a} \quad \hat{v}_{2b} \quad \hat{v}_{2c}]$

Where $\hat{v}_{kx}, k = 1, 2, x = a,b,c$ are computed using (15).

The stator flux can be evaluated by integrating the estimated stator voltage equation:

$$\begin{cases} \hat{\phi}_\alpha = \int_0^t (\hat{v}_\alpha - R_s i_\alpha) d\tau + \hat{\phi}_\alpha(0) \\ \hat{\phi}_\beta = \int_0^t (\hat{v}_\beta - R_s i_\beta) d\tau + \hat{\phi}_\beta(0) \end{cases} \quad (17)$$

The electromagnetic torque can be estimated by:

$$\hat{T}_{em} = p(\hat{\phi}_\alpha i_\beta - \hat{\phi}_\beta i_\alpha) \quad (18)$$

DTC requires accurate knowledge of the magnitude and angular position of stator flux [19]. The relation between stator flux magnitude and its components in plane $\alpha\beta$ is given by equation (19):

$$|\hat{\phi}| = \sqrt{\hat{\phi}_\alpha^2 + \hat{\phi}_\beta^2} \quad (19)$$

The actual position of the stator flux can be determined by equation (20), from the orthogonal flux components:

$$\hat{\theta}_s = \arctan\left(\frac{\hat{\phi}_\beta}{\hat{\phi}_\alpha}\right) \quad (20)$$

Figure 4 shows the switching states of the five-level DCI for one phase.

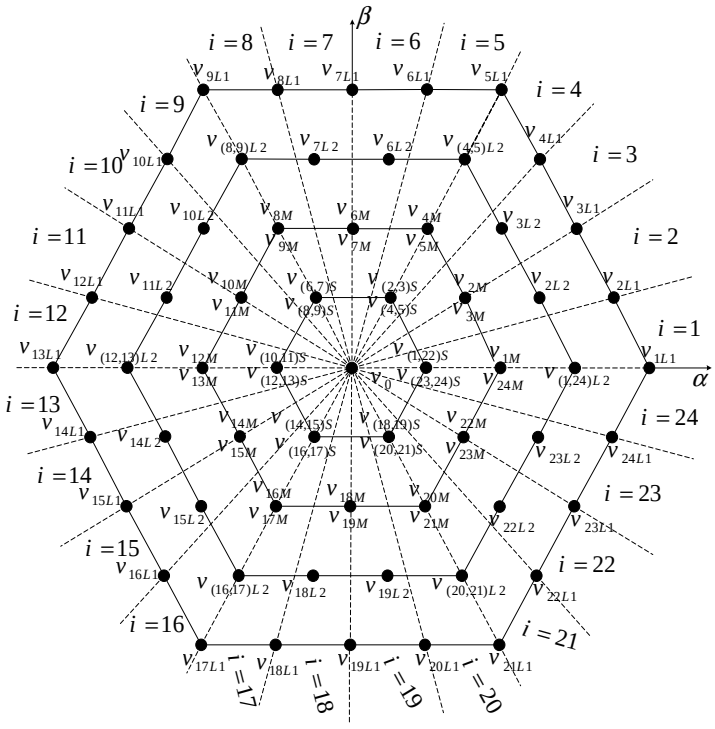

Fig. 4. Switching states of the five-level DCI.

Since five kinds of switching states exist in each phase, a five-level inverter has 125 switching states and there are 61 effective vectors. According to the magnitude of the voltage vectors, the five-level DCI is divide into nine (9) groups (v_0), (v_1, v_2, v_3, v_4, v_5, v_6),(v_{44}, v_{45}, v_{46}, v_{47}, v_{48}, v_{49}), (v_{26}, v_{27}, v_{28}, v_{29}, v_{30}, v_{31}), (v_{75}, v_{76}, v_{77}, v_{78}, v_{79}, v_{80}, v_{81}, v_{82}, v_{83}, v_{84}, v_{85}, v_{86})(v_{63}, v_{64}, v_{65}, v_{66}, v_{67}, v_{68}), (v_{118}, v_{119}, v_{120}, v_{121}, v_{122}, v_{123}), (v_{106}, v_{107}, v_{108}, v_{109}, v_{110}, v_{111}, v_{112}, v_{113}, v_{114}, v_{115}, v_{116}, v_{117}), (v_{100}, v_{101}, v_{102}, v_{103}, v_{104}, v_{105}).

The conventional DTC consists to select stator voltage vectors, according to the differences between the stator flux linkage and electromagnetic torque and their references [3].

The reference values of flux and torque are compared to their estimated values and the resulting errors are fed into a two-level flux hysteresis comparator and a five-level torque hysteresis comparator.

The switching pattern of the DCI is selected based on the output of a pair of hysteresis controllers for both torque and stator flux. In order to adjust the electromagnetic torque and the stator flux linkage, the DTC algorithm chooses the stator voltage space vector that produces the desired change [19].

Tables 1 and 2 present the output voltage vectors which are selected to change the torque angle. This is done based on the instantaneous torque requirement.

Φ	τ	$Zone(i)$	Φ	τ	$Zone(i)$	Φ	τ	$Zone(i)$
1	4	$v_{(i+4)L1}$	0	4	$v_{(i+6)L1}$	−1	4	$v_{(i+8)L1}$
	3	$v_{(i+4)L2}$		3	$v_{(i+6)L2}$		3	$v_{(i+8)L2}$
	2	$v_{(i+4)M}$		2	$v_{(i+6)M}$		2	$v_{(i+8)M}$
	1	$v_{(i+4)S}$		1	$v_{(i+6)S}$		1	$v_{(i+8)S}$
	0	v_0		0	v_0		0	v_0
	−1	$v_{(i+20)S}$		−1	$v_{(i+18)S}$		−1	$v_{(i+16)S}$
	−2	$v_{(i+20)M}$		−2	$v_{(i+18)M}$		−2	$v_{(i+16)M}$
	−3	$v_{(i+20)L2}$		−3	$v_{(i+18)L2}$		−3	$v_{(i+16)L2}$
	−4	$v_{(i+20)L1}$		−4	$v_{(i+18)L1}$		−4	$v_{(i+16)L1}$

Table 1. Switching table used in the conventional DTC of first star for the DSSM.

Φ	τ	$Zone(i)$	Φ	τ	$Zone(i)$	Φ	τ	$Zone(i)$
1	4	$v_{(i+2)L1}$	0	4	$v_{(i+4)L1}$	−1	4	$v_{(i+6)L1}$
	3	$v_{(i+2)L2}$		3	$v_{(i+4)L2}$		3	$v_{(i+6)L2}$
	2	$v_{(i+2)M}$		2	$v_{(i+4)M}$		2	$v_{(i+6)M}$
	1	$v_{(i+2)S}$		1	$v_{(i+4)S}$		1	$v_{(i+6)S}$
	0	v_0		0	v_0		0	v_0
	−1	$v_{(i+18)S}$		−1	$v_{(i+16)S}$		−1	$v_{(i+14)S}$
	−2	$v_{(i+18)M}$		−2	$v_{(i+16)M}$		−2	$v_{(i+14)M}$
	−3	$v_{(i+18)L2}$		−3	$v_{(i+16)L2}$		−3	$v_{(i+14)L2}$
	−4	$v_{(i+18)L1}$		−4	$v_{(i+16)L1}$		−4	$v_{(i+14)L1}$

Table 2. Switching table used in the conventional DTC of second star for the DSSM

V. COMPARATIVE STUDY

To verify the validity of the proposed controller, the system was simulated using the DSSM parameters given in Appendix *2*.

The DC side of the inverter is supplied by a constant DC source $v_{dc}=600V$. The simulation results are obtained using the following DC link capacitors values $C_1 = C_2 = C_3 = C_4 = 1mF$.

The aim of this section is to compare the two-level DTC for DSSM with the five-level DTC for DSSM. Two situations are considered:

Situation 1: Step change in load torque. The DSSM is accelerate from standstill to reference speed *100*rad/s. The system is started with full load torque (T_L = *11*N.m). After wards, a step variation on the load torque (T_L = *0*N.m) is applied at time *t=0.8*s. Finally, the load torque is reversed (T_L = *-11*N.m) at time *t=1.3*s.

As it can be seen from the figures 5 and 6, the employment of a multilevel DTC permits to obtain the same dynamic performances as those obtained with a two-level inverter with resulting far lower torque and flux ripples.

Situation 2: Step change in reference speed. To test the speed evolution of the system, the DSSM is accelerate from standstill to reference speed (*100* rad/s) afterwards it is decelerate to the inverse rated speed (*-100* rad/s) at time *t=1.5*s. The performances are presented in figures 5 and 6 for the two-level DTC and the five-level DTC respectively. Note that, the decoupling control is clearly maintained during speed variation. The speed response is merged with the reference one and the flux is very similar to the nominal value.

The five-level DTC for DSSM decrease considerably the torque ripple.

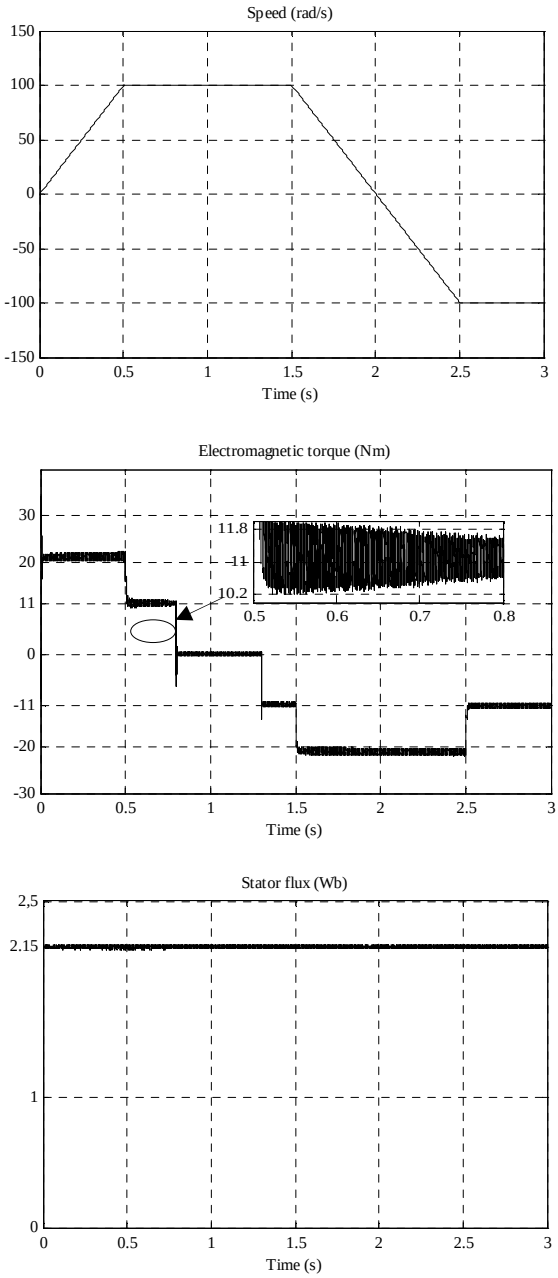

Fig. 5. Dynamic responses of conventional two-level DTC for DSSM.

The five-level DTC ensure good decoupling between stator flux linkage and electromagnetic torque. However, it can be seen perfectly the problem of the unbalance of the four DC voltages of the intermediate capacitors filter. Indeed, the voltages v_{c1} and v_{c4} decrease and the voltages $v_{c2}$and v_{c3} increase. In order to improve the performance of conventional five-level DTC DSSM, the five-level DTC based on balancing mechanism is proposed.

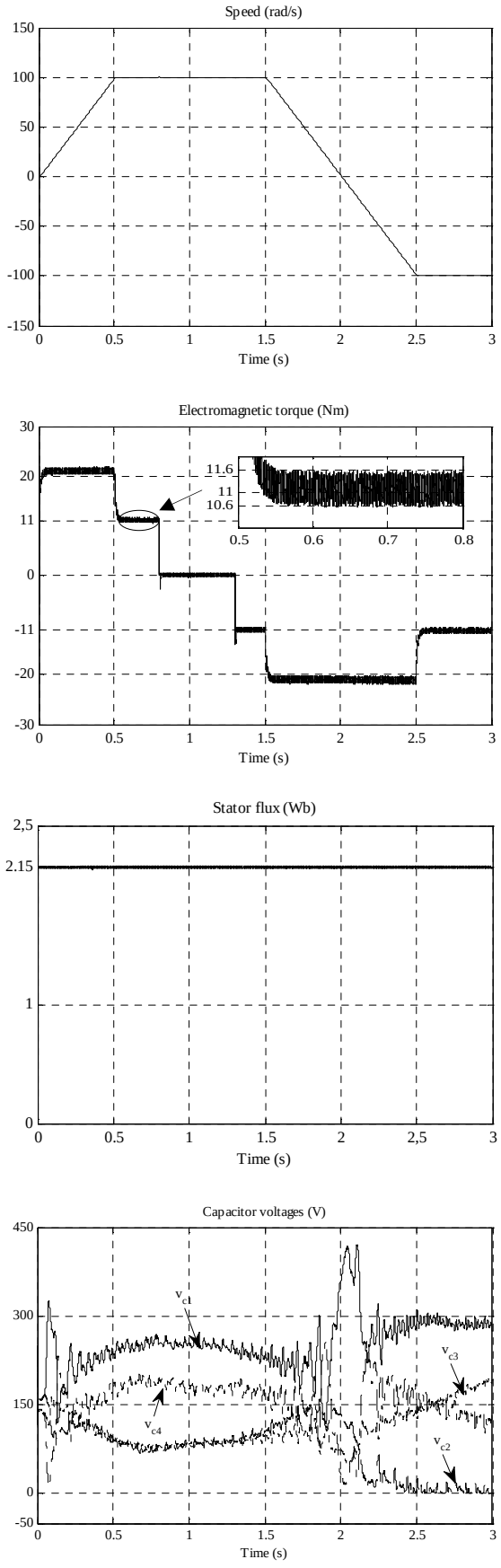

Fig. 6. Dynamic responses of conventional five-level DTC for DSSM.

VI. DC-CAPACITOR VOLTAGE BALANCING STRATEGY BASED ON MINIMUM ENERGY PROPERTY

The voltage balancing strategy proposed in this section uses the minimum energy property and cost function J for selection of redundant switching states of the two DCI units over a switching period.

In an *n*-level DCI, the total energy *E* of (*n* − 1) capacitor is:

$$E = \frac{1}{2}\sum_{j=1}^{n-1} C_j v_{cj}^2 \tag{21}$$

Where

$$\sum_{j=1}^{n-1}\left(v_{cj} - v_{dc}\right) = 0 \tag{22}$$

Assuming that all capacitors are identical, C_{n-1}= . . . C_2= C_1=C, the total energy E has its minimum of $(1/2)C\,(v_{dc}^2/n-1)$ when all capacitor voltages are equal [10].This condition is called the minimum energy property of a balanced *n*-level DCI, which can be used as a basis for the DC-capacitor voltage balancing and control. A control method should minimize (21) to achieve voltage balancing. By a change of variable from v_{cj} to $(v_{cj} - v_{dc}/(n-1))$ in (21) the positive definite cost function becomes:

$$J = \frac{1}{2}C\sum_{j=1}^{n-1}\left(v_{cj} - \frac{v_{dc}}{n-1}\right)^2 \tag{23}$$

For a five-level inverter, *J* can be simplified as:

$$J = \frac{1}{2}C\sum_{j=1}^{4} v_{cj}^2 \tag{24}$$

Where Δv_{cj} is a voltage deviation of capacitor C_j, $\Delta \mathrm{v}_{cj} = \mathrm{v}_{cj} - (\mathrm{v}_{dc}/4)$. Based on proper selection of redundant vectors, *J* can be minimized (ideally reduced to zero) if the capacitor voltages are maintained at voltage reference values of $(\mathrm{v}_{dc}/4)$. The mathematical condition to minimize *J* is:

$$\frac{dJ}{dt} = C\sum_{j=1}^{4}\Delta v_{cj}\frac{dv_{cj}}{dt} = \sum_{j=1}^{4}\Delta v_{cj} i_{cj} \tag{25}$$

Where i_{ckj} is the current through capacitor C_j, the capacitor currents i_{ckj} in (25) are affected by the DC-side intermediate branch currents i_{k3}, i_{k2} and i_{k1}. Currents i_{k3}, i_{k2} and i_{k1} can be calculated if the switching states used in the switching pattern are known. Thus, it is advantageous to express (25) in terms of i_{k3}, i_{k2} and i_{k1}. The DC-capacitor currents are expressed as:

$$i_{cj} = \frac{1}{4}\sum_{y=1}^{3} y\left(\sum_{k=1}^{2} i_{ky}\right) - \sum_{y=j}^{3}\left(\sum_{k=1}^{2} i_{ky}\right) \tag{26}$$

By substituting i_{ckj} calculated from (26) in (25), the condition to achieve voltage balancing, (25) is deduced as:

$$\sum_{j=1}^{4}\Delta v_{cj}\left(\frac{1}{4}\sum_{y=1}^{3} y\left(\sum_{k=1}^{2} i_{ky}\right) - \sum_{y=j}^{3}\left(\sum_{k=1}^{2} i_{ky}\right)\right) \le 0 \tag{27}$$

Since the net DC-link voltage is regulated at v_{dc}

$$\sum_{j=1}^{4}\Delta v_{cj} = 0 \tag{28}$$

Substituting Δv_{c4} calculates from (26), in (27) yields

$$\sum_{j=1}^{3}\Delta v_{cj}\left(\sum_{y=j}^{3}\left(\sum_{k=1}^{2} i_{ky}\right)\right) \tag{29}$$

Applying the averaging operator, over one sampling period, to (29) results in:

$$\frac{1}{T}\int_{KT}^{(K+1)T}\Delta v_{cj}\left(\sum_{y=j}^{3}\left(\sum_{k=1}^{2} i_{ky}\right)\right)dt \ge 0 \tag{30}$$

Assuming that sampling period *T*, as compared to the time interval associate with the dynamics of capacitor voltages, is adequately small, the capacitor voltages can be assumed to remain constant over one sampling period.

Equation (30) is simplified to:

$$\sum_{j=1}^{3}\Delta v_{cj}(K)\left(\sum_{y=j}^{3}\frac{1}{T}\int_{KT}^{(K+1)T}\left(\sum_{k=1}^{2} i_{ky}\right)\right)dt \ge 0 \tag{31}$$

Or

$$\sum_{j=1}^{3}\Delta v_{cj}(K)\left(\sum_{y=j}^{3}\left(\sum_{k=1}^{2}\bar{i}_{ky}\right)(K)\right)dt \ge 0 \tag{32}$$

Where:

$\Delta v_{cj}(K)$: is the voltage drift of C_j at sampling period *K*.

$\bar{i}_{ky}(K)$: is the averaged value of the j^{th} DC-side intermediate branch current.

To calculate $\bar{i}_{ky}$, y = 1, 2, 3, contributions of switching states to the DC side intermediate branch currents and relationship between the DC and AC side currents, i_{ka}, i_{kb} and i_{kc}, are required. The influence of switching states on a DC-side intermediate branch current and its relationship with phase currents, corresponding to sector I are shown in Table 3. When the tip of reference voltage vector v_{ref} is located in sector

I, the average values of the DC-side intermediate branch currents are

$$\begin{bmatrix} \bar{i}_{k3} \\ \bar{i}_{k2} \\ \bar{i}_{k1} \end{bmatrix} = \frac{1}{T} \begin{bmatrix} i_{k3} & 0 & 0 \\ 0 & i_{k2} & 0 \\ 0 & 0 & i_{k1} \end{bmatrix} \begin{bmatrix} T \\ T \\ T \end{bmatrix} \quad (33)$$

Switching state	i_{k3}	i_{k2}	i_{k1}
400	0	0	0
410	0	0	i_{kb}
420	0	i_{kb}	0
430	i_{kb}	0	0
440	0	0	0
411	0	0	$-i_{ka}$
300	i_{ka}	0	0
421	0	i_{kb}	i_{kc}
310	i_{ka}	0	i_{kb}
431	i_{kb}	0	i_{kc}
320	i_{ka}	i_{kb}	0
441	0	0	i_{kc}
330	$-i_{kc}$	0	0
422	0	$-i_{ka}$	0
311	i_{ka}	0	$-i_{ka}$
200	0	i_{ka}	0
432	i_{kb}	i_{kc}	0
321	i_{ka}	i_{kb}	i_{kc}
210	0	i_{ka}	i_{kb}
442	0	i_{kc}	0
331	$-i_{kc}$	0	i_{kc}
220	0	$-i_{kc}$	0
433	$-i_{ka}$	0	0
322	i_{ka}	$-i_{ka}$	0
211	0	i_{ka}	$-i_{ka}$
100	0	0	i_{ka}
443	i_{kc}	0	0
332	$-i_{kc}$	i_{kc}	0
221	0	$-i_{kc}$	i_{kc}
110	0	0	$-i_{kc}$

Table. 3. Current for different switching states in sector I.

For the conventional five-level DTC the cost function is given by:

$$J_k = \sum_{j=1}^{3} \Delta v_{cj}(K) \left(\sum_{y=j}^{3} \left(\sum_{k=1}^{2} \bar{i}_{ky} \right)(K) \right) \quad (34)$$

The currents $\bar{i}_{ky}$ ($y=1\ldots3$) are calculated based on (33) for each set of switching combinations, they are replaced in (34) and the best set that fulfills the condition is selected.

This study aims to demonstrate the effectiveness of the proposed DTC strategy to control and prevent drift of DC capacitor voltages. Figure 7 shows a schematic diagram of the five-level DTC balancing system including the DC capacitor voltage control strategy.

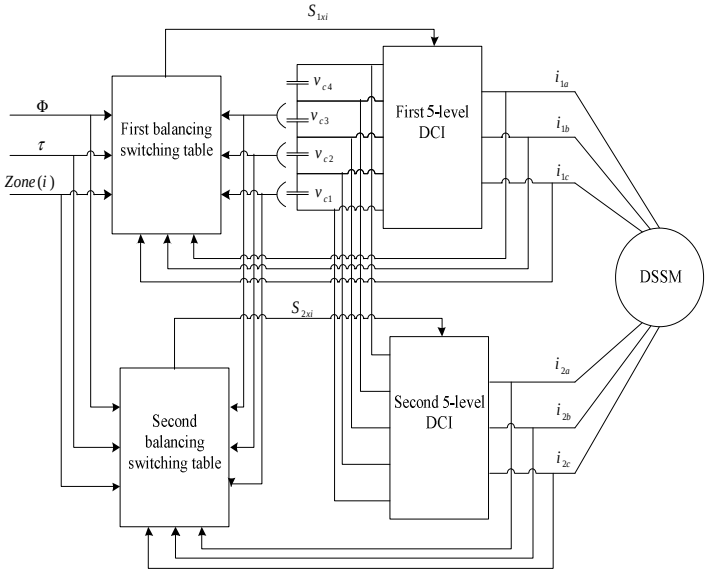

Fig. 7. Schematic representation of the five-level DTC with balancing strategy.

VII. SIMULATION RESULTS

The proposed DTC control of the double star synchronous machine supplied by two five-level voltage source inverters controlled via balancing switching table strategy is tested by digital simulation.

The obtained results are presented in figure 8 for the five-level DTC without balancing strategy and figure 9 for the five-level DTC with balancing strategy. The DSSM is accelerate from standstill to reference speed *100*rad/s. the system simulated with load torque (T_L = *11*N.m), afterwards it is step variation on the rated load (T_L = *0*N.m) at time *t=0.8*s afterwards the load torque inversed (T_L = *-11*N.m) at time *t=1.3*s.

It is important to note that both control approaches ensure good decoupling between stator flux linkage and torque. The speed response is merged with the reference one and the flux is very similar to the nominal case.

Referring to figure 8, it appears that the capacitor voltages given by v_{c1}, v_{c2}, v_{c3} and v_{c4} are deviating from their reference voltage value ($v_{dc}/4$). This result shows the problem of the unbalance capacitor voltages and its consequence on electromagnetic torque harmonics.

As expected in figure 9, the proposed solution is very efficient to solve the above-mentioned instability problem. As result, each capacitor voltage merged with its reference voltage value. Consequently, the torque ripple decreases considerably using the proposed balancing strategy.

It is clear that the five-level DTC with balancing strategy compared to the five-level DTC without balancing strategy has many advantages with regard to the stability of the capacitor voltages and torque ripple.
From the stator flux response, it is appreciated that the flux ripple decreases when the proposed balancing strategy is in use.

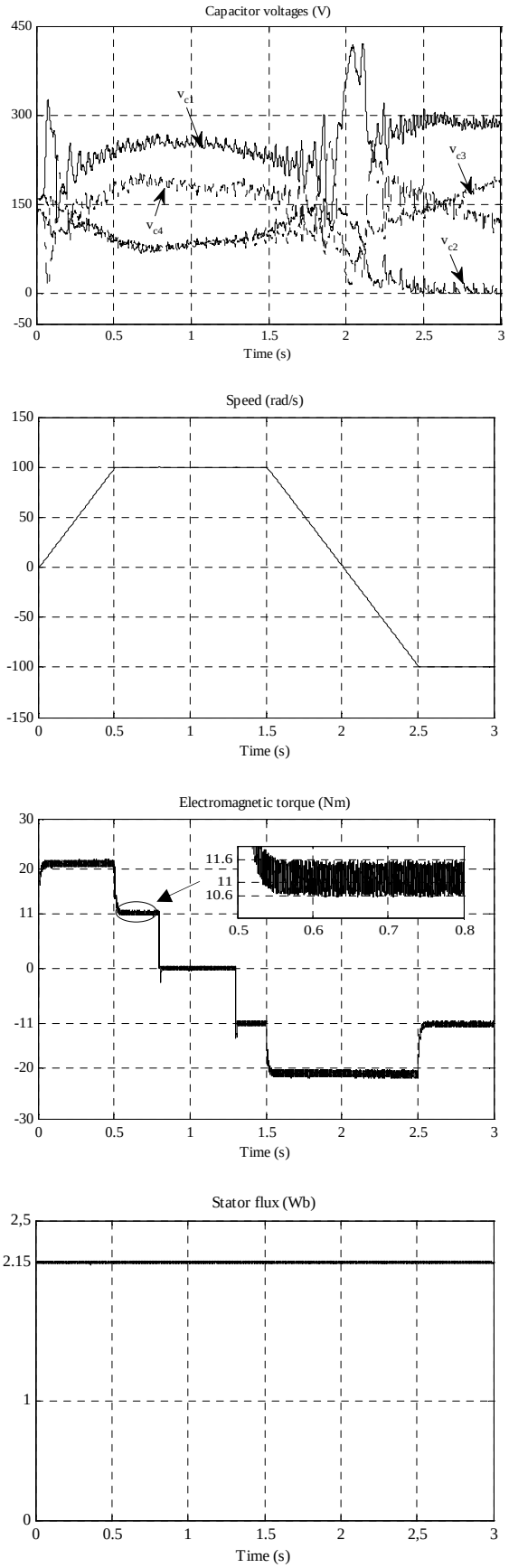

Fig. 8. Dynamic responses of five-level DTC without balancing strategy.

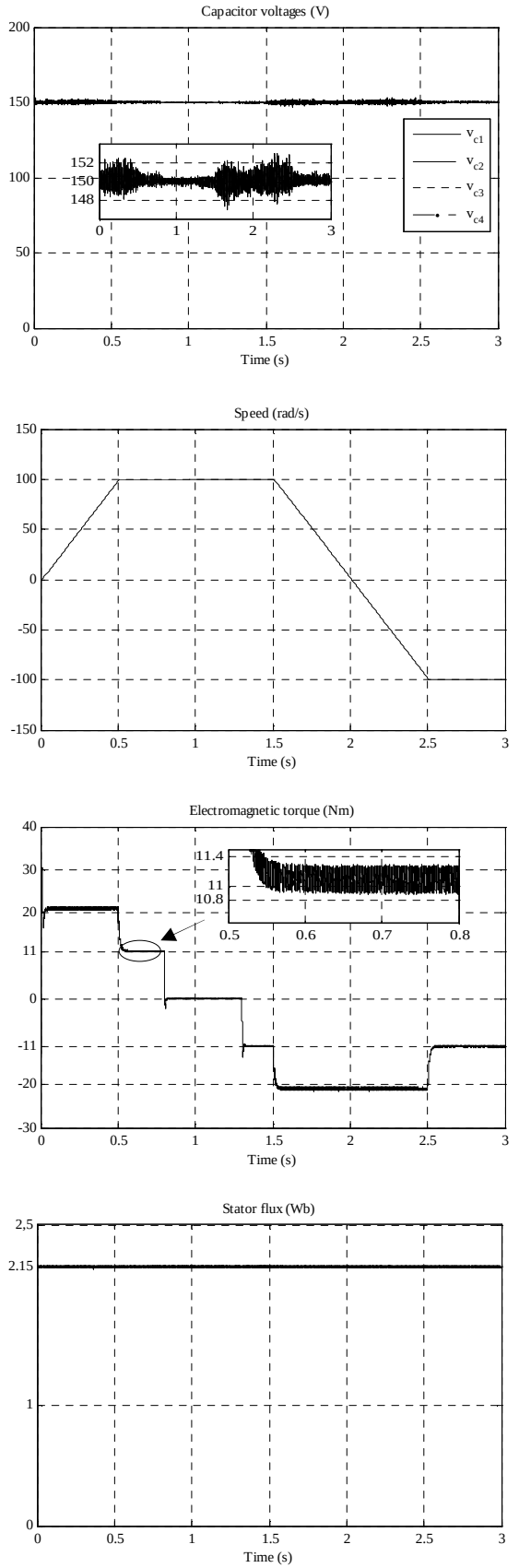

Fig. 9. Dynamic responses of five-level DTC with balancing strategy.

VIII. CONCLUSION

The major problem with the five-level DCI topology is the problem of voltage imbalance in DC capacitors. An arrangement for balancing the capacitor voltages was presented. The authors have suggested a method to balance the voltage across of the DC link capacitors. In this paper, a multilevel DTC method applied on DSSM fed by two five-level inverters is presented and its merits over the conventional DTC approach are confirmed by simulation results. The study is focused on the balancing problem of the input voltages of five-level DCI using a DTC endowed by a balancing strategy. The simulation results conclude that the proposed DTC is able to carry out the voltage-balancing task with no requirement for additional auxiliary power circuitry. Clearly, the balancing of the input DC voltages of the multilevel DCI is necessary to improve the performances of the DSSM fed by the two five-level DCI. Simulation results prove that the proposed method is suitable to a five-level DTC drive based on diode-clamped inverter.

Appendix 1. List of principal symbols

v_{1a}, v_{1b}, v_{1c} : Stator voltages of the first winding.
v_{2a}, v_{2b}, v_{2c} : Stator voltages of the second winding.
v_α,v_β : α-β axis stator voltages.
v_d ,v_q : *d*-*q* axis stator voltages.
v_s : Stator voltage vector.
i_{1a}, i_{1b}, i_{1c} : Stator currents of the first winding.
i_{2a}, i_{2b}, i_{2c} : Stator currents of the second winding.
i_α,i_β : α-β axis stator currents.
i_d ,i_q : *d*-*q* axis stator currents.
i_s : Stator current vector.
ϕ_{1a}, ϕ_{1b}, ϕ_{1c} : Stator flux of the first winding.
ϕ_{2a}, ϕ_{2b}, ϕ_{2c} : Stator flux of the second winding.
ϕ_α,ϕ_β : α-β axis stator fluxes.
ϕ_d ,ϕ_q : *d*-*q* axis stator fluxes.
ϕ_s : Stator flux vector.
v_f ,i_f : DC voltage and current of rotor excitation.
ϕ_f : Flux of rotor excitation.
T_{em} ,T_L : Electromagnetic and load torque.
Ω : Rotor speed.
ω : Rotating speed of rotor flux linkage.
Φ : Output of the stator flux hysteresis comparator.
τ : Output of the torque hysteresis comparator.
$\hat{\theta}_s$: Angular position.
$\gamma = \pi/6$: Angle between first stator and second stator.
R : Stator resistance.
R_f : Rotor resistance.
L_d , L_q : *d*-*q* stator inductance.
L_f : *d* axis Rotor inductance.
p : Pole pair number.
J : Moment inertia.
f_r : Friction coefficient.
M_{fd} : Mutual inductance between *d* axis for each stator and rotor.

Appendix 2. DSSM parameters

p_n=5 kW, v_n=232V, p=1, R=2.35 Ω, R_f=30.3Ω, L_d=0.3811H, L_q=0.211H, L_f=15H, M_{fd}=2.146H, J=0.05Nms2/rad, f_r=0.001Nms/rad, i_f=1A.

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