PHOTOVOLTAIC BASED NEW MULTILEVEL INVERTER TOPOLOGY WITH MINIMUM NUMBER OF SWITCHING COMPONENTS

M. Anitha[1], P. Somasundaram[2] , V. Thiyagarajan[3]
[1]Research Scholar, Department of EEE, CEG, Anna University, Chennai, Tamilnadu, India.
[2]Associate Professor, Department of EEE, CEG, Anna University, Chennai, Tamilnadu, India.
[3]Assistant Professor, Department of EEE, SSN College of Engineering, Kalavakkam, Tamilnadu, India.
Email: aamizh@yahoo.com

Abstract: *Multilevel inverter (MLI) plays a strong role in low power photovoltaic (PV) applications to transfer large amount of high quality power. It offers less distortion and can be used in high power, medium voltage applications. The objective of this paper is to propose a photovoltaic based new multilevel inverter topology with reduced number of switches and voltage sources. The proposed inverter consists of two units namely basic unit which produces unidirectional output voltage and polarity changing unit which helps to change the polarity of the output voltage. The basic unit of the proposed inverter topology produces five level output voltage waveform during symmetric operation and nine level output voltage waveform during asymmetric operation. This topology can be extended with multiple dc sources to synthesize large output levels. The advantage of this topology is it uses minimum number of components and hence the cost and size of the inverter is reduced. In this paper, the dc source for the proposed inverter topology is modelled as a PV array. A mathematical model for the PV array is developed and implemented with the proposed multilevel inverter topology. The proposed inverter is simulated using MATLAB/Simulink software. The simulation results for different output levels are analysed and presented.*

Key words: *Multilevel inverter, Symmetric, Asymmetric, THD, Photovoltaic.*

1. Introduction

Multilevel inverters were introduced in 1975 by Baker Richard H and Bannister Lawrence H, in their work titled Electric Power Converter [1]. It has attracted great attention of modern day researchers. The multilevel inverters are classified into two groups, namely, symmetric multilevel inverter, where the magnitude of all dc voltage sources is same and asymmetric multilevel inverter, where the magnitude of all dc voltage sources is different [2]. Renewable energy resources, capacitors or batteries are mostly used as the dc voltage sources. Multilevel inverters has various advantages such as low distortion, high power quality, minimum peak inverse voltage (PIV), staircase output voltage, low dv/dt stress, smaller common mode voltage and minimum switching losses[2-5]. However, it requires larger number of power semiconductor switches and associated gate driver circuits to achieve higher number of output levels [6]. At first the multilevel inverter was started with three-level and then several topologies of higher level inverter have been developed in recent years [7]. The most popular topologies of multilevel inverters are diode-clamped [8], flying capacitor [9] and cascaded H-bridge inverters [10]. In diode clamped MLI with the help of clamping diodes, the DC bus voltage is clamped to half of its levels. In flying capacitor MLI, the device voltage is clamped to the level of one capacitor voltage with the help of independent capacitors. In both DCMLI and FCMLI, voltage imbalance is a major problem. In order to overcome these limitations, cascade MLI topology was introduced. The main advantages of multilevel inverter is its low total harmonic distortion (THD) which is mainly due to closely sinusoidal output voltage waveforms produced by multilevel inverter. Nowadays, many researchers have proposed modified pulse width modulation (PWM) techniques and new inverter topology.

An improved configuration for cascaded MLI topology is proposed in [14]. In this topology, each modules can synthesize a maximum of 9-level output voltage waveform with a reduced power number of power components. Ref. [15] presents a hybrid cascaded MLI topology which is formed by the combination of symmetrical 4-level sub module and a full bridge unit. A new single phase cascaded MLI topology based on novel H-bridge units is proposed in [16]. The basic unit consists of six power switches and two dc sources which is able to generate seven levels at the output. The main disadvantage of the proposed basic unit over the H-bridge is it requires higher number of voltage sources and power switches. In [18], a combination of CHB MLI with a double level circuit is presented. In this, a half bridge inverter is combined with a CHB MLI to increase the output voltage level to nearly twice that of a conventional CHB MLI. Another inverter topology with minimum switches is proposed in [22]. This topology generates a larger numbers of output voltage levels with reduced number of switches. Photovoltaic (PV) energy becomes a most potential, pollution free energy

resource in India. In this paper, the dc source for the proposed inverter topology is modelled as a photovoltaic array.

This paper proposes a new photovoltaic source based multilevel inverter with reduced number of switches. The proposed multilevel inverter uses two voltage sources, four main switches and two diodes. Section II presents the model of PV array. Section III explains the operation of the proposed multilevel inverter topology. The generalised structure of the proposed inverter topology and its magnitude determination are discussed in Section IV. The comparison study between the proposed inverter topology with conventional and other presented topologies are shown in Section V. The modulation strategy for the proposed inverter is presented in Section VI. The simulation results obtained using MATLAB/Simulink are presented in Section-VII and the conclusions were presented in Section-VIII.

2. PV Array Model

A photovoltaic cell is basically a P-N semiconductor junction diode which converts solar energy into electrical energy. A several series connected photovoltaic cells form a photovoltaic module and a several PV modules are modules connected in series and parallel to form a PV array. The series combination of PV modules determines the output voltage whereas the parallel combination defines the maximum output current drawn from the array. A simple solar cell model is shown in Fig. 1 where the solar cell is modeled as a current source in parallel with a diode, a series resistor (R_S) and a shunt resistor (R_P) [11-13]. The value of series resistor is small when compared with shunt resistor. By Kirchhoff's Current Law (KCL), we get

$$I_S = I_D + \frac{V_D}{R_p} + I_{PV} \qquad (1)$$

Where, I_S is the isolation current, I_{PV} is the solar cell current, I_D is the current in the bypass diode and V_{PV} is the voltage across solar cell.

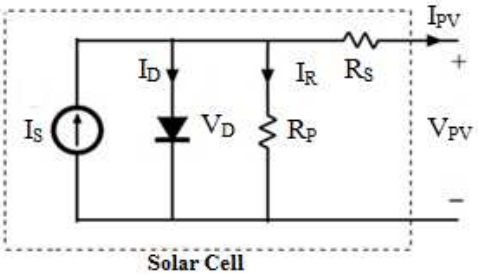


Fig. 1. Equivalent circuit of a solar cell

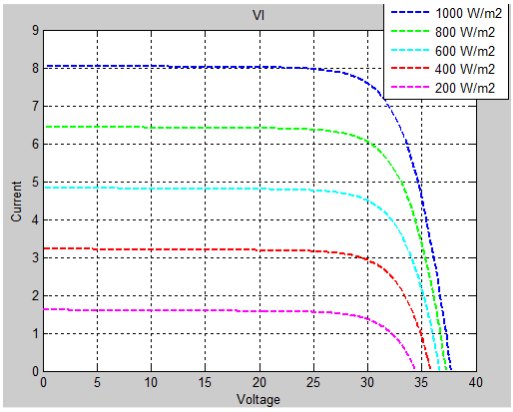
The characteristics equation of bypass diode across the PV module is given by the equation,

$$I_D = I_O(e^{V_D/V_T} - 1) \qquad (2)$$

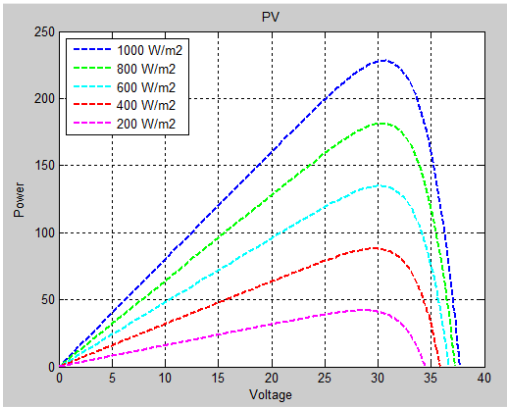
Where, I_O is the reverse saturation current and V_T is the thermal voltage. Since, the photovoltaic array is made up of several solar cells connected in series, the current in each of the series solar array is given by the equation,

$$I_S = I_o\left(e^{V_D/n_s V_T} - 1\right) + \frac{V_{PV} + R_S I_{PV}}{R_P} + I_{PV} \qquad (3)$$

Where, n_S is the number of solar cells in series.



(a)



(b)

Fig. 2. Solar cell (a) VI characteristics (b) PV characteristics

The voltage-current and power-voltage characteristics of the typical single diode solar cell for different isolation is shown in Fig. 2. Due to the variation in the solar irradiation, the photovoltaic array exhibits non-linear power-voltage (PV) and voltage-current (VI) characteristics.

3. Proposed Multilevel Inverter

The basic unit of the proposed multilevel inverter is shown in Fig. 3 (a). It consists of two voltage sources, four main switches and two diodes. The proposed inverter can produce 5-level output voltage during symmetrical case and 9-level output voltage during asymmetrical case of operation. In order to obtain the bidirectional output voltages, a polarity

changer is used. Here, the full bridge inverter is acted as a polarity changer. The overall diagram of the proposed inverter with polarity changing unit is shown in Fig. 3(b).

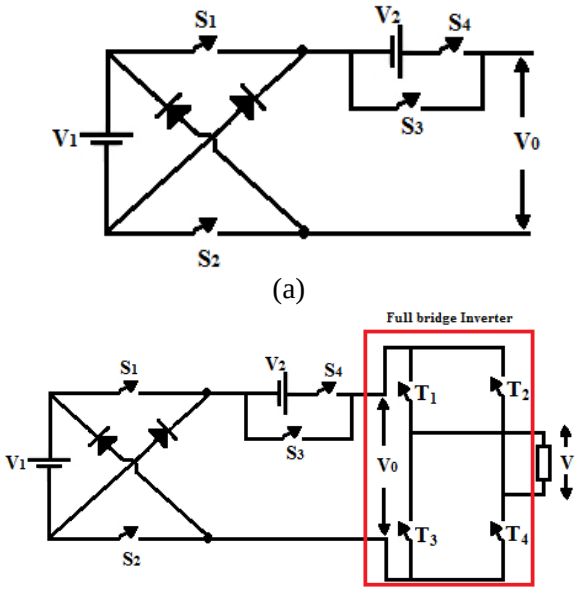
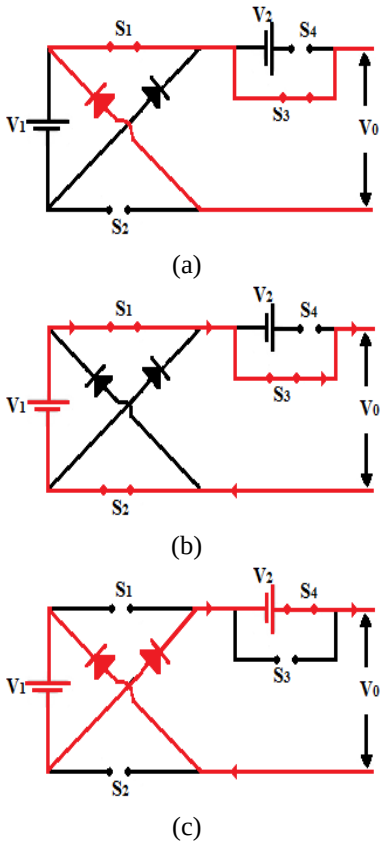


Fig. 3. Proposed Multilevel Inverter (a) basic circuit (b) with H-bridge

The different modes of operation of the proposed inverter is shown in Fig. 4.



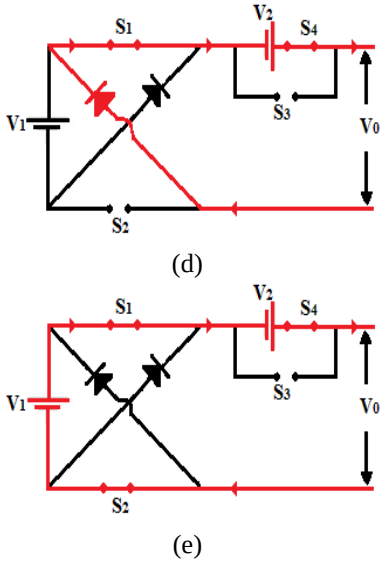


Fig.4. Modes of operation (a) Mode - 0 (b) Mode - 1 (c) Mode - 2 (d) Mode - 3 and (e) Mode - 4

In mode-0, the switches S_1 and S_3 are ON and the other switches are OFF and hence, zero voltage is obtained. In mode-1, the switches S_1, S_2 and S_3 are ON and the switch S_4 is OFF and the obtained voltage is V_1. The reverse operation is done in mode-2. In mode-2, the switches S_1, S_2 and S_3 are OFF and the switch S_4 is ON and the obtained voltage is V_2-V_1. During mode-3, the voltage V_2 is obtained with the switches S_1 and S_4 are ON and the switches S_2 and S_3 are OFF. During mode-5, the switch S_3 is OFF and the other switches are ON and hence, the voltage is V_2 -V_1 obtained.

4. Generalised multilevel inverter topology

The generalised topology of proposed multilevel inverter with 'n' voltage sources and 'k' switches is shown in Fig.5. The total output voltage of the generalised topology of proposed inverter is given by,

$$V_o = \sum_{i=1}^{n} V_i \qquad (4)$$

Since the basic unit consists of 'k' switches, the total number of switches (N_{switch}) in the proposed multilevel inverter with polarity changing circuit is given by,

$$N_{switch} = k + 4 \qquad (5)$$

The relation between the number of dc voltage sources and the number of switches is given by,

$$N_{switch} = 2(n + 2) \qquad (6)$$

The number of output levels in the output voltage depends on the number of voltage sources and its corresponding magnitude. Therefore, the magnitude

of voltage sources has to be chosen differently to achieve greater number of output levels.

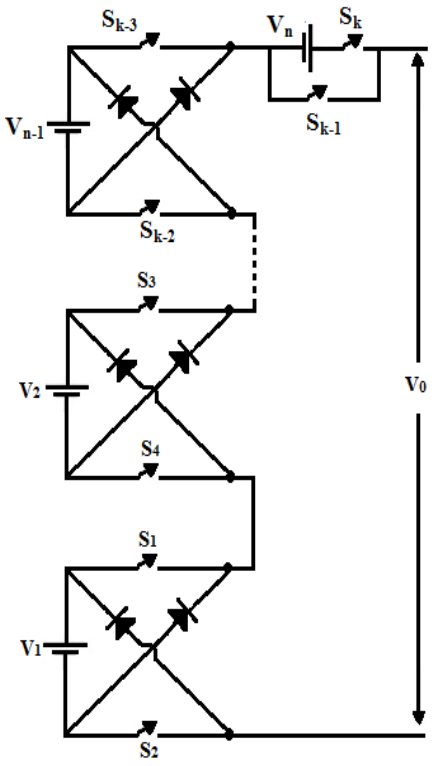


Fig. 5. Generalised inverter topology.

The different algorithms to determine the magnitude of each voltage sources are explained as follows:

Algorithm-1

Here, the magnitude of all voltage sources is equal to V_{dc}. Therefore, the total number of levels 'm' in the output voltage is given by,

$$m = 2n + 1 \qquad (7)$$

From equ. (6) and (7), the relation between the total number of levels 'm' and the number of switches ' N_{switch}' is obtained as

$$N_{switch} = m + 3 \qquad (8)$$

Algorithm-2

Here, the magnitude of each voltage source is different and are given by,

$$V_i = iV_{dc} \qquad (9)$$

where, i=1, 2, 3...n.

The number of voltage levels achieved is given by,

$$m = n^2 + n + 1 \qquad (10)$$

Algorithm-3

Here, the magnitude of each voltage source is given by,

$$V_i = \left(2^{i-1}\right)V_{dc} \qquad (11)$$

where, i=1, 2, 3...n.

The number of voltage levels achieved is given by,

$$m = 2^{n+1} - 1 \qquad (12)$$

Algorithm-4

Here, the magnitude of each voltage source is given by,

$$V_i = \left(3^{i-1}\right)V_{dc} \qquad (13)$$

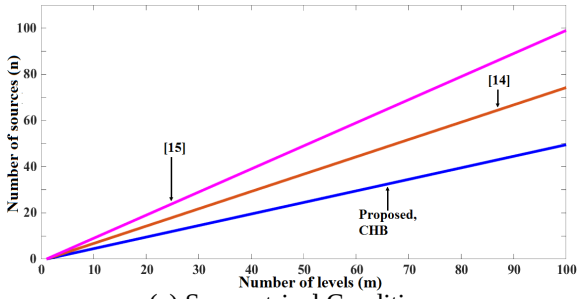
where, i=1, 2, 3...n.

The number of voltage levels achieved is given by,

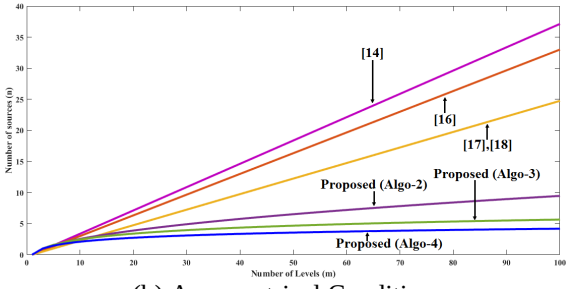
$$m = 3^n \qquad (14)$$

5. Comparison Study

This section presents the comparison study based on the number of voltage sources and number of switches required to synthesize the necessary output voltage levels of the proposed inverter topology with CHB and other existing topologies. The comparison of the number of levels versus number of voltage sources during symmetrical and asymmetrical condition are shown in Fig. 6(a) and Fig. 6(b) respectively. It is observed that the proposed inverter topology requires less number voltage sources to synthesize required output levels during both symmetric and asymmetric conditions.



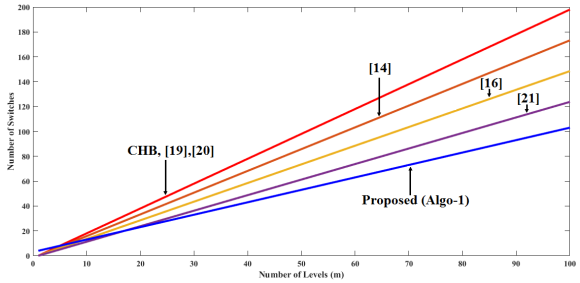
(a) Symmetrical Condition



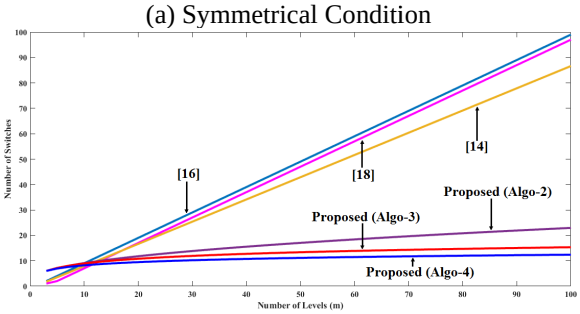
(b) Asymmetrical Condition

Fig. 6. Levels vs Sources

Fig. 7. (a) and (b) shows the comparison between the number of levels and switches during symmetrical and asymmetrical conditions, respectively. It is seen that the proposed inverter topology synthesize higher output levels with minimum number of switches as compared with CHB inverter and other presented topologies.



(a) Symmetrical Condition



(b) Asymmetrical Condition

Fig. 7. Level vs Switches

6. Multi-Carrier Modulation Strategies

According to the switching frequency, the modulation techniques for multilevel inverter are divided into two categories (a) low-frequency modulation (LFM) techniques and (b) pulse-width modulation (PWM) techniques. In the present work, LFM technique is used, because it is more flexible, easy to implement and drastically reduce switching losses. In this strategy, the switching pulses are generated by comparing the constant carrier signals with the reference sinusoidal signal. Here, $\left(\frac{m-1}{2}\right)$ constant amplitude carrier signals are compared with the sinusoidal reference waveform. The amplitudes of the different carrier signals are determined using the following expression [22],

$$V_{Ci} = V_{\max}\left(\frac{2i-1}{m-1}\right) \quad i = 1,2,3.....,\left(\frac{m-1}{2}\right) \qquad (15)$$

where V_{max} is the maximum voltage of the reference sinusoidal signal.

The generation of switching pulses for 9-level inverter is shown in Fig. 8.

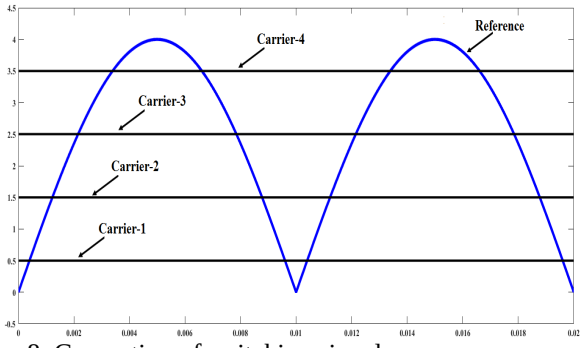


Fig. 8. Generation of switching signals.

7. Simulation Results

The simulation results of the proposed multilevel inverter are presented in this section. The proposed inverter produces unidirectional output voltages and hence, a polarity changing unit is used to obtain the bidirectional output voltage across the load. For simulation of proposed inverter topology, a photovoltaic array is used as input dc source.

A. Symmetrical - 5-level

Fig. 9. shows the basic unit of the proposed inverter topology consists of two voltage sources V_1 and V_2.

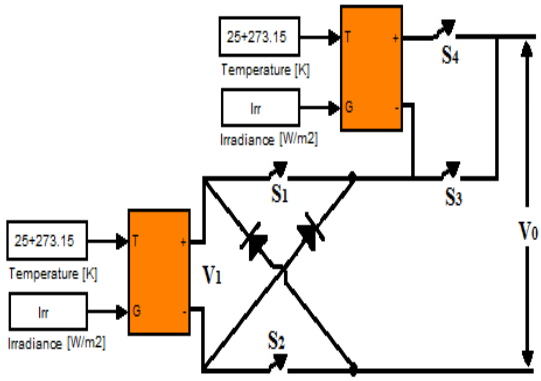
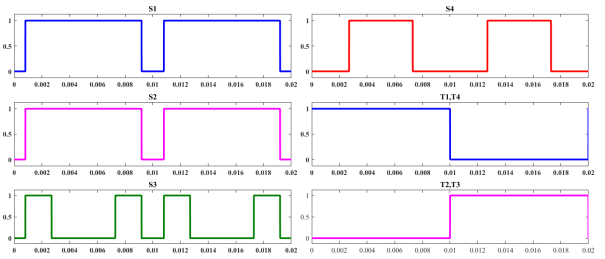


Fig. 9. Proposed inverter with two voltage sources.

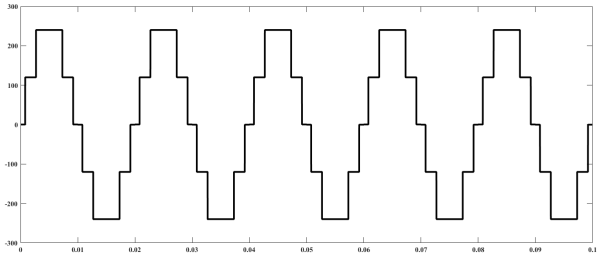
In this case, the values of the dc voltage sources are $V_1 = V_2 = V_{dc} = 120$ V and hence, the maximum voltage obtained as 240 V (i.e., $V_1 + V_2$). This case is called as symmetrical since the dc voltage sources has same magnitude. This topology generate 5-level output voltage. The level-1 voltage as 120 V is obtained during mode-1 operation and level-2 voltage as 240 V is obtained during mode-4 operation of the inverter. The negative voltage values are obtained with the help of polarity changer. The switching states for symmetrical 5-level inverter is given in Table I and the corresponding switching pulses are shown in Fig. 10(a).

TABLE I
SWITCHING STATES FOR SYMMETRIC 5-LEVEL

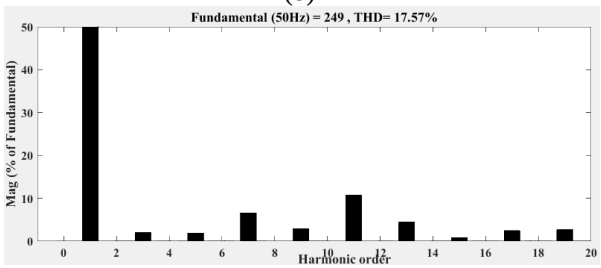
Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	T_1,T_2	T_3,T_4
V_{dc}	S_1,S_2,S_3,T_1,T_4	S_1,S_2,S_3,T_2,T_3
$2V_{dc}$	S_1,S_2,S_4,T_1,T_4	S_1,S_2,S_4,T_2,T_3



(a)



(b)



(c)

Fig. 10. 5-level (a) Switching pulse (b) Output Voltage and (c) THD.

TABLE II
DETAILS OF LOAD VARIATION STUDY FOR 5-LEVEL

S.No	Load (R-L)	Power factor	Load Voltage THD (%)	Load Current THD (%)
1	50mH	0	17.57	6.31
2	10Ω, 55mH	0.5	17.57	10.72
3	30Ω, 71.5mH	0.8	17.57	11.90
4	100 Ω	1	17.57	17.57

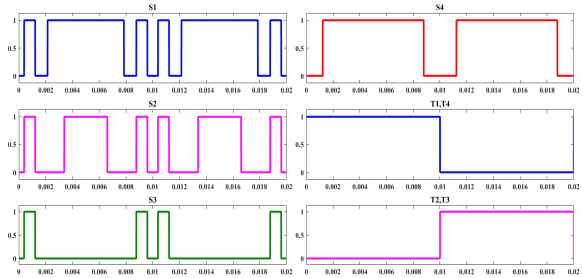
The 5-level output voltage obtained across the load is shown in Fig. 10(b) and its THD result is shown in Fig. 10(c). It is observed that the THD of the 5-level output voltage waveform is obtained as 17.57%. The THD of the load voltage and load current waveform for various loads are given in Table II.

B. Asymmetrical - 9-level

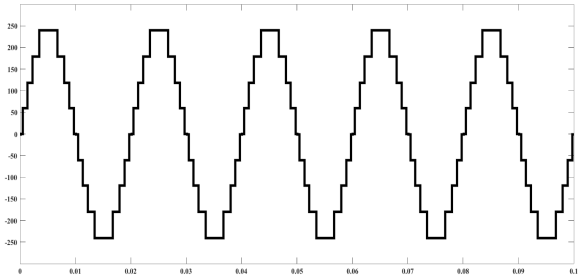
Fig. 9. shows the basic unit of the proposed inverter topology consists of two voltage sources V_1 and V_2. In this case, the values of the dc voltage sources are $V_1 = V_{dc} = 60$ V and $V_2 = 3V_{dc} = 180$ V and the maximum voltage obtained as 240V (i.e., V_1+V_2). This topology generates 9-level output voltage. This case is called as asymmetrical since the dc voltage sources has different magnitude. The switching states for asymmetrical case of the proposed multilevel inverter is given in Table III. The switching pulses, output voltage and THD for asymmetrical-9-level output voltage are shown in Fig. 11. It is observed that the THD of the 9-level output voltage waveform is obtained as 9.38%. The THD of the load voltage and load current waveform for various loads are given in Table IV.

TABLE III
SWITCHING STATES FOR ASYMMETRIC 9-LEVEL

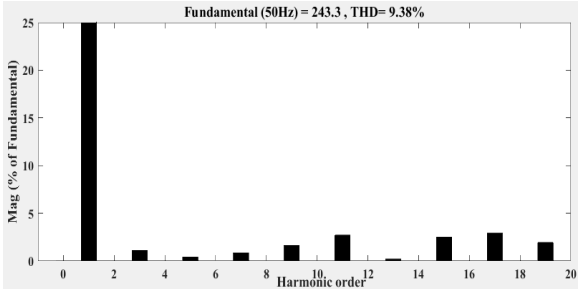
Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	T_1,T_2	T_3,T_4
V_{dc}	S_1,S_2,S_3,T_1,T_4	S_1,S_2,S_3,T_2,T_3
$2V_{dc}$	S_4,T_1,T_4	S_4,T_2,T_3
$3V_{dc}$	S_1,S_4,T_1,T_4	S_1,S_4,T_2,T_3
$4V_{dc}$	S_1,S_2,S_4,T_1,T_4	S_1,S_2,S_4,T_2,T_3



(a)



(b)



(c)

Fig. 11. 9- level (a) Switching pulse (b) Output Voltage and (c) THD.

TABLE IV

DETAILS OF LOAD VARIATION STUDY FOR 9-LEVEL

S.No	Load (R-L)	Power factor	Load Voltage THD (%)	Load Current THD (%)
1	50mH	0	9.38	5.48
2	10Ω, 55mH	0.5	9.38	8.61
3	30Ω, 71.5mH	0.8	9.38	9.09
4	100 Ω	1	9.38	9.38

C. Asymmetrical - 27-level

Fig. 12. shows the basic unit of the proposed inverter topology consists of three voltage sources V_1,$V_2$and V_3. In this case, the magnitude of the dc voltage sources are chosen as $V_1 = V_{dc} = 18V$, $V_2 = 3V_{dc} = 54V$ and $V_3 = 9V_{dc} = 162V$. This topology generates 27-level output voltage and the maximum voltage obtained across the load as 234V (i.e., $V_1+V_2+V_3$). The switching states for this case is given in Table V and the corresponding switching pulses are shown in Fig. 13(a). The 27-level output voltage obtained across the load is shown in Fig. 13(b) and its THD result is shown in Fig. 13(c). It is observed that the THD of the 27-level output voltage waveform is obtained as 3.18%. The THD of the load voltage and load current waveform for various loads are given in Table VI.

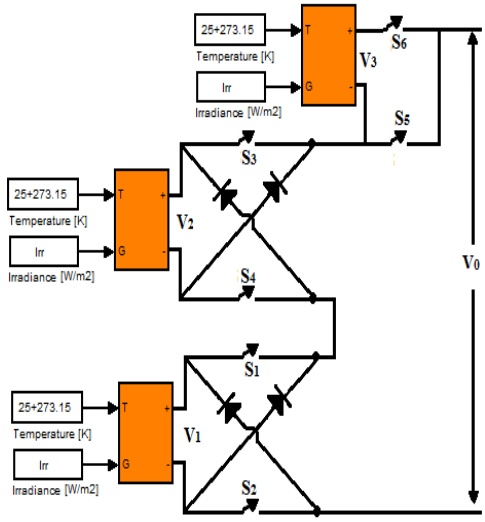
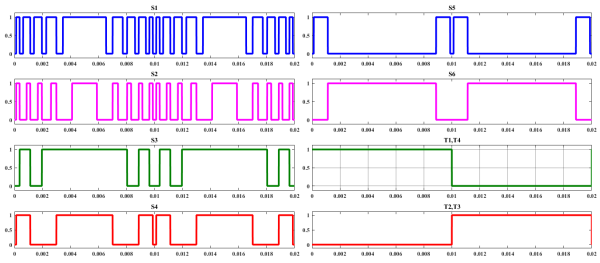


Fig.12. Proposed inverter with three voltage sources.

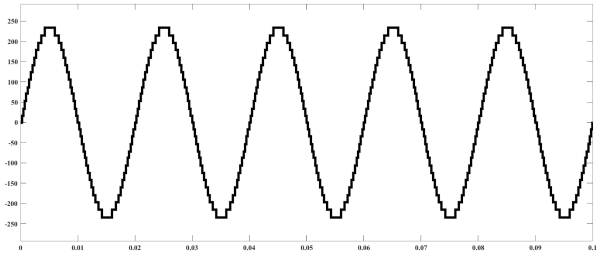
TABLE V

SWITCHING STATES FOR ASYMMETRIC 27-LEVEL

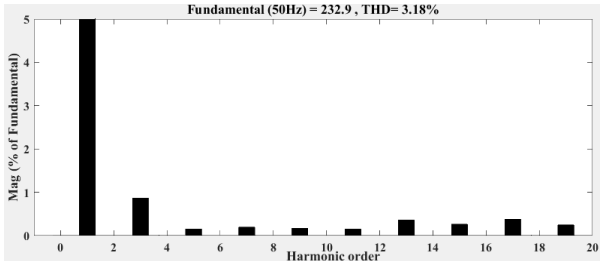
Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	T_1,T_2	T_3,T_4
V_{dc}	S_1,S_2,S_4,S_5,T_1,T_4	S_1,S_2,S_4,S_5,T_2,T_3
$2V_{dc}$	S_3,S_4,S_5,T_1,T_4	S_3,S_4,S_5,T_2,T_3
$3V_{dc}$	S_1,S_3,S_4,S_5,T_1,T_4	S_1,S_3,S_4,S_5,T_2,T_3
$4V_{dc}$	$S_1,S_2,S_3,S_4,S_5,T_1,T_4$	$S_1,S_2,S_3,S_4,S_5,T_2,T_3$
$5V_{dc}$	S_6,T_1,T_4	S_6,T_2,T_3
$6V_{dc}$	S_1,S_6,T_1,T_4	S_1,S_6,T_2,T_3
$7V_{dc}$	S_1,S_2,S_6,T_1,T_4	S_1,S_2,S_6,T_2,T_3
$8V_{dc}$	S_3,S_6,T_1,T_4	S_3,S_6,T_2,T_3
$9V_{dc}$	S_1,S_3,S_6,T_1,T_4	S_1,S_3,S_6,T_2,T_3
$10V_{dc}$	S_1,S_2,S_3,S_6,T_1,T_4	S_1,S_2,S_3,S_6,T_2,T_3
$11V_{dc}$	S_3,S_4,S_6,T_1,T_4	S_3,S_4,S_6,T_2,T_3
$12V_{dc}$	S_1,S_3,S_4,S_6,T_1,T_4	S_1,S_3,S_4,S_6,T_2,T_3
$13V_{dc}$	$S_1,S_2,S_3,S_4,S_6,T_1,T_4$	$S_1,S_2,S_3,S_4,S_6,T_2,T_3$



(a)



(b)



(c)

Fig. 13. 27-level (a) Switching pulse (b) Output Voltage and (c) THD.

TABLE VI

DETAILS OF LOAD VARIATION STUDY FOR 27-LEVEL

S.No	Load (R-L)	Power factor	Load Voltage THD (%)	Load Current THD (%)
1	50mH	0	3.18	1.15
2	10Ω, 55mH	0.5	3.18	2.43
3	30Ω, 71.5mH	0.8	3.18	2.89
4	100 Ω	1	3.18	3.18

D. Asymmetrical - 81-level

Fig. 14. shows the basic unit of the proposed inverter topology consists of four voltage sources V_1,V_2,V_3 and V_4. Here, the magnitude of the dc voltage sources are chosen as $V_1 = V_{dc} = 6V$, $V_2 = 3V_{dc} = 18V$, $V_3 = 9V_{dc} = 54V$ and $V_4 = 27V_{dc} = 162V$. This topology generates 81-level output voltage and the maximum voltage obtained across the load is 240V (i.e., $V_1+V_2+V_3+V_4$). The switching states for asymmetrical 81-level inverter is given in Table VII and the corresponding switching pulses are shown in Fig. 15(a). The 81-level output voltage obtained across the load is shown in Fig. 15(b) and its THD result is shown in Fig. 15(c). It is observed that the THD of the 81-level output voltage waveform is obtained as 1.43%. The THD of the load voltage and load current waveform for various loads are given in Table VIII.

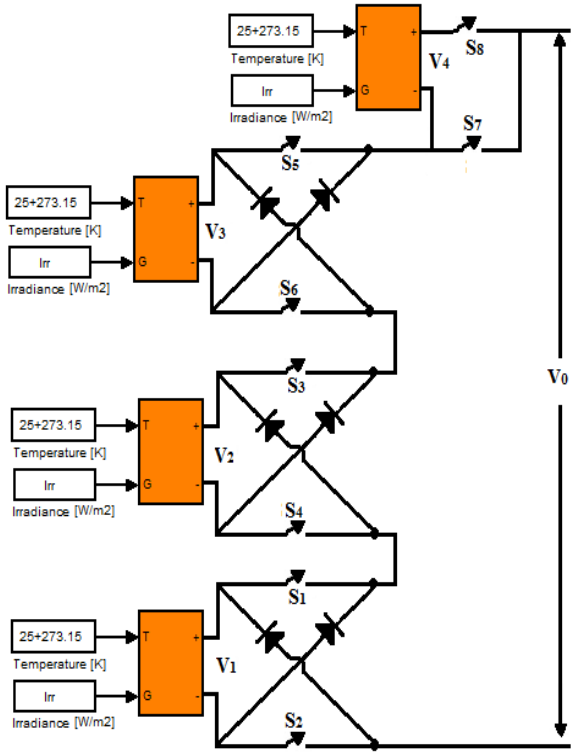
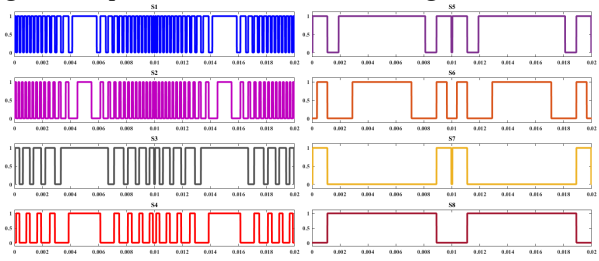
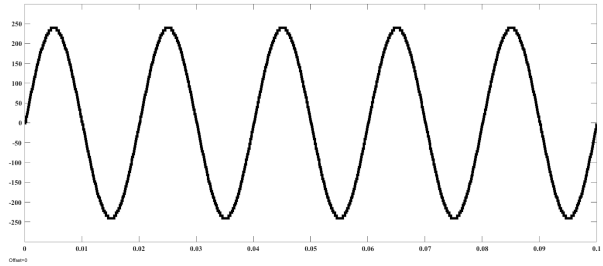


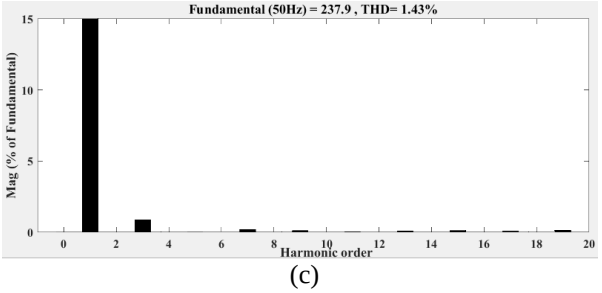
Fig. 14. Proposed inverter with four voltage sources.



(a)



(b)



(c)

Fig. 15. 81-level (a) Switching pulse (b) Output Voltage and (c) THD.

TABLE VIII

DETAILS OF LOAD VARIATION STUDY

S.No	Load (R-L)	Power factor	Load Voltage THD (%)	Load Current THD (%)
1	50mH	0	1.43	0.94
2	10Ω, 55mH	0.5	1.43	1.07
3	30Ω, 71.5mH	0.8	1.43	1.15
4	100 Ω	1	1.43	1.43

TABLE VII

SWITCHING STATES FOR ASYMMETRIC 81-LEVEL

Output Voltage	On-State Switches		Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle		Positive Cycle	Negative Cycle
0	T_1,T_2	T_3,T_4	0	T_1,T_2	T_3,T_4
V_{dc}	$S_1,S_2,S_3,S_5,S_7,T_1,T_4$	$S_1,S_2,S_3,S_5,S_7,T_2,T_3$	$21V_{dc}$	S_1,S_3,S_4,S_8,T_1,T_4	S_1,S_3,S_4,S_8,T_2,T_3
$2V_{dc}$	S_3,S_4,S_5,S_7,T_1,T_4	S_3,S_4,S_5,S_7,T_2,T_3	$22V_{dc}$	$S_1,S_2,S_3,S_4,S_8,T_1,T_4$	$S_1,S_2,S_3,S_4,S_8,T_2,T_3$
$3V_{dc}$	$S_1,S_3,S_4,S_5,S_7,T_1,T_4$	$S_1,S_3,S_4,S_5,S_7,T_2,T_3$	$23V_{dc}$	S_5,S_8,T_1,T_4	S_5,S_8,T_2,T_3
$4V_{dc}$	$S_1,S_2,S_3,S_4,S_5,S_7,T_1,T_4$	$S_1,S_2,S_3,S_4,S_5,S_7,T_2,T_3$	$24V_{dc}$	S_1,S_5,S_8,T_1,T_4	S_1,S_5,S_8,T_2,T_3
$5V_{dc}$	S_5,S_6,S_7,T_1,T_4	S_5,S_6,S_7,T_2,T_3	$25V_{dc}$	S_1,S_2,S_5,S_8,T_1,T_4	S_1,S_2,S_5,S_8,T_2,T_3
$6V_{dc}$	S_1,S_5,S_6,S_7,T_1,T_4	S_1,S_5,S_6,S_7,T_2,T_3	$26V_{dc}$	S_3,S_5,S_8,T_1,T_4	S_3,S_5,S_8,T_2,T_3
$7V_{dc}$	$S_1,S_2,S_5,S_6,S_7,T_1,T_4$	$S_1,S_2,S_5,S_6,S_7,T_2,T_3$	$27V_{dc}$	S_1,S_3,S_5,S_8,T_1,T_4	S_1,S_3,S_5,S_8,T_2,T_3
$8V_{dc}$	S_3,S_5,S_6,S_7,T_1,T_4	S_3,S_5,S_6,S_7,T_2,T_3	$28V_{dc}$	$S_1,S_2,S_3,S_5,S_8,T_1,T_4$	$S_1,S_2,S_3,S_5,S_8,T_2,T_3$
$9V_{dc}$	$S_1,S_3,S_5,S_6,S_7,T_1,T_4$	$S_1,S_3,S_5,S_6,S_7,T_2,T_3$	$29V_{dc}$	S_3,S_4,S_5,S_8,T_1,T_4	S_3,S_4,S_5,S_8,T_2,T_3
$10V_{dc}$	$S_1,S_2,S_3,S_5,S_6,S_7,T_1,T_4$	$S_1,S_2,S_3,S_5,S_6,S_7,T_2,T_3$	$30V_{dc}$	$S_1,S_3,S_4,S_5,S_8,T_1,T_4$	$S_1,S_3,S_4,S_5,S_8,T_2,T_3$
$11V_{dc}$	$S_3,S_4,S_5,S_6,S_7,T_1,T_4$	$S_3,S_4,S_5,S_6,S_7,T_2,T_3$	$31V_{dc}$	$S_1,S_2,S_3,S_4,S_5,S_8,T_1,T_4$	$S_1,S_2,S_3,S_4,S_5,S_8,T_2,T_3$
$12V_{dc}$	$S_1,S_3,S_4,S_5,S_6,S_7,T_1,T_4$	$S_1,S_3,S_4,S_5,S_6,S_7,T_2,T_3$	$32V_{dc}$	S_5,S_6,S_8,T_1,T_4	S_5,S_6,S_8,T_2,T_3
$13V_{dc}$	$S_1,S_2,S_3,S_4,S_5,S_6,S_7,T_1,T_4$	$S_1,S_2,S_3,S_4,S_5,S_6,S_7,T_2,T_3$	$33V_{dc}$	S_1,S_5,S_6,S_8,T_1,T_4	S_1,S_5,S_6,S_8,T_2,T_3
$14V_{dc}$	S_8,T_1,T_4	S_8,T_2,T_3	$34V_{dc}$	$S_1,S_2,S_5,S_6,S_8,T_1,T_4$	$S_1,S_2,S_5,S_6,S_8,T_2,T_3$
$15V_{dc}$	S_1,S_8,T_1,T_4	S_1,S_8,T_2,T_3	$35V_{dc}$	S_3,S_5,S_6,S_8,T_1,T_4	S_3,S_5,S_6,S_8,T_2,T_3
$16V_{dc}$	S_1,S_2,S_8,T_1,T_4	S_1,S_2,S_8,T_2,T_3	$36V_{dc}$	$S_1,S_3,S_5,S_6,S_8,T_1,T_4$	$S_1,S_3,S_5,S_6,S_8,T_2,T_3$
$17V_{dc}$	S_3,S_8,T_1,T_4	S_3,S_8,T_2,T_3	$37V_{dc}$	$S_1,S_2,S_3,S_5,S_6,S_8,T_1,T_4$	$S_1,S_2,S_3,S_5,S_6,S_8,T_2,T_3$
$18V_{dc}$	S_1,S_3,S_8,T_1,T_4	S_1,S_3,S_8,T_2,T_3	$38V_{dc}$	$S_3,S_4,S_5,S_6,S_8,T_1,T_4$	$S_3,S_4,S_5,S_6,S_8,T_2,T_3$
$19V_{dc}$	S_1,S_2,S_3,S_8,T_1,T_4	S_1,S_2,S_3,S_8,T_2,T_3	$39V_{dc}$	$S_1,S_3,S_4,S_5,S_6,S_8,T_1,T_4$	$S_1,S_3,S_4,S_5,S_6,S_8,T_2,T_3$
$20V_{dc}$	S_3,S_4,S_8,T_1,T_4	S_3,S_4,S_8,T_2,T_3	$40V_{dc}$	$S_1,S_2,S_3,S_4,S_5,S_6,S_8,T_1,T_4$	$S_1,S_2,S_3,S_4,S_5,S_6,S_8,T_2,T_3$

8. Conclusion

This paper proposed a photovoltaic based new symmetric and asymmetric type multilevel inverter topology. The main advantage of this inverter topology is it uses minimum switching components for larger levels as compared with other conventional topologies. The simulation results for both the symmetric and asymmetric modes of the proposed multilevel inverter are presented. The result shows that the output voltage waveform of proposed multilevel inverter achieves less %THD during both symmetric and asymmetric operation.

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