A Comprehensive Analysis of Carrier Shifting Algorithms for Diode-Clamped MLI Based Drive

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Abstract—**common mode voltage (CMV) and Circulating current (CC) minimization is one of the most important attentions in inverter fed drive. Diode-clamped multi-level inverter (MLI) enables higher output currents per phase, effectively increasing the power rating of the drive. Various switching operation in the inverter legs creates the better voltage profile and leads to the enabling of CMV and CC in the drive system. The induced CC flows between the apparatus neutral (N) to the supply ground (G) due to the existence of parasitic capacitance. This CC may cause potential danger especially when parasitic capacitance poses large. In the past, several conversion topologies and modulation techniques have been introduced with minimization of the circulation current. However, these techniques lead to complexity, high cost, low voltage profile and efficiency due to lower modulation parameters. This paper proposes PS, POD, PD carrier shifting PWM algorithms for diode clamped MLI to tumbling the circulating current within each phase of inverter legs. The performances of proposed algorithms, in terms of circulating current, total harmonic distortion, losses and efficiencies are analyzed theoretically. The theoretically analyses are validated via simulation and FPGA based experimental results.**

***Index Terms*—Common mode voltage, circulating current, pulse width modulation (PWM), phase shift, phase opposition disposition, phase disposition.**

I. INTRODUCTION

Inverters are using widely in different industrial applications for conditioning the power in adjustable speed drives and renewable energy system because of the capacity to control the amplitude and frequency of the output voltage [1],[2]. Now in order to minimize the harmonics in the inverters and output voltage and to reach the voltage rating of the power equipments' the multi-level topologies are used. Multilevel inverters are having more advantages, because of the power rating, better harmonic performance and minimized EMI emission. The multilevel inverter contains three topologies namely diode-clamped (DC-MLI), cascaded inverters (H-bridge-MLI), capacitor clamped inverters (FC-MLI) [3],[4]. The inverters have various types of modulation strategies to control the performance. The most popular PWM techniques are Space Vector Modulation (SVM) and carrier based. The carrier based modulation strategy segregated into two types they are single carrier and multi carrier PWM. The diode clamped multilevel inverters are having some good advance features like stair case waveform and minimized harmonics, and it is having a advantage of controlling the medium voltage drives [5]

In diode clamped inverters the carrier depends modulation techniques PD (phase disposition), POD (phase opposition disposition), APOD (alternative phase opposition disposition), PS (phase shift) gives best results in terms of constant carrier frequency not synchronized with the stator terminal frequency [6],[7]. For diode clamped inverters, phase opposition disposition (POD) depends modulation strategy is widely used but it offers a high harmonic performance [8]. Out of the modulation strategies the space vector PWM gives greater fundamental output voltage and improved harmonic performance of inverter.

In the applications of AC motor drives the analysis of the circulating current is more important. It produces between the neutral point of the motor and to the earth of the ground. The circulating current is responsible for the shaft voltage and damage of the bearing. The simultaneous switching of the series connected switches creates a voltage with high dv/dt at the load terminals of inverter. The amount of the circulating current will increase, and it is hazardous for the motor insulation and the cable also. In drive applications, it may causes the electromagnetic interference (EMI) this noise causes to trip the inverter drive [9]. It is very essential to limit the circulating current to certain boundary. A MLI can reduce the circulating current. Multilevel inverters have more number switching states because of this the output voltage will vary in small increments [10], it allows to mitigate the low frequency harmonics thereby the switching loss will be reduced. Furthermore, the circulating current will be reduced because of the low dv/dt [11]. The H-bridge inverter is implemented for the industrial applications in the literature [12],[13], however the main drawback of this type of configuration is it requires a high number of DC sources or isolation transformers on AC side. Among the all configurations present in the multilevel inverter, the analysis of circulating current is derived for the DC-MLI, which is the more frequent topology of the 3-level inverters. Because this topology is best suitable for high and medium voltage drives and can be directly connected to the utility power system.

Shaft voltages and their resulting currents were recognized by Alger [14] in 1920's. Various mechanical modifications in the system had been presented in the literature to eliminate the negative effects of the circulating current over motor bearing, like cable type, passive filters and the type of the bearing. There are two types of cables are available they are shielded type and unshielded type; the unshielded type of cable has no impact on the circulating currents. Even shielded type of cables

also has no impact on small rating motors, on large rating motors impact depends on the motor speed highest magnitude occurs at the low motor speed. *P. pairodamonchai* [15] has given the procedure for designing and complications while designing passive filters. There are 4 types of filters are available to eliminate the circulating current they are dv/dt filters (11 kW power level) and dv/dt reactors (110 and 500 kW power levels), sinusoidal filters [16], and common-mode chokes [17]. The elimination of bearing current is 30 to 90% [18], [19] based on the type of the filter on large rating motors and there is no impact [20] in small rating motors. Moreover, the passive filters have more size and weight penalties. There are two types of bearings are available insulated bearing [21], [22] and hybrid bearing. Insulated bearing eliminates 40 to 60% of the circulating current on small rating motors and 60 to 80% [23] on large rating motors. Hybrid bearings give complete suppression of bearing currents in small motors not suitable for the large motor applications [24].

The PWM technique provides different values of circulating current in the inverter. In this paper, the circulating current suppression is proposed with the different modulation strategies. A three-level diode clamped multi-level is designed for a three-phase, 400 V induction motor. Sinusoidal PWM, PD-SPWM, POD-SPWM, PS-SPWM techniques are implemented using a Matlab-2013b for a switching frequency of 1050 Hz and a modulating index, ma=0.9; The partial elimination of circulating current implemented using FPGA-SPARTEN III processor. Simulation and experimental results are provided to validate the three-level diode clamped inverter.

II. EFFECT OF HIGH CIRCULATING CURRENT

The circulating current is defined as the current that exists between the application neutral and ground.

$$I_{NG} = \frac{I_{AN}+I_{BN}+I_{CN}}{3} \quad (1)$$

The modern PWM inverters producing high frequency, high amplitude common mode voltages, which intern induces a shaft voltage on the rotor side of the motor. The induced shaft voltage exceeds the breakdown voltage of the lubricant in the bearings; this overall process results in the large circulating currents in the motor.

$$i_c = C_b \frac{dV_b}{dt} \quad (2)$$

$$i_c = BVR.C_b \frac{dV_{NG}}{dt} \quad (3)$$

Where BVR is the bearing voltage ratio.

This circulating current leads to the malfunctioning of the sensitive electronic equipment and control systems, false tripping of the ground fault relays. This damage the bearings, and finally leads to motor damage and also cause EMI. The instantaneous current sum is called as the circulating current. The generation of circulating current can be observed from the following figure 2.

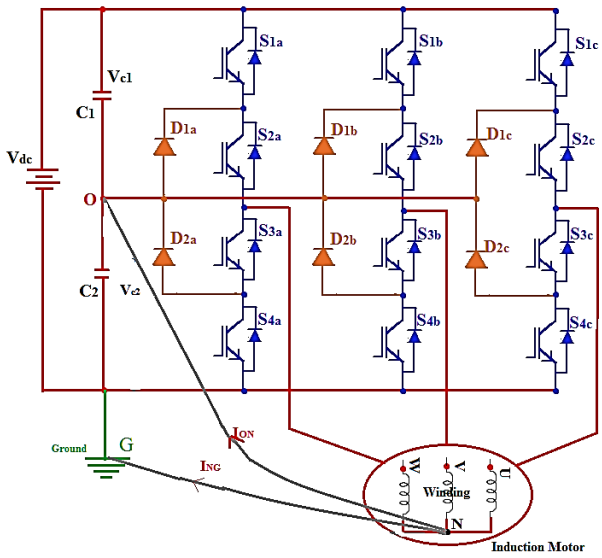


Fig 2. Circuit diagram of three-level NPC induction motor drive with circulating current

III. MODULATION TECHNIQUES

In the carrier based pulse width modulation the triangular wave is compared with the sine reference wave in order to generate the required PWM signal

3.1 SINGLE CARRIER PWM

The SPWM is a one of the most popular modulation technique in the voltage source inverters. In the SPWM, a reference sine wave is compared with one triangular waveform in order to generate gate signals in switching of the power electronic devices. In the medium voltage applications power dissipation is one of the most common problems. The open loop SPWM control method at fundamental frequency is to minimize the switching losses.

3.2 MULTI CARRIER PWM

The multi carrier PWM method is only for the multi-level inverter. This method is used to increase the efficiency of the multi-level inverters. In multi carrier PWM technique the carrier waves are in two ways, they are horizontal and vertical. The vertical carrier distribution techniques are classified into two configurations they are Phase Disposition (PD), Phase opposition Disposition (POD), where horizontal distribution arrangement is only one type and that is Phase Shift (PS) control technique.

3.2.1 PHASE DISPOSITION (PD): The phase disposition is a one of the technique in the multi carrier PWM. In this type of techniques, the number of carriers depends upon the multi-level inverter. The formula to know the number of carriers is (m-1), where m is number of levels. All carriers should be in phase disposition (PD, the PD-PWM is best suited for the NPC). We can observe this technique from the figure 3.2.1.

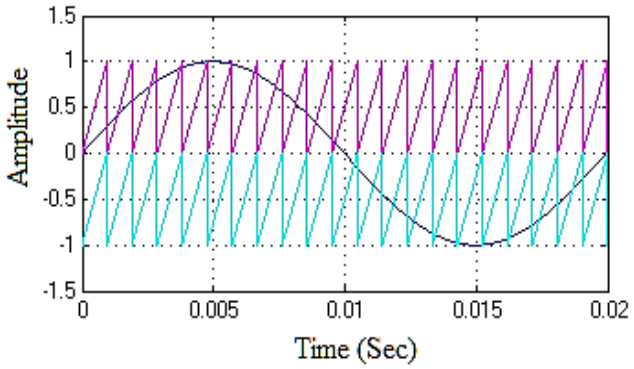


Fig 3.2.1 Phase Disposition

3.2.2 PHASE OPPOSITION DISPOSITION (POD): The number of carriers is (m-1), and all these carriers are in phase above and below the zero reference. The carriers those are above the zero reference are in phase, but the carriers below zero reference are in phase opposition. The figure 3.2.2 represents the POD technique.

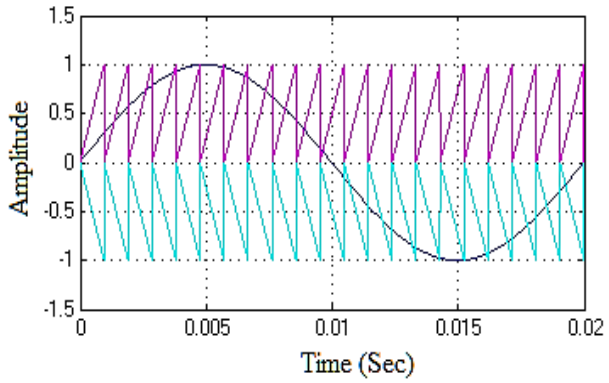


Fig 3.2.2 Phase Opposition Disposition

3.2.3 PHASE SHIFT (PS): The number of carriers is (m-1), and each carrier is shifted by an angle of 90 degree accordingly. The figure 3.2.3 represents the phase shift technique.

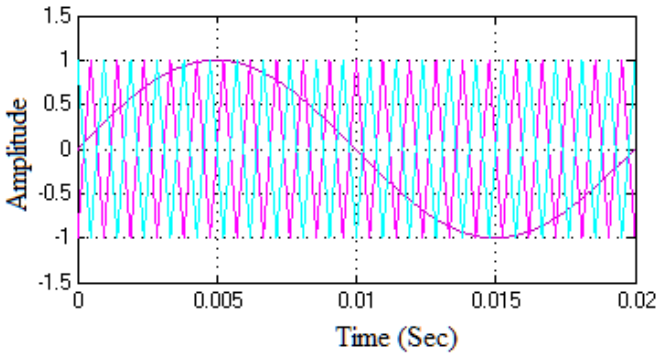
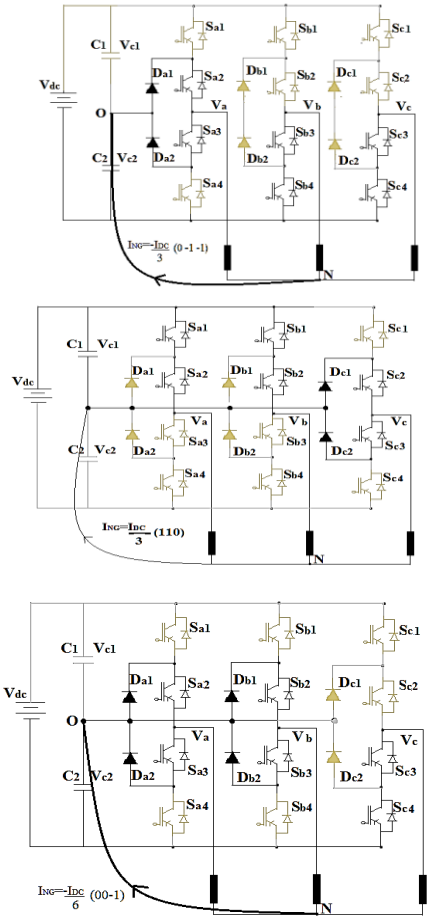


Fig 3.2.3 Phase Shift

IV. ANALYSIS OF CIRCULATING CURRENT DEPEND UPON SWITCHING STATES

The circulating currents have been discussed for the different switching states available in the below sections. The circulating current is defined as the current between the application neutral and the ground point of the inverter.

The circulating current depends on the amount of the inverter input current. In the star connected balanced load the sum of phase currents is zero. The three-level NPC inverter produces different combinations of the phase current depends on the switching states. There are 27 possible different switching states are available, each switching state has different amount of circulating current. The state 1 produces the phase current of +Idc/2, 0 state produces 0A& -1 state produces –Idc/2. All over 12 switching states produces ±Idc/6, 7 states produces zero circulating current, 6 states produce ±Idc/3& 2 states produce ±Idc/2. Some sample different switching states and their circulating current are shown in the figure 4.



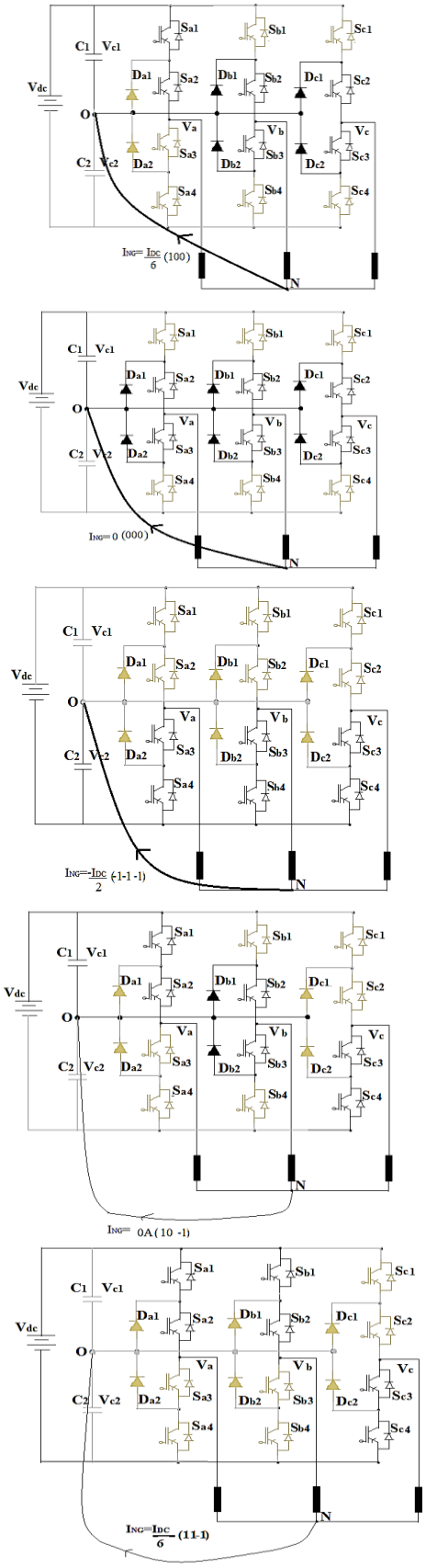


Fig 4. Different Switching states and its Circulating Current

V. CIRCULATING CURRENT REDUCTION

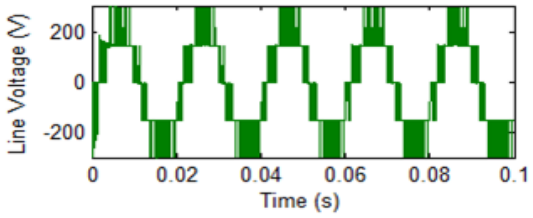
The circulating current minimization can be done by avoiding the abnormal switching of inverter. The PWM techniques like PD, POD, and PS can control the circulating current to such an extent, though the controlling of switching operation is not possible. The above chapter gives the detailed analysis of the available switching states and corresponding circulating current. From that analysis selecting the proper switching states the circulating current can be minimized. In the partial reduction of circulating current can be eliminated up to $I_{dc}/3(n-1)$ for n-level inverter. In the partial elimination, the 3-level inverter allows the circulating current magnitude of $\pm I_{dc}/6$. The common mode voltage is inversely proportional to the harmonics, which means the harmonics will improve with the elimination of the common mode voltage. In the similar way, the circulating current is directly proportional to the harmonics the amount of harmonics will decrease with the reduction of the circulating current.

Different PWM techniques like PS, PD, POD will reduce the circulating current to such an extent. The PS PWM technique eliminates only till the level of $\pm I_{dc}/2$. The PD technique will reduce the circulating current till $\pm I_{dc}/6$. Finally the POD algorithm will reduce the circulating current till $\pm I_{dc}/3$. By comparing all the above results the best algorithm to reduce the circulating current is PD algorithm type. As we know already the circulating current directly proportional to the harmonics. So the harmonic level in the PD technique is comparatively low compared to all different algorithms.

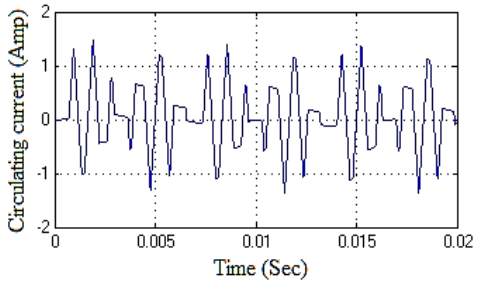
VI. SIMULATION RESULTS

The MATLAB/Simulink model is developed for three-level three-phase NPC-MLI with different multicarrier PWM scheme PD, POD, PS. The NPC-MLI is structure for 2kW connected with 1440 RPM induction motor with a rated voltage of 380V& current of 5A. The inverter dc-link is keep constant as 400V for all PWM schemes. The induction motor parameters are stator resistance=2.9Ω, rotor resistance=2.2Ω, stator leakage induction=12mH, rotor leakage induction=12mH& mutual induction=290mH. An open-loop stator voltage speed control method is used to control the speed of the motor. The inverter frequency is set as 3 kHz with dead time if 5microsec. The simulations are carried out for full range of modulation index from 0 to 0.9. The results are tested for all PWM schemes with modulation index range of 0 to 0.9 and the corresponding CMV and bearing current were measured. The Fig.5 shows the line voltage and its corresponding circulating current. From the results is could see that the PD method is delivering 245V, however due to the higher output CMV behavior , the circulating current on this PWM is critically high as 2 Amp peak to peak. Fig. 6 shows the live voltage and circulation current waveform of POD method. Here, the live voltage is observed as 249V and 1 Amps peak to peak circulating current. The CMV voltage for this POD is quite low compare to the PD method. The CMV for POD is $V_{dc}/6$, which is 50% lower than PD and PS method. As a result, the circulating current for POD method is 50% lower than PD and PS method. Finaly, the NPC-MLI is simulated for PS-PWM

method and results are capture for the line voltage and motor circulating current. The line voltage in the PS method is relatively higher than other two PWM method and the circulating current is measured as 3amps peak to peak, which is 200% higher than POD and 100% higher than PD method. The voltage THDs are measured and compared in table V along with circulating current. From the Table it could understood that, though the PD and PS method are good for fundamental voltage and THD%, the POD method is circulating current is lesser than other PWM. At the same direction, the fundamental voltage and voltage THD is better.

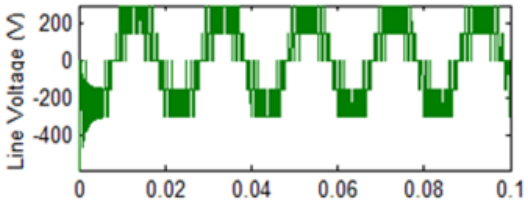


(a)

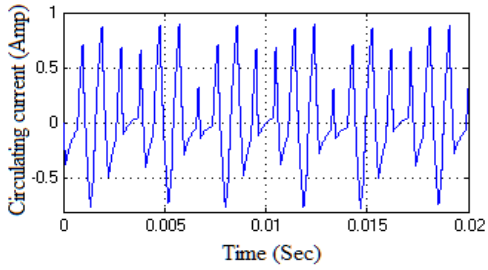


(b)

Fig 5. Simulation results of PD-PWM; (a) Line voltage, (b) circulating current

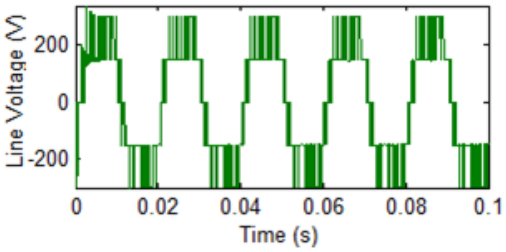


(a)

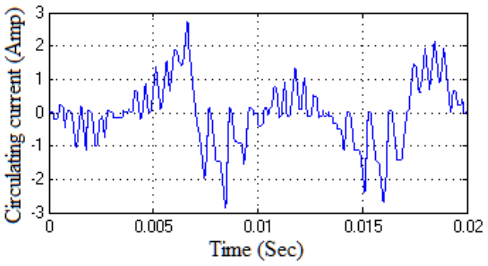


(b)

Fig 6. Simulation results of POD-PWM; (a) Line voltage, (b) Circulating current



(a)



(b)

Fig 7. Simulation results of PD-PWM; (a) Line voltage, (b) Circulating current

V. SIMULATION RESULTS

PWM technique	V_{THD}%	Circulating current
PD	24.3%	±2
POD	19.8%	±1
PS	32.4%	±3

VII. EXPERIMENTAL RESULTS

In order to validate the simulation results, the A 1kW three-phase three-level NPC-MLI connected 1 kW induction motor drive system is developed and the PWM schemes are collaborated with FPGA SPARTAN-III-3AN-XC3S400 FPGA family board as shown in Fig.8. The PD, POD and PS PWM schemes are developed through MATLAB/Simulink separately and down loaded in the FPGA board and texted the results for the full range of modulation indexes.

Fig.8 Experimental setup- 1kW three-phase NPC-MLI fed IM

The NPC-MLI is designed by using 12 IGBT -IRG4BC20FD and with 12V TLP gate driver circuits. The inverter is designed with current and voltage production to avoid the short circuit and wrong triggering issues. During the operation the inverter dc-link voltage is maintained as 400V and two 1000microF dc-link capacitors are used to maintains their neutral point fluctuation on the inverter input mid-point 'P. the with a fundamental frequency of 50 Hz and switching frequency of 3kHz. The rating of the motor used here is 1 Kw and 50 mH inductance and the capacitance is 15nF. For all PWM methods the output voltage, CMV and voltage THD is measured using DSO. The circulating current is measured through multicenter, since there no option to measure the circulating current trough DSO. Fig. 9 is shows the experimental results of PD technique output voltage and common mode voltage for 0.9 modulation index. Here, the CMV voltage is measured as 97V ($\pm V_{dc}/3$) and corresponding circulation current measured as 2 amps. When the PS method the CMV is measured as 87V as shown in fig.10. the circulating current is measured as 3 amps. The fig. 11 shows the line voltage and CMV for POD method. Here, the line voltage is observed as 250.3V and CMV is 34V. The fig. 12 to fig. 14 shows the Line voltage harmonics spectra. Based on the %THD, the POD method lower order harmonics performance sis better than other methods.

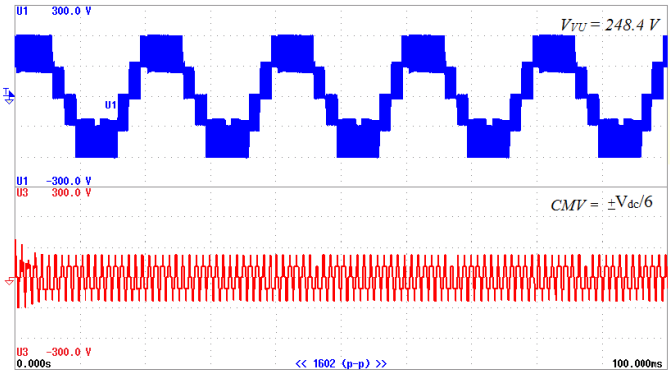


Fig 9. Experimental results for PD technique; Output voltage (150V/div) (b) Common mode voltage (150V/div)

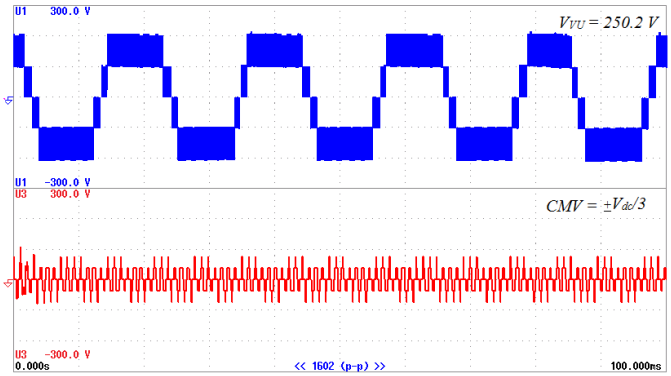


Fig 10. Experimental results for POD technique; Output voltage (150V/div) (b) Common mode voltage (150V/div)

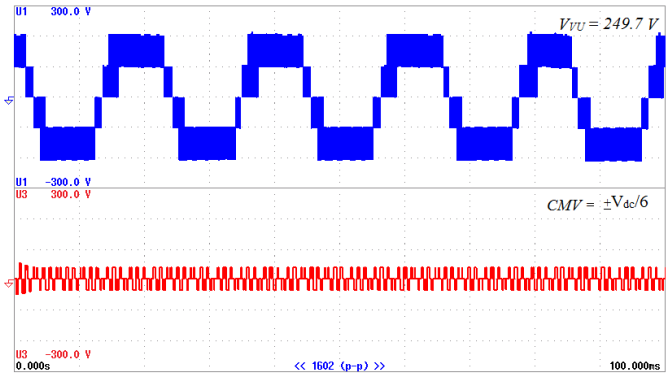


Fig 11. Experimental results for PS technique; Output voltage (150V/div) (b) Common mode voltage (150V/div)

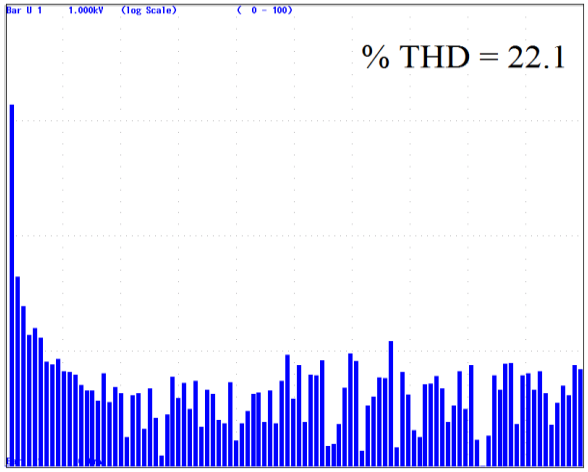


Fig 12. Experimental THD spectra for PD technique

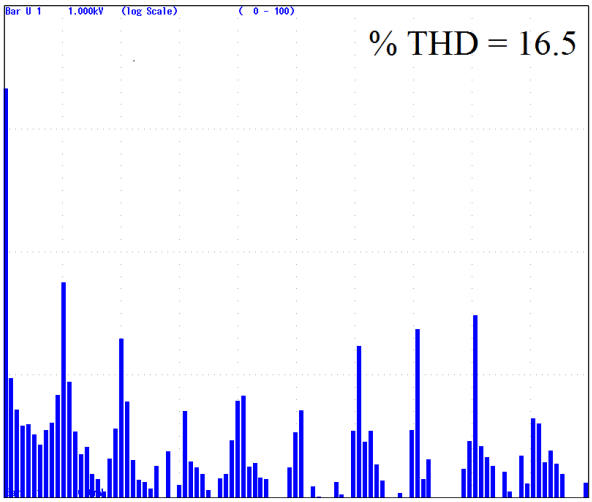


Fig 13. Experimental THD spectra for POD technique

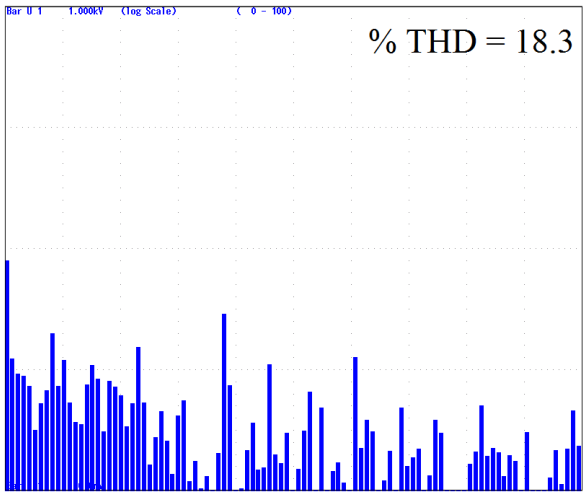


Fig 14. Experimental THD spectra for PS technique

The fig.15 shows the Experimental results performance comparisons among PD, POD and PS with respect to Line voltage and voltage %THD for the different range of modulation index. Here, for all the PWM voltage THD is poor in lower modulation indexes due to the pulse dropping, where as in the line voltage magnitude is increasing while the increasing in modulation index. The voltage harmonics performance is better in POD-PWM scheme among all other PWM methods. Similarly, the CMV and circulating current is low in POD compare to the other PWMs PD and PS. The circulating current in POD is 200% lower than PS and 100% lower than PD.

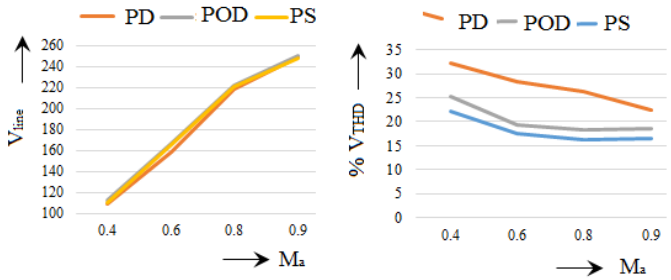


Fig 15. Experimental results performance comparisons among PD, POD and PS with respect to Line voltage and voltage %THD for the different range of modulation index.

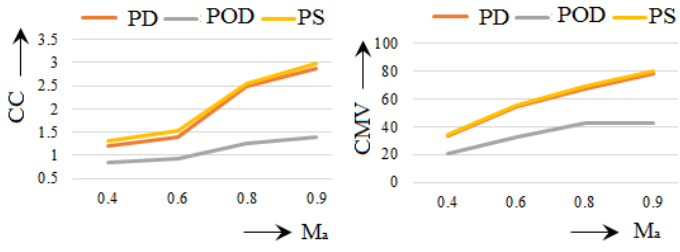


Fig 15. Experimental results performance comparisons among PD, POD and PS with respect to CMV and circulating current for the different range of modulation index

VIII. CONCLUSION

Conventional two-level inverter generates the circulating current which is responsible for the premature failure of the bearings. Multi-level inverters are having the inherent ability to reduce the circulating current. Simulation and experimental results prove that the magnitude of the circulating current minimized to ±Idc/6, and that has a minimum THD in the current and line voltage. A multi-level eliminates the dv/dt in its output voltage and therefore the circulating current also reduced.

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