THE CONTRIBUTION OF DIRECT TORQUE CONTROL WITH APPLICATION OF FUZZY LOGIC ON THE PERFORMANCE OF A MULTI-LEVEL INVERTER FED INDUCTION MACHINEWITH A FAULT TOLERANCE

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***Summary* - Today it is possible to obtain induction machines performances similar to those of dc machines through the mastering of power electronics and control. Moreover, there are new methods of control for sensor less speed traction-type applications already studied particularly those related to the Direct Torque Control technique (DTC). This study consists at optimizing the three-level DTC algorithm fed from an NPC structure multilevel inverter with fault tolerant using a reconfigurable redundant spare arm to increase the average value of the torque. The results obtained in the DTC are further improved by applying the technique of fuzzy logic.**

Keywords—Multilevel Inverter, DTC, NPC, Fault tolerance, Fuzzy Logic.

I. INTRODUCTION

These last years, the use of multilevel inverters has largely increased in many industrial applications [1].The multilevel voltage source inverter can be classified into three major circuit topologies, namely, diode clamped multilevel inverter, commonly known as three-level Neutral-Point-Clamped (NPC) voltage source inverter, which was first introduced by Akagi et al. in 1981[2],flying capacitor inverter originated from conventional two-level inverter by adding capacitors to the series connected switches, cascaded H-bridge inverter, which is composed of a series of single-phase H-bridge power cells [3].The orientation to the multilevel inverter is due to the various advantages of these topologies,like operating under high dc-bus voltages, reduction in output voltage harmonics [4], low voltage stress on power switches [5], and low dv/dt of output voltage [6].Fault-tolerant capability of power electronics equipment is extremely important to safety-critical applications where continuous drive operation must be insured.Obviously, this capability is expensive and can be justified only for applications with high reliability requirements where risk to human life is substantial, damage of the environment or high costs arising from downtime.In many critical industrial applications, multilevel inverters are used as induction machine drive. The failure of one ormore IGBT module of this drive can causethe total shut down of the system.One of thesolution proposed to handle this problem, is the reconfiguration of the faulty inverter [7][8][9].The DTC widely applied for induction machine control [10], has been applied in the fault tolerant control [11].

In this paper, a fault control strategy is proposed for induction machine drives fed with three-level NPC converter by applying the direct torque control.The proposed reconfigured multilevel NPC inverter is first described. The DTC technique including the inverter system is then dealt with.Wethen move to the study of the system under various faults such as:1) switch short in a phase leg, 2) switch open in a phase leg, 3) phase leg open.The post-fault performance of each drive is analyzed and test results are presented for the reliability of tolerance and susceptibility of fault.

II. PROPOSED TOPOLOGY

The additional phase leg fault-tolerant inverter topology consists of four inverter legs and a standard three-phase machine, as shown in Fig. 1. In this topology, each phase leg contains a series of two fuses at the terminal upper and lower power devices to isolate the leg for shoot through faults similar to additional leg topology. Each phase leg contains a series of two fuses at the upper and lower power devices terminals to isolate the leg for shoot through faults similar to additional leg topology. Each phase winding of the machine is connected to a normally closed side of an SPDT electromechanical relay, while the open terminals of three relays are tied to the center point of the inverter fourth leg, as shown in Fig. 1. Under normal operation, the fourth leg is not activated. [12][13].

If a fault occurs in any one of the inverter phase legs, that leg is isolated by means of the relay, and the phase winding is connected to the additional phase leg and activated.

This topology provides rated post-fault power without the overrating of power devices, and the output torque is similar to that of the pre-fault operation without excessive torque ripple, as will be shown in Section III via simulation work. It consists of sixteen MOSFETs, eight fuses, three relays, six terminals connections, and a filter capacitor.

The flying capacitor multilevel inverter is another type of multilevel inverter that can tolerate switch faults through reconfiguration of the inverter switching pattern [14].

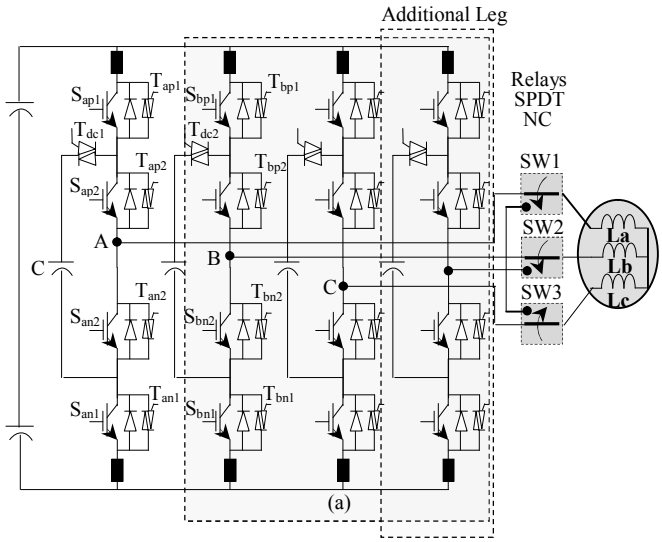


Fig. 1. Schematic of three leg of a flying capacitor multilevel (three-level) inverter with isolating capability.

Three legs of the fault-tolerant three-level flying capacitorinverter are shown. Assuming that $S_{ap1}$is a faulty switch, it canbe bypassed using the parallel low-frequency switch, T_{bp1}.At the same time, the corresponding switch in the opposite polarity, Tbn1is forced to turn on, and $T_{dc2}$is turned off to separate the related dc-bus capacitor branch. Accordingly, the remaining switches,S_{bp2} and S_{bn2}can operate like an inverter leg in conventional two-level inverters. The most remarkable feature of this design is that it does not require an auxiliary leg in addition to tolerating a single-switch fault per phase without reducing the quality of the generated three-phase output voltagesshown in part(a). The disadvantage of this three-level inverter is that,S_{bp2} and S_{bn2} must hold twice the normal voltage magnitude during the post-fault situation. As the number of levels (or cells) increases, the number of possible alternative switching patterns for the same output voltage increases. For example, in a four-level flying capacitor inverter, the number of levels in the output voltages can remain constant after isolating a single switch per phase [14].

II. FAULT TOLERANT DTC STRATEGY

II. 1. DTC Principle

Direct Torque Control is based on control of both torqueamplitude and stator flux amplitude of the machine byapplying appropriate stator voltage vectors using twohysteresis regulators. The control scheme principle isdescribed in Fig.2. Stator flux estimation is performed usingstator current and voltage measurements and stator voltageequation in$\propto \beta$ reference frame:

$$\emptyset_s = \sqrt{\emptyset_{s\alpha}^2 + \emptyset_{s\beta}^2} \quad (5)$$

Where:

$$\emptyset_{s\alpha} = \int (V_{s\alpha} - R_s I_{s\alpha}) dt \quad (6)$$

$$\emptyset_{s\beta} = \int \left(V_{s\beta} - R_s I_{s\beta}\right) dt \quad (3)$$

The electromagnetic torque is calculated as:

$$T_{em} = P.(\emptyset_{s\beta}.I_{s\alpha} - \emptyset_{s\alpha}.I_{s\beta}) \quad (4)$$

Where$P$ is the number of poles.

Fig.2 shows the different blocs of the DTC strategy.

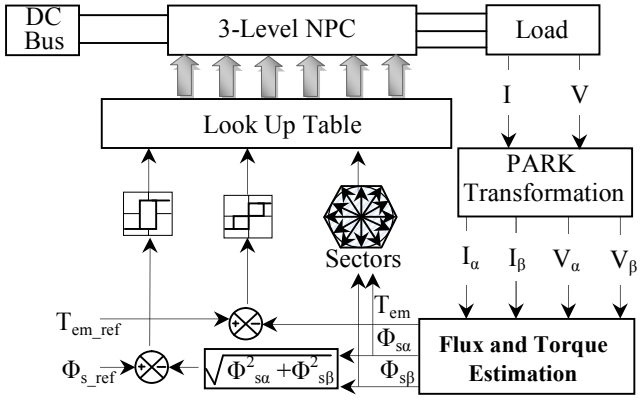


Fig. 2.DTC strategy.

II.2. SELECTION OF THE VOLTAGEVECTOR Vs

The choice of the vector Vs depends on the location of the $\emptyset_s$ in the referential (S), on the desired variation of the module $\emptyset_s$, on the desired variation torque and on the direction of rotation of $\emptyset_s$. The evolution space of $\emptyset_s$in (S) is divided into twelve space areas, with i = [1,12] see Fig.3.

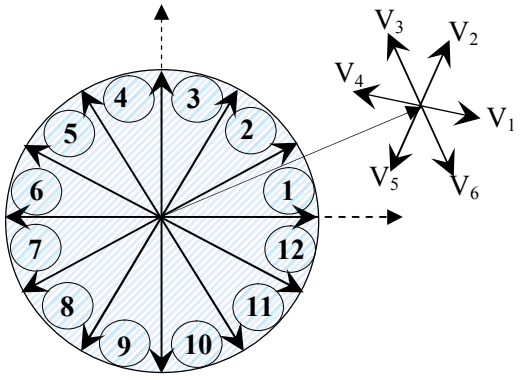


Fig.3. Representation of 12 divisions of the complex plane.

The voltage vectors associated with switching states are:

Vector	Symbol
ZVV	(P P P),(O O O),(N N N)
MVV	(P O N),(O P N),(N P O),(N O P),(O N P),(O N P)
LVV	(P N N),(P P N),(N P N),(N P P),(N N P),(P N P)
USVV	(P O O),(P P O),(O P O),(O P P),(O O P),(P O P)
LSVV	(O N N),(O O N),(N O N),(N O O),(N N O),(O N O)

Tab. 1. Voltage vectors associated with switching states of 3-levelinverter.

The table shows that there are 27 states of the inverter switching. Under these conditions, there will be 19 different vector voltages.

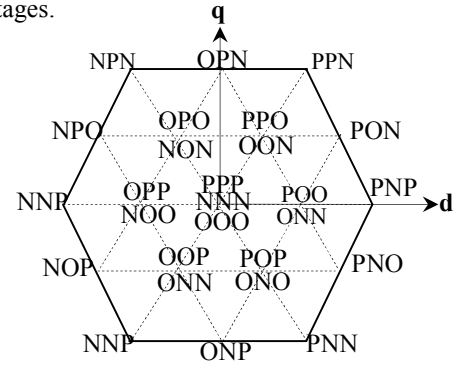


Fig.4. Space voltage vector diagram in normal condition.

Figure 4 shows that the voltage vectors are classified into four groups according to their modules. These are:

-ZVV group, the zero voltage vectors: V_0.
-SVV group, the small voltage vectors:$V_1,V_4,V_7,V_{10},V_{13},V_{16}$. -MVV group, the mean voltage vectors :$V_3,V_6,V_9,V_{12},V_{15},V_{18}$ -LVV group, the large voltage vectors:$V_2,V_5,V_8,V_{11},V_{14},V_{17}$.

III.ELABORATION DE LA TABLE DE COMMUTATION AVEC LES 4 GROUPES DES VECTEURS TENSION

N		N	N	N	N	N	N	N	N	N	N	N	N
cflx	ccpl												
1	2	V	V	V	V	V11	V	V	V	V	V	V	V
	1	V	V	V	V	V9	V	V	V	V	V	V	V
	0	V	V	V	V	V0	V	V	V	V	V	V	V
	-1	V	V	V	V	V6	V	V	V	V	V	V	V
	-2	V	V	V	V	V5	V	V	V	V	V	V	V
0	2	V	V	V	V	V10	V	V	V	V	V	V	V
	1	V	V	V	V	V10	V	V	V	V	V	V	V
	0	V	V	V	V	V0	V	V	V	V	V	V	V
	-1	V	V	V	V	V0	V	V	V	V	V	V	V
	-2	V	V	V	V	V1	V	V	V	V	V	V	V
-1	2	V	V	V	V	V14	V	V	V	V	V	V	V
	1	V	V	V	V	V15	V	V	V	V	V	V	V
	0	V	V	V	V	V0	V	V	V	V	V	V	V
	-1	V	V	V	V	V18	V	V	V	V	V	V	V
	-2	V	V	V	V	V2	V	V	V	V	V	V	V

Tab .2 Look up table for twelve sectors before failure.

IV. BASED FUZZY LOGIC DTC

A. Based principle of fuzzy logic

Fuzzy logic is a method of treatment of uncertainties and is intended for the representation of imprecise knowledge. It is based on current linguistic terms such as: small, large, medium.... etc... It allows intermediate values between right and wrongand admits overlap between them. [15][16].

B. Control Variable

Control rules can be expressed in terms of input variables and outputs as follows:R_i: if ε_c is A_i and $\varepsilon_{\phi s}$ is B_i , and Θ_s is C_i then n is N_i where A_i,B_i, N_i are the fuzzy sets [17].
The treatment of these rules shall be made by the method of the least Mamdani expressed by: $\mu_{Ri}(n)=\min(\alpha_i,N_i)$;With:

$$\alpha_i=\min(\mu_{Ai}(\varepsilon_C),\mu_{Bi}(\varepsilon_\phi),\mu_{Ci}(\Theta_S)) \quad (7)$$

C. Switching table for (DTC_LF)

The following tables are similar.Simulation results of stator current, stator flux, electromagnetic torque and output voltage for the case of a three-phase IM with 10Nm load at t=0.3s.variables errors: "ε_ϕ"flux error,"ε_c"Torque errors and "ε_ϕ "flux position.

ε_ϕ \ ε_C	LS	NS	NL	PS	LS	NS	NL	PS	LS	NS	NL	PS
P	V5 Θ1	V1 Θ1	V2 Θ1	V2	V1 Θ2	V1 Θ2	V2 Θ2	V3	V1 Θ3	V2 Θ3	V3 Θ3	V3
N	V5	V7	V4	V3	V6	V5	V4	V4	V6	V0	V5	V4
P	V2 Θ4	V2 Θ4	V3 Θ4	V4	V2 Θ5	V3 Θ5	V4 Θ5	V4	V3 Θ6	V3 Θ6	V4 Θ6	V5
N	V1	V6	V5	V5	V1	V7	V6	V5	V2	V1	V6	V6
P	V3 Θ7	V4 Θ7	V5 Θ7	V5	V4 Θ8	V4 Θ8	V5 Θ8	V6	V4 Θ9	V5 Θ9	V6 Θ9	V6
N	V2	V0	V1	V6	V3	V2	V1	V1	V3	V7	V2	V1
P	V4 Θ10	V4 Θ10	V5 Θ10	V6	V6 Θ11	V5 Θ11	V1 Θ11	V1	V6 Θ12	V6 Θ12	V1 Θ12	V2
N	V3	V2	V1	V1	V4	V0	V3	V2	V5	V4	V3	V3

Tab .3Table de commutation pour douze secteurs après le défaut.

III. SIMULATION RESULTS

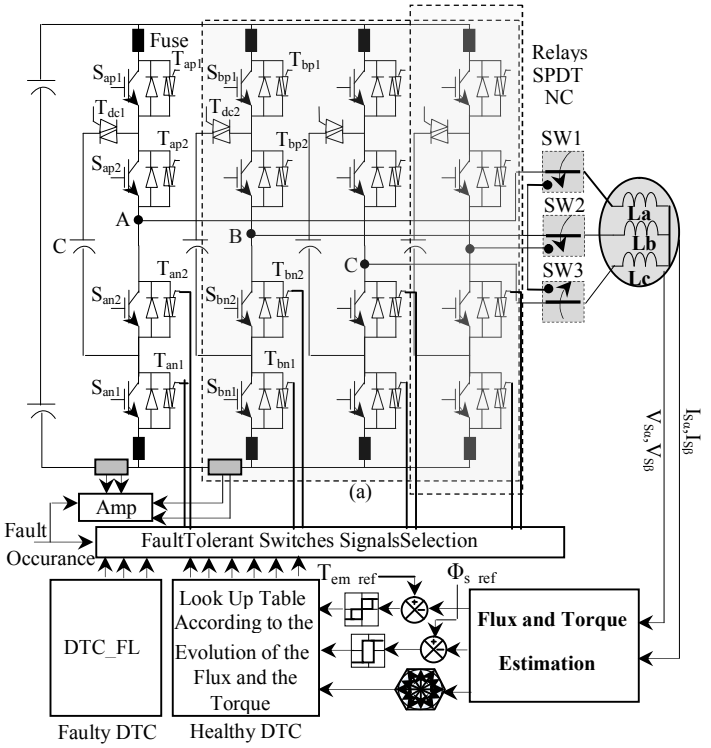


Fig. 5.Schematic of three leg of a flying capacitor multilevel (three-level) inverter with isolating capability.

The proposed DTC strategy (Fig.5) is tested on a 7.5 kW induction machine.

The simulation parameters are defined as follows: DC bus=500V, torque hysteresis band=10%, flux hysteresis band=10%. Torque and flux references are respectively 10N.m and 1.2Web.

The controller block diagram for this topology is shown inFig. 5. The normally open terminals of all the SPDT relaysSW1–SW3 are connected to the additional phase leg, as shownin Fig. 5. When a fault occurs in a given phase leg, theSPDT relay of that phase isolates the faulted inverter phaseleg and connects the machine phase winding to the additionalleg while steering the gate pulses of the faulted inverter legto the respective power devices of the additional phase leg forpostfault operation.

Dans le cas où un défaut sera signalé au niveau du reste dispositif (le bras redondant ou les deux premiers bras sains), à ce moment les relais de SPST reconfigurent l'onduleur de trois niveaux à deux niveaux.

Using this model,the following faults have been simulated additional phase leg.

1) switch short-circuit fault in a phase leg;
2) switch gate pulse open fault in a phase leg;
3) phase leg open fault.

1) *Switch Short-Circuit Fault in a Phase Leg*:In this fault,the bottom switch in phase leg A is shorted, as symbolized inFig. 5.The performance of the drive during normal operation, faulted condition, and postfault operation is shown in Fig. 6.

The fault is created at t = 0.41 s, and the gate pulse to the upper device is disabled to avoid a shoot through condition. The drive is allowed to continue under faulted condition for 0.05 s, and remediation action is taken by isolating the faulted phase leg A by means of the electromechanical relay SW1 while steering the gate pulses of the faulted phase leg to respective devices of the additional phase leg inverter.The second fault is creacted at t=0.5s, The drive is allowed to continue under faulted condition for 0.01 s, assuming that $S_{ap1}$is a faulty switch, it canbe bypassed using the parallel low-frequency switch, T_{bp1}.At the same time, the corresponding switch in the opposite polarity,$T_{bn1}$is forced to turn on, and $T_{dc2}$is turned off to separate the related dc-bus capacitor branch. Accordingly, the remaining switches,S_{bp2} and S_{bn2}can operate like an inverter leg in conventional two-level inverters.

The simulation results of phase currents and electromagnetic torque ofthe machine for this fault under prefault, faulted, and postfault operation is shown in Fig. 6. It is clear that under faultconditions, the drive experiences large torque oscillations as in the previous cases, however, this topology restores normal postfault operation without an inverter overrating, as required in the other two topologies[18].

2) *Switch Gate Pulse Open in a Phase Leg*: Simulation results of switch gate pulse open in a phase leg are shown in Fig. 6. In this case, large torque oscillations occur during thefault, and the normal postfault operation is restored with theadditional phase leg.

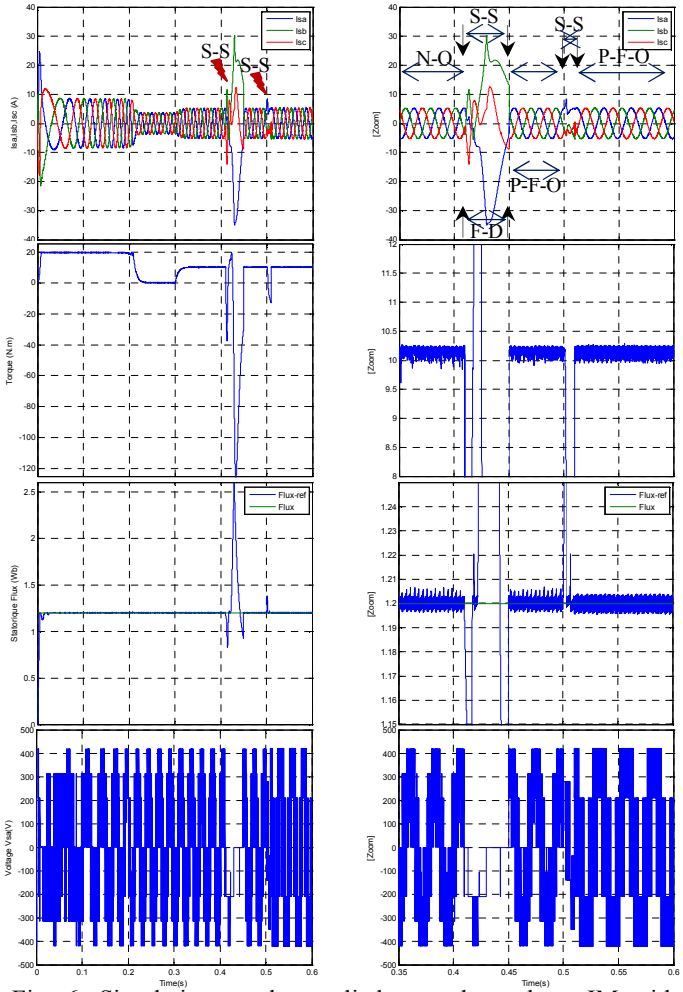
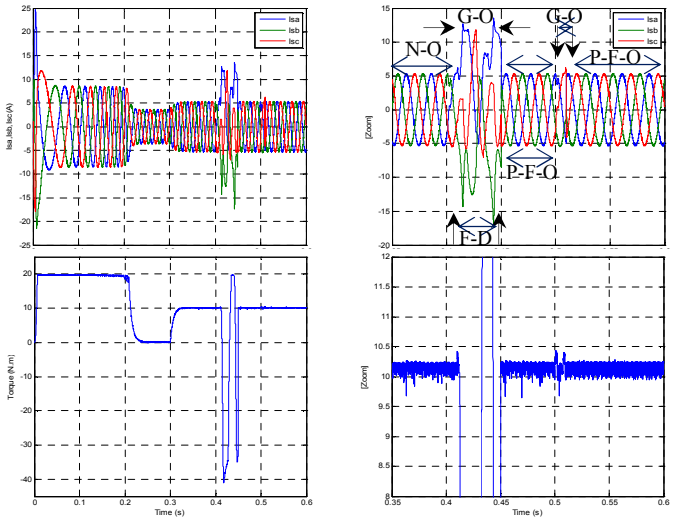


Fig. 6. Simulation results applied to a three-phase IM with 10Nm load at t=0.3s.Stator currents, Stator flux, electromagnetic torque and output voltage. Switch short-circuit fault failure introduced inS_{an1},S_{bn2} at 0.41s,0.5srespectively.



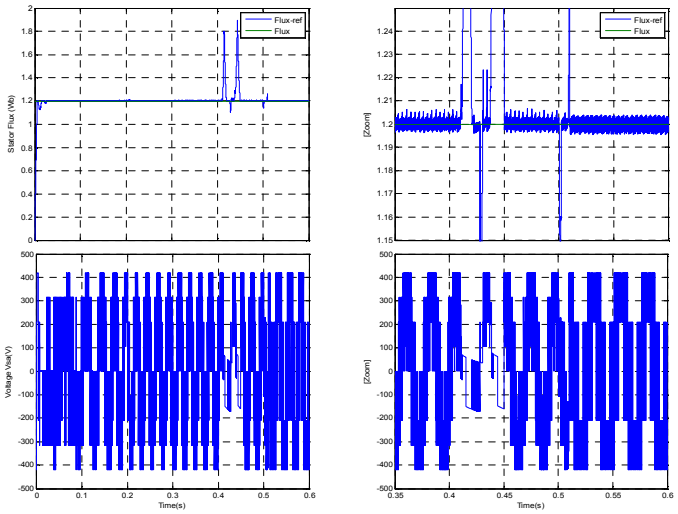
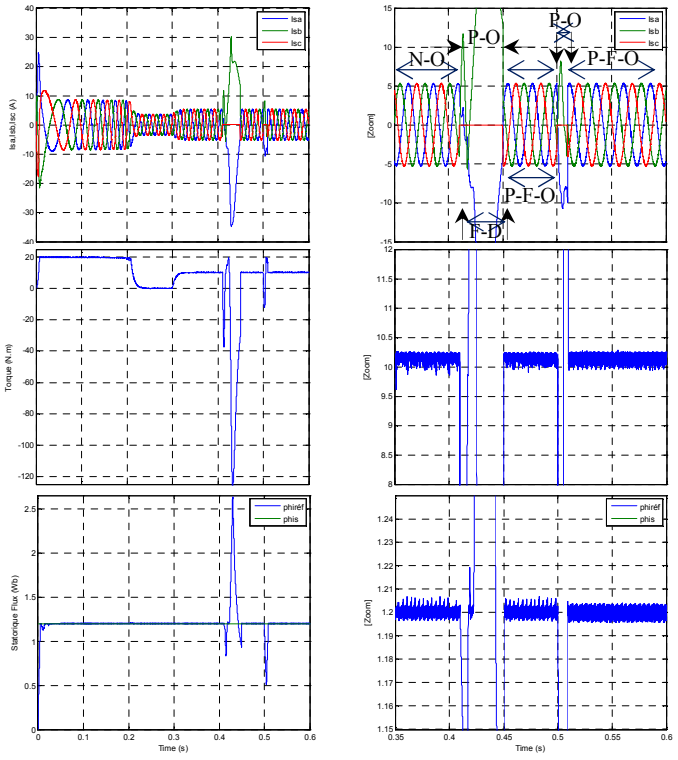


Fig. 7. Simulation results of stator current, stator flux, electromagnetic torque and output voltage for the case of a three-phase IM with 10Nm load at t=0.3s.The gate pulse open fault failure introduced in S_{an1},S_{bn2} at 0.41s and 0.5s respectively.

3) Phase Leg Open Faults: Simulation results of a phase leg open fault are shown in Fig. 8. In this case, large torque oscillations also occur during the fault, and the normal post-fault operation is restored by transferring the phase winding from the faulted phase leg to the additional phase leg and activating. Thus, the additional phase leg topology restores normal post-fault operation, which is an important requirement for automotive safety critical systems.



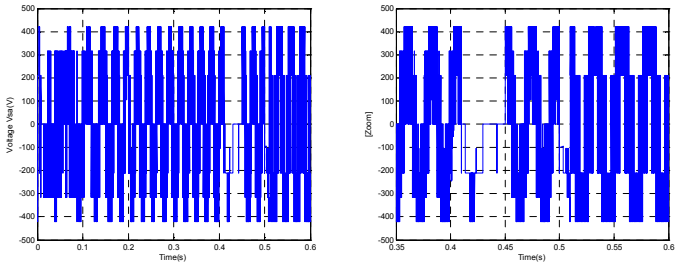


Fig. 8.Simulation results of stator current, stator flux, electromagnetic torque and output voltage for the case of a three-phase IM with 10Nm load at t=0.3s. The phase open fault failure introduced in S_{an1},S_{bn2} at 0.41s and 0.5s respectively.

Abbreviation	Meaning
NO	Normal Operation
FD	Fault Duration
SS	Switch Sort-Circuit
GO	Gate pulse Open
PO	Phase leg Open
PFO	Post Fault Operation

Tab .3Table of different fault proposed and abbreviation.

VI. OTHER FAULTS AFFECTING THE SYSTEM PERFORMANCE

There are several other faults, including dc bus fault and machine winding faults, that can affect the performance of the drive. Though the scope of this paper is not to address the machine faults, the authors would like to provide some information without violating some of the company's proprietary/ confidential information with respect to the mean time between failures of the system, including the following.

1) In case of a dc bus fault resulting dc bus over current, the over current limit circuit trips the breaker. For example, dc bus capacitor failure is one such type of fault that occurs commonly.
2) To avoid winding faults, machines are built with proper winding insulation, slot liners between winding and the stator core, and phase separators in the slots as well as at the end windings. Providing adequate separation between the lead wire terminals at the connector and potting with insulation compound at the back of the connector minimizes terminal shorts. In low-voltage machines, which in this case is 42 V, the possibility of any machine fault is very remote, which is an order or two magnitudes less than the inverter faults.

The types of machine faults are listed as follows.

1) Line–ground fault: it can be minimized by proper slot insulation and impregnation of windings.
2) Line–line fault: proper phase separation insulator likeNomex 410 in slots as well as at the end windings minimizes such fault.
3) Three-phase terminal short fault: proper spacing and termination of lead wires to the connector and potting

with insulating resin compound at the back of the connector minimizes such fault.

4) Turn–turn fault: by providing additional insulation for the first few turns of the coil of each phase and also providing slot insulation to slightly protrude the stator slots off so that impregnation resign bonds to the stator core minimizes such fault.

A. Faults Identification

Identification of faults is very important for the fault-tolerant system. Prognostics and diagnostics of the faults in the machine as well as in the inverter are new research topics. Identification techniques, such as wavelets, Kalman filters, and particle filters, are being developed for prognostics of faults in the machine as well as in the inverter based on phase current and voltage measurements to avoid catastrophic failures.

Most of the faults can be identified by phase currents and gatepulses signatures, and necessary actions can be taken to isolatethe faulted component. Over current protection circuit of eachphase can detect some machine faults and trips the main circuitbreaker.

1) Phase–ground fault: the ground fault circuit at the inverter detects the deviation in summation of three phase currents and trips the dc bus circuit breaker.
2) Line–line fault: a line-to-line fault due to failure of twoupper or lower switching devices of inverter legs connected to different phases or short of two phases near themotor terminal box can be detected by the over currentprotection circuit.
3) Gate pulse open fault: the gate pulse not reaching the gate of any switching device of a phase leg can be identified by a flag of the digital logic circuitry. The gate pulse fault of any switching device of a phase leg can be identified by the gate pulse circuitry as well as by the voltage across the device. The faulted leg is isolated, and the healthy additional leg is connected for postfault operation.

IX. SUMMARY AND CONCLUSION

Three fault-tolerant inverter configurations have been analyzed as to their suitability for control systems.

The simplified additional phase leg topology with mechanical relays was found to be the most cost effective and fault tolerant of the topology examined. This topology uses simple normally closed SPDT mechanical relays to restore normal postfault operation without excessive torque ripple or phase currents.

The performance of this simplified additional leg inverter technology was verified through simulations.

Therefore, for safety of direct torque of control with application artificial intelligence fuzzy logic,the simplified additional phase leg inverter topology with normally closed electromechanical relays is the most cost-effective configuration that has a postfault performance that matches the normal prefault operation. Moreover, it uses conventional threephase machines without the additional phase windings or leadsto provide access to the neutral, as required in the other two topologies.

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