

# DEVICES BASED ON PROGRAMMABLE LOGIC INTEGRATED CIRCUITS TO CONTROL THE STEPPER MOTOR

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The article proposes a new approach for solving the problem of control stepper motor. Actuators based on the discrete type stepper motor are electrical devices that convert the control signal to the angular or linear displacement of the rotor with fixing it in a given situation. To generate control signals stepper motor device designed made on the basis of programmable logic integrated circuit. These simulation results confirm efficiency of the control devices. The developed scheme of direct impulse control stepper motors for programmable logic integrated circuits with small modifications can be used in a variety of destinations devices inertia and precise actuators in robotics, in the electronic industry, medical technetium, etc.

Keywords: stepper motor, programmable logic integrated circuits

## 1 INTRODUCTION

The growing demand for devices that have reduced design and production cycle, rapid prototyping and reconfiguration of digital systems, convenience of the programming by the user and low-cost, continuously expanding the scope of the programmable logic integrated circuits.

Manufacturers offer a variety of programmable logic integrated circuits [1-4]: simple, programmable, matrix and complex logic device (SPLD, PAL, CPLD); programmable basic matrix chip (FPGA). They have specific characteristics and the combination of parameters such as speed, power consumption, the level of integration and cost. This diversity is one of the most difficult problems faced by developers of electronic devices. However, due to the fact that the manufacturers of programmable logic integrated circuits pursuing a policy of industrial standardization, the task of selection of such devices much easier.

The largest application currently has a variety of programmable logic integrated circuits - FPGA (Field Programmable Gate Array). FPGA is a matrix of programmable logic blocks, between the rows and columns which are programmable connections. Today's highly integrated FPGA crystals contain, in addition matrices built a powerful memory, transceivers, microcontrollers, a user can connect to solve their problems by means of programmable connections inside the crystal, without limiting the number of reprogramming. Variety of programmable logic integrated circuits CPLD (Complex Programmable Logic Device) - complex programmable logic devices are volatile, with some restrictions allowable number of overwriting. Such programmable logic integrated circuits are characterized by high ratio of the number of logic elements to the number of registers and different flexible asset tracing. The main advantages of CPLD - lower power consumption and simplified regime for the preservation of information.

When choosing a specific type, series and family of FPGA or CPLD designers usually guided by complexity, expressed in number of logic elements, and the availability of development tools.

Price FPGA, CPLD proportional to their capacity, and hence to implement the developed device, you must select the programmable logic integrated circuits with optimal capacity. It is possible to use cheap FPGA, CPLD, because due to the rapid repetition of simple operations you can perform slow applications for small hardware cost.

Also, please note that the degree of integration of FPGA, CPLD has reached a level at which the size of the crystal is not affected by the total number of valves.

However, for large projects, created from scratch, while the full verification of the traditional ways may prove to be unacceptably high, forcing the use of functional blocks developed by third-party firms. Breadth of choice of functional blocks and the possibility to take their parameters as a whole simulation developed device is an important criterion in selecting a specific chip for the implementation of projects. In the systems management of the various objects are frequently used devices made on the basis of microcontrollers or microprocessors. With their help, we can solve many problems of measurement, management and maintenance. Such devices are easily programmable, low power consumption and without complications included in the scheme.

However, FPGA, CPLD have a large number of findings, customizable interface of inputs and outputs with virtually any standard logic levels and the ability to replace multiple chips, including the microcontroller, the registers of ports, interface, etc.

Accounting architectural features and advantages of programmable logic integrated circuits to microprocessors allows you to make competitive products on the FPGA, CPLD.

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## 2 DEVELOPMENT OF A STEPPER MOTOR CONTROL

An example of result-based approach to the selection of components for the implementation of the designed device is the development of control devices stepper motor (SM) using a programmable logic integrated circuit.

In automatic control systems as an actuator is often used stepper motors, called the global technical literature: a valve-inductor; controlled rectifier jet; switched reactive with variable magnetic resistance, the electron-switched, non-contact jet, etc.

Stepper motor is an electromechanical device that converts a control signal to the angular (or linear) displacement of the rotor with the exact fixing it in a given situation.

Rotor SM rotates discretely after the receipt of each pulse from the output management system to the inputs of the phase windings of the motor, or remains stationary, when the pulses are not received. With the ability to control movement of the rotor at any corner of SM has the best properties that can be successfully used in the design of the discrete actuator type.

When you type SM electric actuator was chosen as a hybrid type of engine. This permanent magnet motors, but with a large number of poles. Selected type SM was estimated by the following parameters: the frequency of the circular vibration, electromagnetic time constant, the coefficient of internal damping, limiting mechanical and dynamic characteristics.

Limit the mechanical and dynamic characteristics allow you to select the frequency of control pulses, applied to the phase windings SM. So the maximum mechanical properties set the permissible time dependence of resistance on the frequency of control pulses in a steady mode. With increasing frequency control pulses affects the delay in current rise and at a certain frequency limit engine torque becomes zero.

For different types of SM, this frequency may be several kilohertz. Limit dynamic characteristics, the dependence of the frequency of intake capacity from the moment of resistance and moment of inertia of the load, allow the final choice of the frequency of control pulses.

Frequency of intake capacity - this is the maximum frequency of the control pulses, at which the engine can start without losing a step.

This frequency increases with: increasing the maximum clock time; reduction step, reducing the time constant of the windings, the load and moment of inertia.

Typically SM frequency of intake capacity is recommended to choose between 100 ... 1000 Hz. Thus, SM has to work out a single control pulses, and a series of pulses at a frequency determined by limiting dynamic characteristics.

Found that at frequencies up to 200 ... 400 Hz SM can be stopped within a single step. Because of inertia at high frequencies such a stop is difficult. Therefore, when developing a system of direct control actuating

device, with the exact position and practicing with a small moment of inertia, was used by the frequency of displacement of the rotor SM, located within 100 ... 400 Hz.

The speed of rotation of SM was determined by the frequency of the control pulses from the specified range. At each time interval when applying pulses of the motor shaft rotates a fixed angle. The angle of rotation is controlled by counting the number of steps (pulses).

Since in the task at hand does not require high torque of the motor, then the design scheme, we have control of the existing bipolar and unipolar configurations of windings SM was preferred unipolar. This allows for a more compact actuator, to work with smaller losses, as well as make plans to simplify the control system. In addition, unipolar SM usually have one winding in phases and from the middle of each winding concludes.

This allows you to change the direction of the magnetic field produced by winding, simply by connecting the halves of windings. Although unipolar SM control system at the outlet should have four key devices, but in general the device is simpler than the control system for a bipolar motor.

Based on these features and benefits, projected SM control system implemented on programmable logic integrated circuit. When designing the device used freely available CAD Quartus II ver.9.1, allowing to implement the project based on programmable logic integrated circuit company Altera [1].

The system design has a full cycle, and supports cross-cutting the process from input to the programming and control circuits. It is an independent architectural design environment, adaptable to the specific design requirements.

Project description file is created in a text editor package. Project digital device, implemented on the programmable logic integrated circuit produced by the language VHDL, the input language used by non-CAD.

VHDL can describe algorithms for operation of digital systems and perform a wide range of arithmetic and logical operations. In describing the operation algorithm, developed the device took into account the sequence of turning on and off power switches, thus permit the realization of the ways to control the phases of SM (total step with the inclusion of one phase, the total step with the inclusion of two phases, and half-step mode).

Fragment file software VHDL - descriptions of management systems on CPLD for the implementation of the total step mode with the inclusion of one phase SM

```
entity Main is
port(
  Clk: in bit;
  Revers: in bit;
  Load: in bit;
  StepNum: in integer range 0 to 2000;
```

```

A,B,C,D: out bit
);
end Main;

architecture Struct of Main is
signal i: integer range 0 to 3;
signal Step: integer range 0 to 2000;
signal Ena: bit;
begin
process(Clk)
begin

if (Clk'event and Clk='1') then
case i is
when 0 =>
A<=(not Revers) and Ena;
B<=Revers and Ena;
C<='0';
D<='0';
i<=i+1;

when 1 =>
A<='0';
B<='0';
C<=(not Revers) and Ena;
D<=Revers and Ena;
i<=i+1;

when 2 =>
A<=Revers and Ena;
B<=(not Revers) and Ena;
C<='0';
D<='0';
i<=i+1;

when 3 =>
A<='0';
B<='0';
C<=Revers and Ena;
D<=(not Revers) and Ena;
i<=0;

end case;
end if;
end process;
end case;

```

After debugging the circuit components on the basis of established when compiling the output files, simulation work carried out projects with the subsystem (Simulator) package Quar-tus II ver.9.1.

It tested the internal time relations projects. Compilation made with the defined requirements: ensuring the temporal characteristics of projects, optimization of resources used CPLD.

As a result of the compilation of files created for programming and configuring the CPLD Altera, allowing to use full step and half step modes of management phases SM.

Fig. 1 shows a functional circuit that realizes full step mode with the inclusion of one phase.

When compiling the projects selected CPLD MAX7000S, device EPM7064SLC44-5, which has 64 logic elements [5].

In CPLD MAX7000S realized one of the above-mentioned control circuit stepper motor. Percentage of selected CPLD in the implementation of each of the three control schemes, respectively, was 74, 75 and 77.

Functional diagram of control systems, realizing full step mode with the inclusion of one phase of SM control is shown in Fig. 1.

The scheme consists of multiplexers MUX1 - MUX5, adder ADDER, blocks D-flip-flops DFF1 and DFF2, multi-block key elements of the Main, D-flip-flops DFF3 ... DFF7, scaler pulses CDF.

Scheme of control system on CPLD works as follows. The target number of steps (pulses) in the parallel code is fed to the inputs of multi-block key elements of the signal Main StepNumber [10 ... 0]. Maximum number of steps required for a particular device is introduced at the signal 11h7FE input to the adder ADDER.

The circuit elements including blocks of MUX1, ADDER, Main, DFF1 and DFF2, the passing of the necessary number of pulses that matches their values, the inputs of the multiplexers MUX2 - MUX5 and triggers DFF4 ... DFF7, which in turn provide a time shift of pulses at the outputs A, B, C and D schemes. As a result, full step mode is realized with the inclusion of one phase SM.

Start control system implemented on a signal fed to Load, from process control system, which uses an electronic expansion valve.

Right direction of the motor supply signal is given by "0" input Revers. To change the direction of rotation of the engine should give a signal "1" on the same input.

Fig. 2 represented a functional circuit that realizes full step mode with the inclusion of two phases.

Fig. 3 shows a functional diagram presented at half step mode.

### 3 RESULTS OF EXPERIMENTAL STUDIES

Simulation results management system SM, sold, given the potential CPLD, in full step mode, with the inclusion of one phase and the forward direction of rotation of the rotor are shown in Fig. 4 and 5.

Simulation results management system SM, sold, given the potential CPLD, in full step mode, with the inclusion of the two phases are shown in Fig. 6 and 7.

Fig. 8 and 9 are timing diagrams at half step. The results of modeling work developed by the three stepper motor control systems have made in the CPLD affirm the circuit in full accordance with the presentation of inferior quality. These timing diagrams were obtained at a frequency of control pulses at 200 Hz.



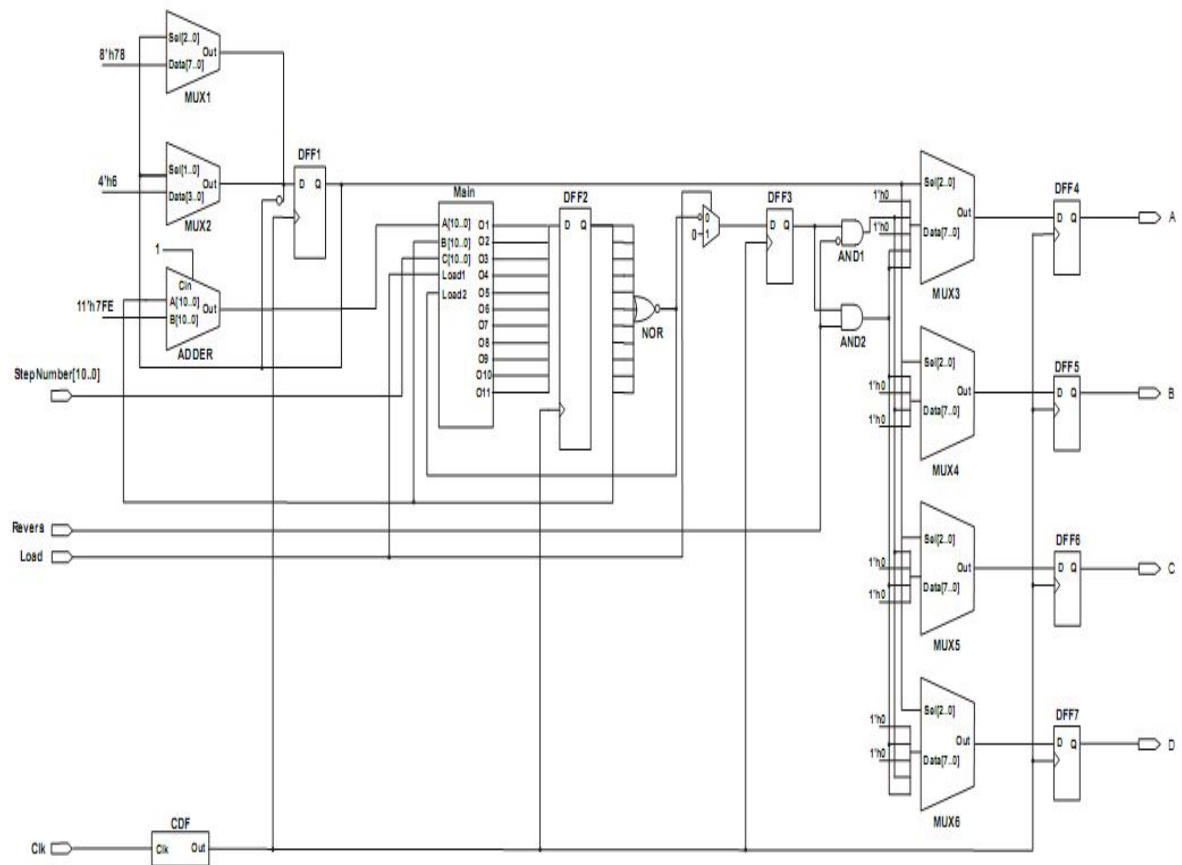


Fig.3. Functional control scheme at half step SM

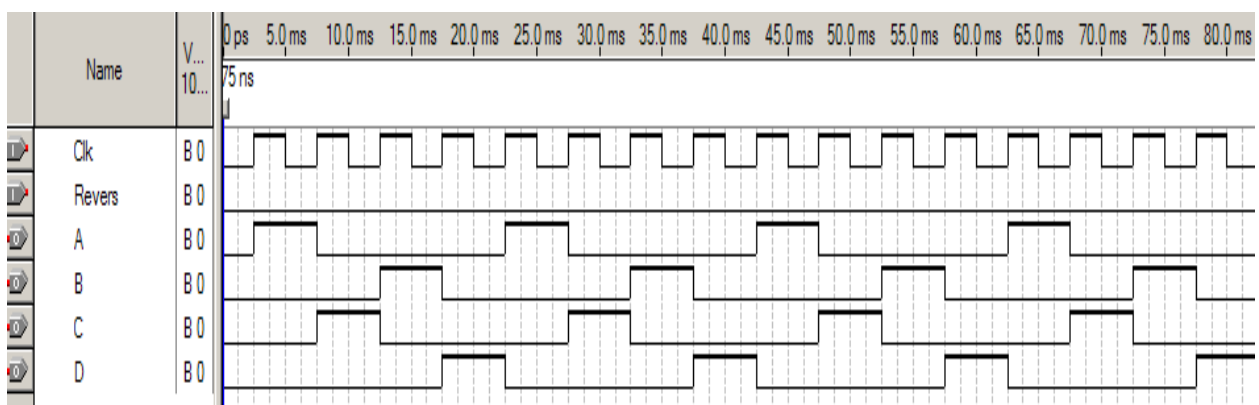


Fig.4. The simulation results management system SM with full step mode, with the inclusion of one phase and the forward direction of rotation of the rotor

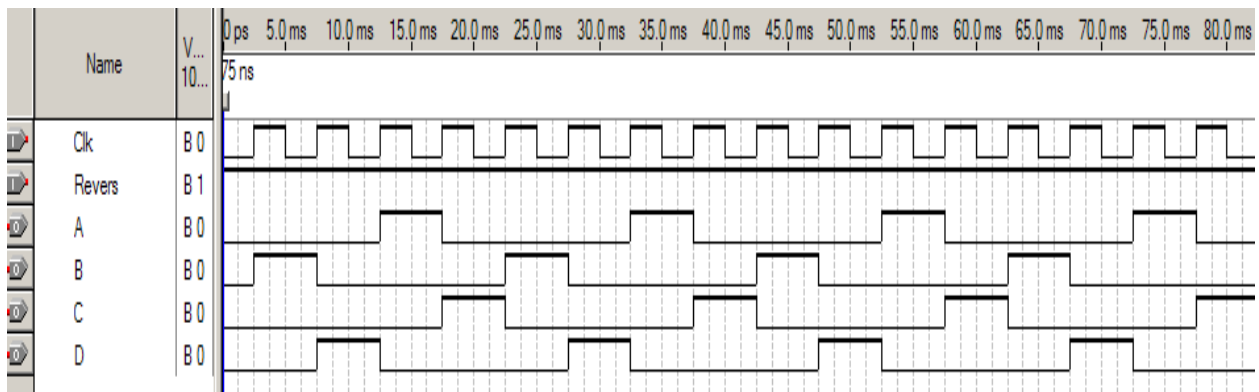


Fig.5. Simulation results management system SM with full step mode, with the inclusion of one phase and the reverse direction of rotation of the rotor

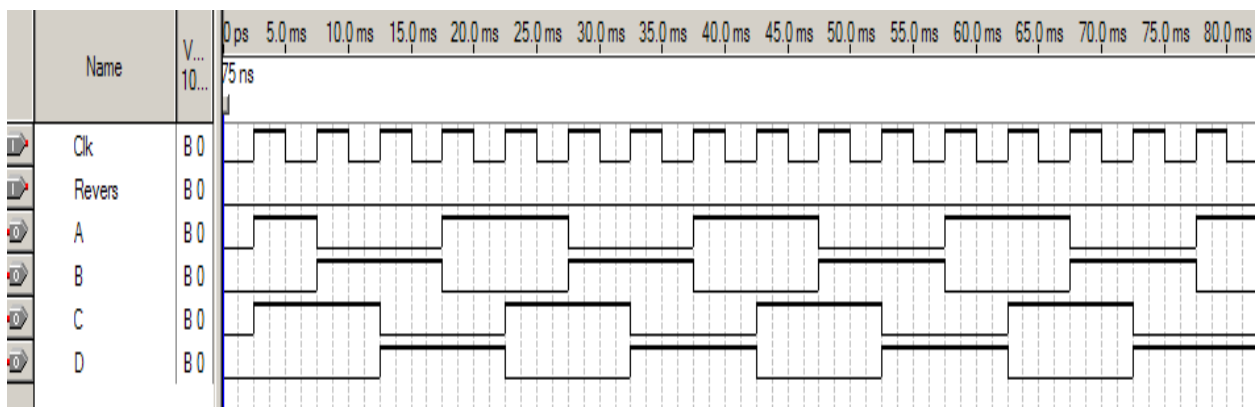


Fig.6. Simulation results of control SM with the inclusion of two phases and the forward direction of rotation of the rotor

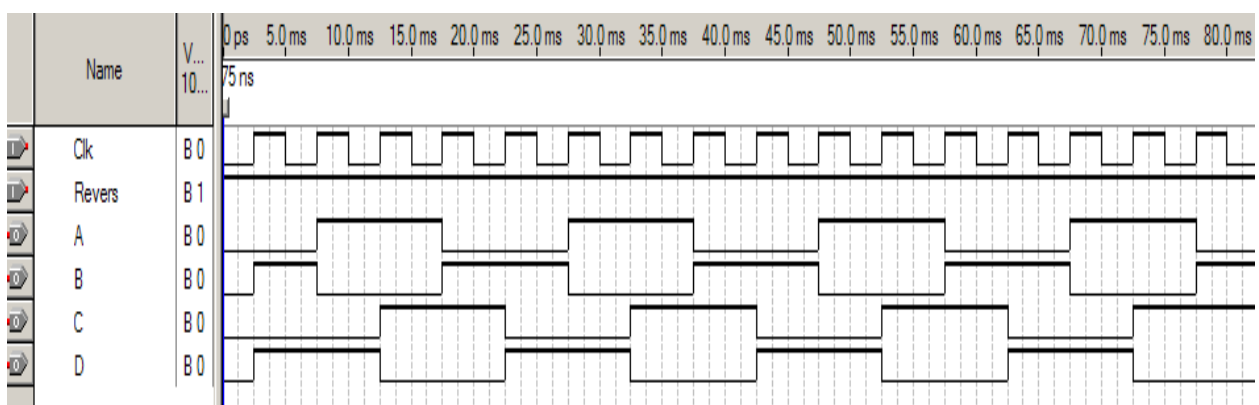


Fig.7. Simulation results of control SM with the inclusion of two phases and the reverse direction of rotation of the rotor

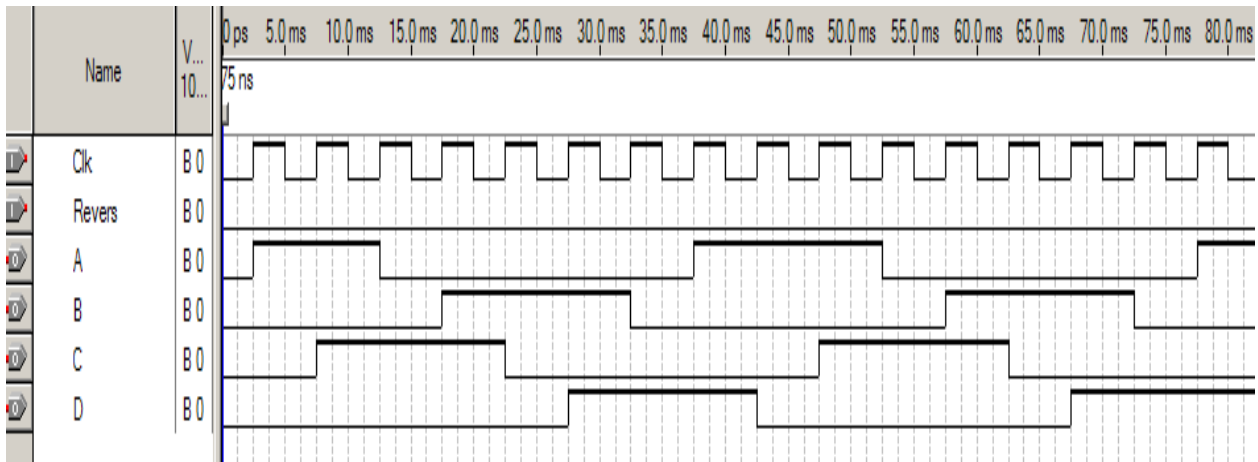


Fig.8. Simulation results management system SM at half stepping mode and the forward direction of rotation of the rotor

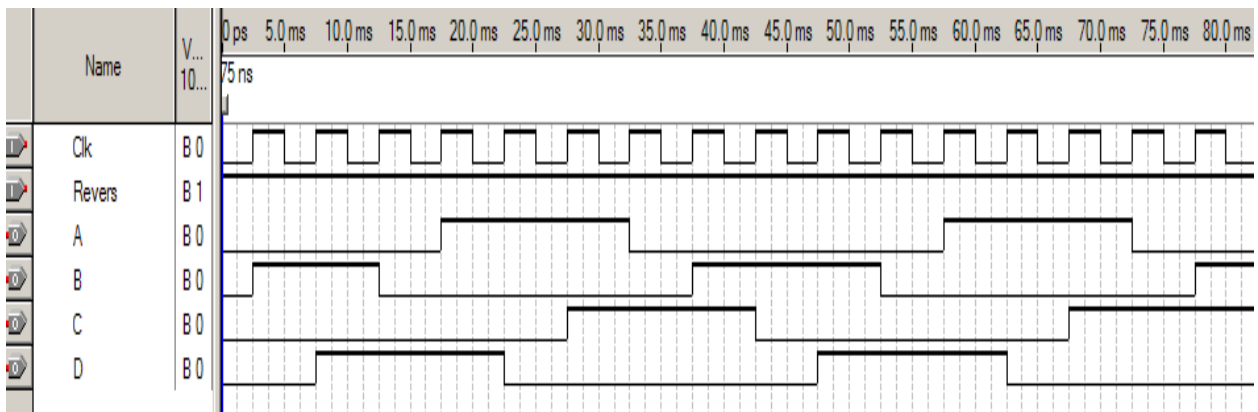


Fig.9. Simulation results management system SM at half stepping mode and the reverse direction of rotation of the rotor

#### 4 PRACTICAL IMPLEMENTATION OF MANAGEMENT

To implement any of the three schemes of impulse control phases of SM, a principle electrical circuit device shown in Fig. 10 DD1-clock generator. For switching the motor windings using transistor switches open collector constituent circuits DD3).

Circuit consists of transistor pairs with high-voltage outputs with common cathode coupling diodes for switching inductive loads. Output current of each transistor pair in the limit is 500 mA. Power chosen by SM is limited to a maximum current through a single

key and the hardware the total power dissipated chip DD3. All pins are fitted with internal diodes, ie each half winding SM (Fig. 10) shunted diode, eliminating switching voltage peaks.

Transistor switches DD3 provide amplification and conclusions CPLD protection against possible infiltration voltage SM.

As the SM (Fig. 10) is selected motor rated for 12V, the current phase of 400 mA and has a torque of  $1.60 \text{ kg} \cdot \text{cm}$ , moment of inertia of  $30 \text{ kg} \cdot \text{cm}^2$ , angle step 7.5 degrees. Reversible motor control is given logical level signals, switching the FF and FB (Fig. 10).

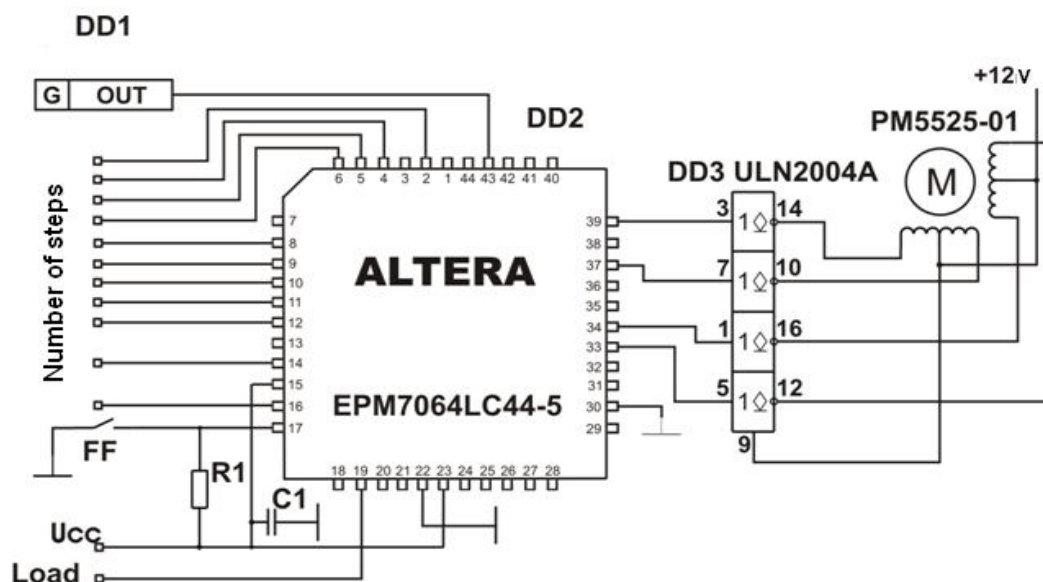


Fig.10. Schematic diagram of electrical control system SM

#### 4 CONCLUSIONS

Using the results obtained for simulation of control systems SM, will conduct a comparative analysis of used methods of management. Figure 4 and 5 are timing diagrams of control system on CPLD total step in the implementation of the regime with the inclusion of one phase. When using this control method provides for alternate switching phases SM.

For a selected unipolar SM in this case in the same time using 25% of windings. In addition, such management can not be made full time, and the equilibrium point of the rotor for each step coincides with the "natural" equilibrium point of the rotor in the absence of power the engine. In managing the phases of the SM with overlap, when two phases are included in the same time (Fig. 6 and 7), the rotor is fixed in the intermediate positions between the poles of the stator. This ensures that approximately 40% more time than in the case of one phase included.

The second control method provides the same step angle as the first method, but the position of equilibrium points of the rotor is shifted by half a step. Figure 8 and 9 shows the results of modeling management system SM, operating at half-stepping mode. This control method is a combination of the total step with the inclusion of one phase and the total step with the inclusion of the two phases of management. In this case, every second step SM powered only one phase, while in other cases, powered two. As a result, the angular displacement of the rotor angle is one-half step to full step ways to control. In addition to reducing step, this method of control compared with full-stepper can partially get rid of the phenomenon of resonance, and also has the advantage of a higher resolution.

The method does not require the formation of the stepped supply current windings SM. Despite the fact that the developed control system SM implements three methods of control, preference should be given half-stepper mode of operation of the engine.

The developed scheme of direct impulse control SM using a programmable logic integrated circuit with slight modifications can be used in a variety of destinations devices inertia and precise actuators in robotics, in the electronic industry, medical engineering, etc.

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