IMPLEMENTATION OF H BRIDGE INVERTER BASED DVR USING ATMEL MICROCONTROLLER 89C2051

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Abstract—Among the various power quality problems, the voltage sags, are attracting a large amount of attention of researchers from industry. Dynamic Voltage Restorer(DVR) gives the solution to the above mentioned problem. The main function of DVR is to mitigate the voltage sag. It controls voltage applied to the load by injecting voltage of compensating amplitude, frequency and phase angle to the distribution line. The DVR is primarily responsible for restoring the quality of voltage delivered to the end user when the voltage from the source is not appropriate to be used for sensitive loads. Usage of DVR enables consumers to isolate and protect themselves from transients and disturbances caused- by sags. DVR is simulated using Matlab and it is implemented using microcontroller 89C2051. The experimental results are compared with the simulation results

Index Terms— DVR, Matlab, Microcontroller 89C2051

I. INTRODUCTION

With the rapid technology advancements in industrial control processes, electric utilities are experiencing more demanding requirements on the power quality from the large industrial power consumers. Such power quality problems have been better appreciated when the price paid due to the economic losses caused by them is large. These concerns are reflected in the newer versions of power quality standards, such as IEEE 1159-1995 [1] and IEC6100-4-30 [2]. Trends of deregulation happening in Europe and America exert pressures on the utilities to accommodate such demanding requirements in a competitive electricity market environment.

Among the various power quality problems, the voltage sag, usually resulting from the faults on parallel transmission/distribution feeders, is attracting quite a large amount of attention of researchers from both industry and academia [3]-[5]. A definitive solution to this problem at large power levels has been commonly called dynamic voltage restorer (DVR), under the rubric of the custom power concept introduced by EPRI [6]. The main function of DVR is to mitigate the voltage sag, although sometimes, additional functions such as harmonic compensation and reactive power compensation are also integrated to the device. It has also been shown in a previous study that the series compensation device such as the DVR as shown in Fig. 1(a) is preferred over shunt compensation strategy as shown in Fig. 1(b) for stiff systems [7], typical of large industrial load installations. Much of the published literature on DVRs deal with a voltage source converter (VSC) realized using two-level converters, which are well suited for 480-V systems [8], [9]. While in high power applications such as at distribution voltage levels, a multilevel converter is a more attractive solution, whose application in a DVR has not been well addressed. On the other hand, for the control of DVR, the open loop feed-forward technique is found to be a common practice, which generally results in poor damping of the output harmonic filter [10]. In the literatures [1] to [10], the implementation details of DVR using Atmel microcontroller are not available. In this paper, the hardware implementation details using embedded microcontroller are presented. The paper is organized as follows. The power architecture is introduced in Section II followed by simulation results in Section III. The experimental results are given in section IV.

II. POWER ARCHITECTURE

Although various topologies may be used to realize the VSC illustrated in Fig. 1, at higher power levels cascaded H-bridge multilevel power conveners are seen to have advantages in several aspects [11], [12]. First, multilevel converters can realize the higher power and high voltage using semiconductor switches of relative small ratings while avoiding the voltage sharing and current sharing problems associated with series and parallel connection of switches commonly employed in two-level converter realization. Second, multilevel converters can synthesize the output voltage with smaller steps and reduced harmonic content, while potentially resulting in smaller dv/dt thus lower electromagnetic interference (EMI). Third, compared with diode clamped multilevel topology, the H-bridge cascaded structure can avoid unequal device rating and unbalanced dc link voltage problems. Compared to flying-capacitor topology, the H-bridge cascaded multi-level converter has less storage capacitors and

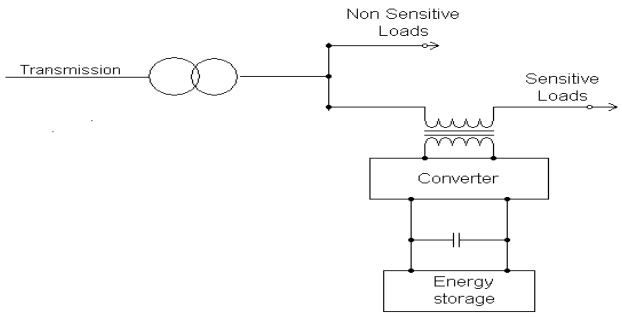

Fig 1a

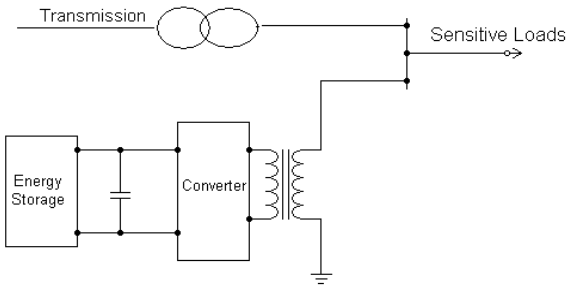

Fig. 1.b

Fig. 1 Interconnection schematic of (a) series and (b) shunt compensation configurations for power quality improvement

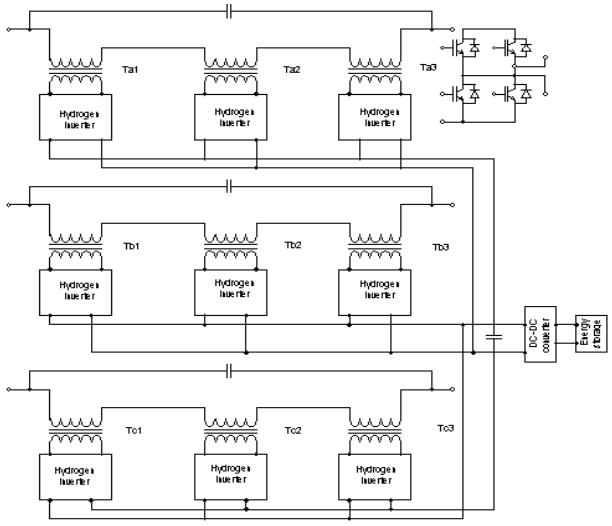

Fig. 2 Power architecture of the transformer coupled H-bridge converter applied to DVR.

requires simpler control [13]. Finally, it is worth noting that the modularity nature of the H-bridge cascaded multilevel converter makes an easier realization.

The proposed power architecture of the transformer coupled H-bridge converter is illustrated in Fig. 2. Each phase is composed of three H-bridge inverters. The AC outputs of the converters are connected in series through transformers. This architecture fits squarely with the DVR application, which necessarily involves a series injection of the compensating voltage source. Use of the transformers here allow for voltage matching, isolation, series injection and multilevel waveform synthesis simultaneously. Furthermore, instead of using isolated DC link for each H-bridge inverter, a common DC link bus connects all the nine H-bridge inverter DC ports in parallel. This is different from the conventional H-bridge cascaded multilevel converter [13]. This is also different from the multi-pulse converter which includes multiple six-pulse three-phase converters [14]. Compared to the transformer-less realisation of the DVR with the conventional H-bridge cascaded multilevel converter [15]-[17], the Common DC Bus (CDCB) structure significantly simplifies the energy management on the DC side while retaining all the other good features of the multilevel converter, such as high quality waveforms, low EMI and evenly load-sharing among semiconductor switches, etc..

Furthermore, CDCB structure reduces the low frequency DC link ripple current due to the phase shift between the three phases and high frequency ripple currents resulting from switching harmonics cancelled due to the carrier phase shift. The three transformers in each phase could be one transformer with three secondary windings, which is a preferred approach since the switching harmonics cancellation will reduce the core loss. However, to keep the modularity of the design, a separate injection transformer is used for each H-bridge.As seen in Fig.2, the primary side of the injection transformer carries the rated load current. The voltage rating of the transformer depends on the grid voltage level and the depth of the voltage sag required to compensate. So the rated current multiplied by the injection voltage level gives the VA rating of each phase. The phase VA rating divided by the number of series connected module is the rating for one module. The number of series connected modules is an additional degree of freedom that may be chosen to fulfill other requirements. The turns ratio of the transformer is determined by the available voltage and current rating of semiconductor switches for a given VA rating. The filter capacitor can be sized based on the leakage inductance of the transformer such that the cut off frequency of the LC filter is about a decade below the switching frequency.

Depending on the load condition, mainly the power factor, two different compensation strategies may be applied, Zero Active Power compensation (ZAP) and Minimum Active Power compensation (MAP) [7]. Under ZAP condition, the converter injects purely reactive component of voltage to maintain regulation. When the load and line conditions preclude ZAP operation, the MAP strategy is invoked. Under MAP condition, the DC link voltage will be controlled by drawing energy from the storage. The two different compensation strategies can be realized by varying the relative phase angle between the grid voltage space vector and injection voltage space vector. For resistive load, the only choice is MAP, which results in injected voltage exactly in phase with grid positive sequence

voltage. Under this operating condition, the rating of the energy storage is based on the VA rating and duration of the sag for a unity power factor load.
The mathematical equations are as follow,

$$V_{o(Avg)} = E(1-2\delta/T)$$
$$V_{o(RMS)} = E\sqrt{(1-2\delta/T)}$$

Where,
$V_{o(Avg)}$ – Average output voltage,
$V_{o(RMS)}$ – RMS output voltage,
δ – Dead time; T– Time period

The control input to the inverter is the switching signal. In the output of the inverter, the pulse width can be controlled

III .SIMULATION RESULTS

The circuit model for DVR system is shown in Fig. 3.a. The Fig. 3.a shows the line compensation circuit with additional ac source. During normal conditions, there is normal flow of current through load-1 and breaker-3 is closed.When breaker-2 is closed an extra load is added to and voltage sag occurs. At this point breaker-1 closes and breaker-3 opens and allows additional AC source to inject voltage. The Fig.3.b shows the voltages across transformer primary. The voltages across loads 1 and 2 are shown in Fig. 3c. The Fig.4.a shows the line compensation with DVR circuit. The DVR model is shown in Fig. 4.b. The DVR system has four MOSFETs. The driving pulses are produced by AT89C2051 microcontroller. The LC filter is added with DVR to get better output. The Fig. 4c shows the DVR circuit with LC filter. The Fig.4d and Fig. 4e show the voltage across external source and compensated voltage across load-1 and load-2 without and with filter respectively. From this figure it can be seen that proper voltage is injected to improve the voltage profile.

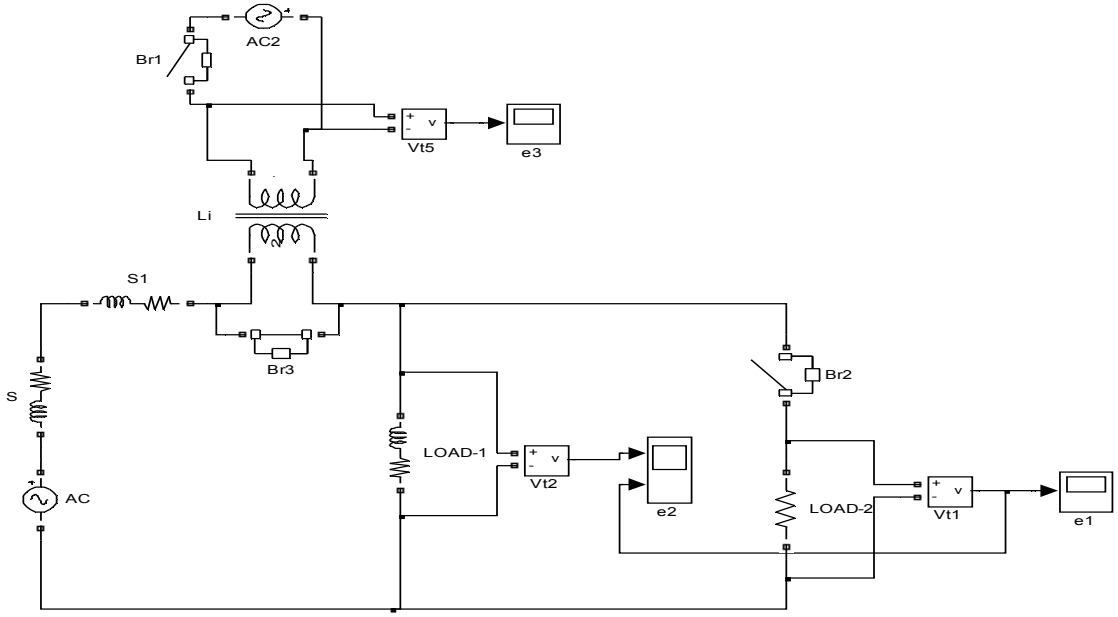

Fig.3a. Line compensation circuit with additional AC source

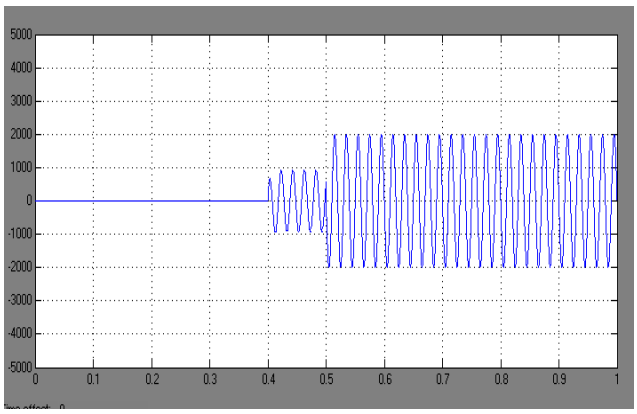

Fig. 3b Voltage across transformer primary

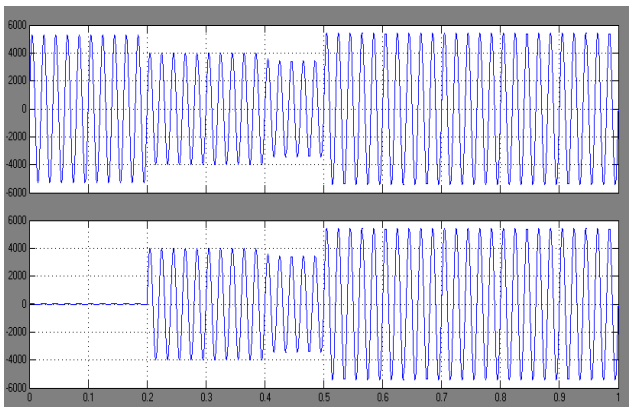

Fig. 3c Voltage across load -1 and load-2

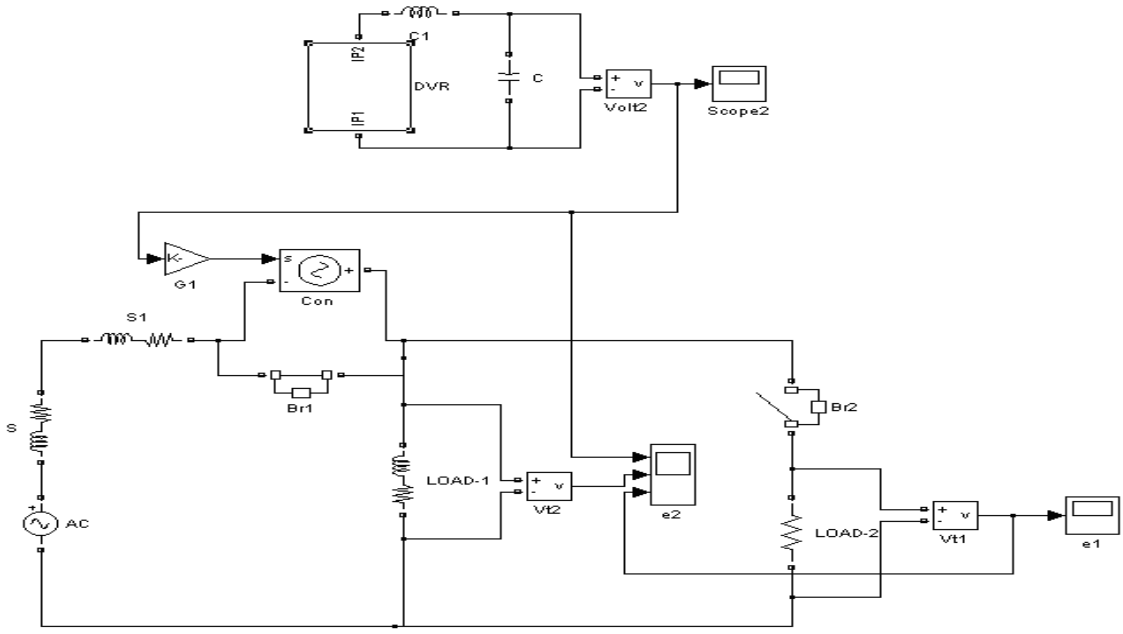

Fig. 4a Line compensation circuit with DVR circuit

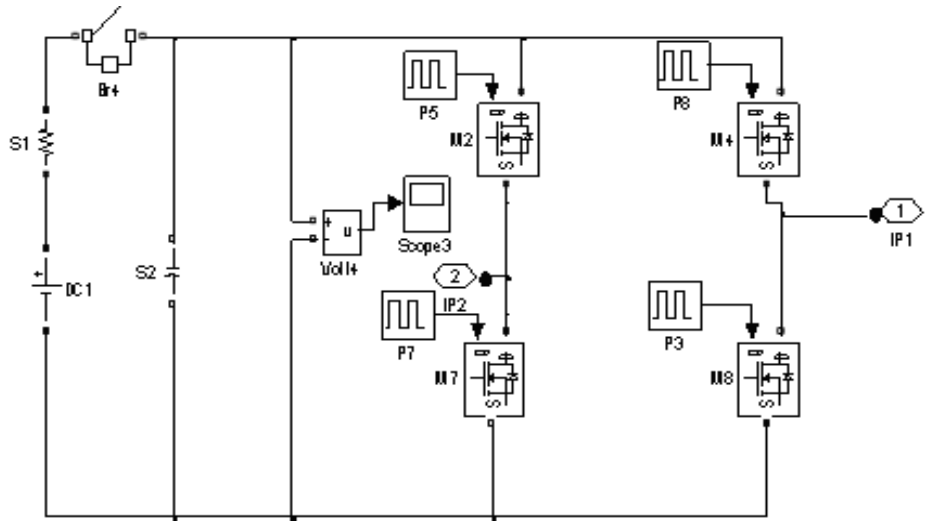

Fig. 4b Sub system

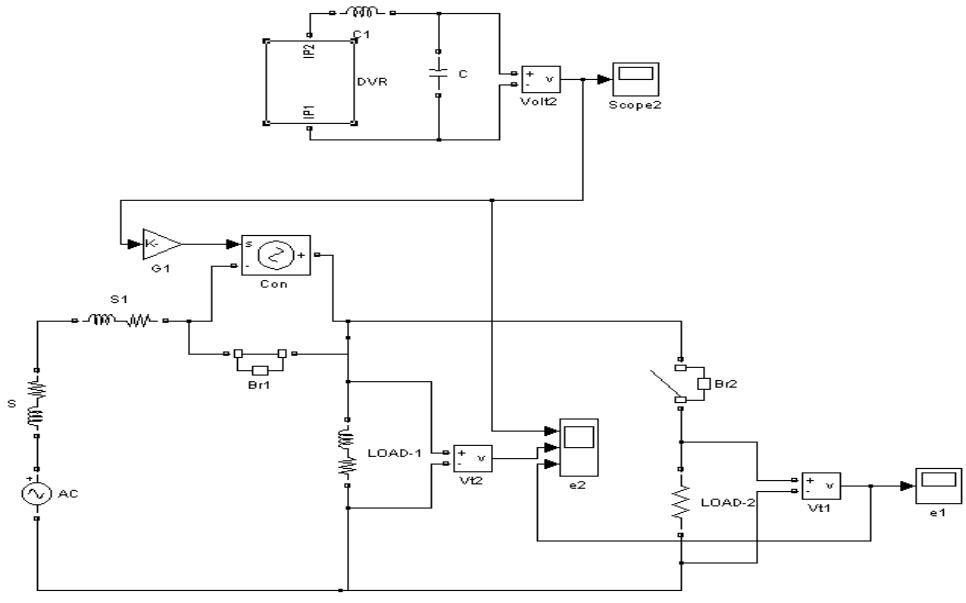

Fig. 4c DVR with LC filter

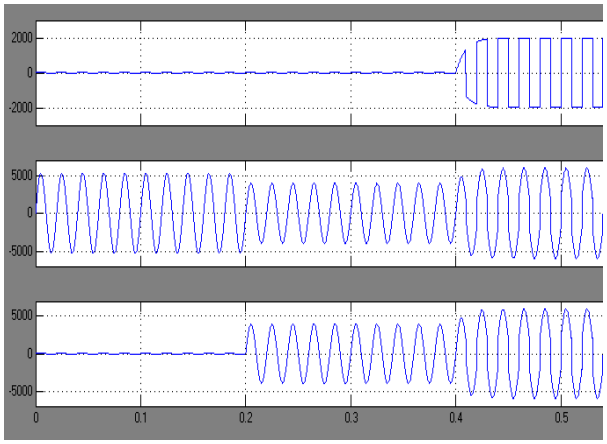

Fig.4d Voltage waveforms across external source, load-1 & load-2 without filter

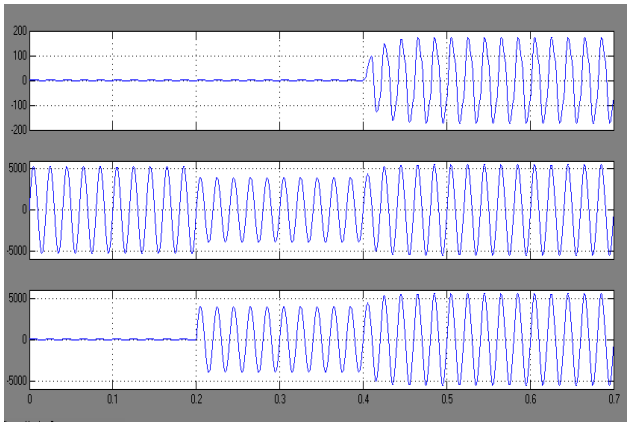

Fig. 4e Voltage wave forms across external source, load-1& load-2 with filter

IV. EXPERIMENTAL RESULTS

A 1kW Laboratory model is fabricated and the hardware is tested. The pulses are generated using the microcontroller Atmel 89c2051. Top view of the hardware is shown in Fig. 5a. Pulses from microcontroller are shown in Fig. 5b. These pulses are amplified using the driver IC 2110. The amplified pulses from the driver are shown in Fig. 5c. The output voltage of inverter is shown in Fig.5d. The harmonics are filtered using LC filter and the output of the DVR is shown in Fig.5e. Microcontroller based control circuit is shown in Fig.5f

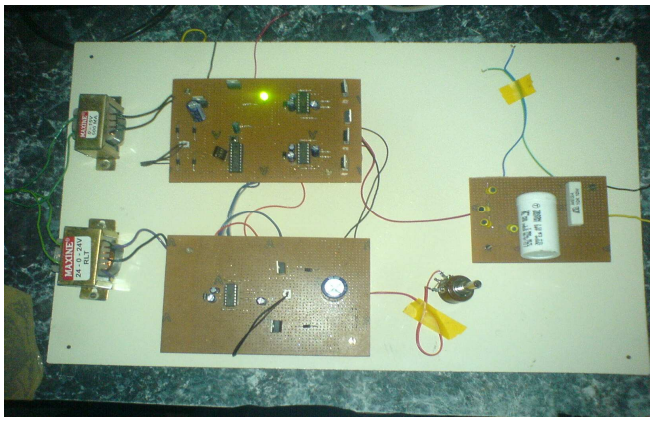

Fig.5a Top view of the hardware

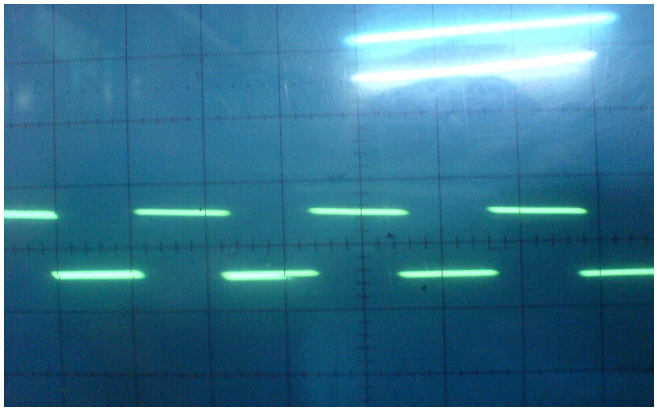

Fig. 5b Pulses from microcontroller

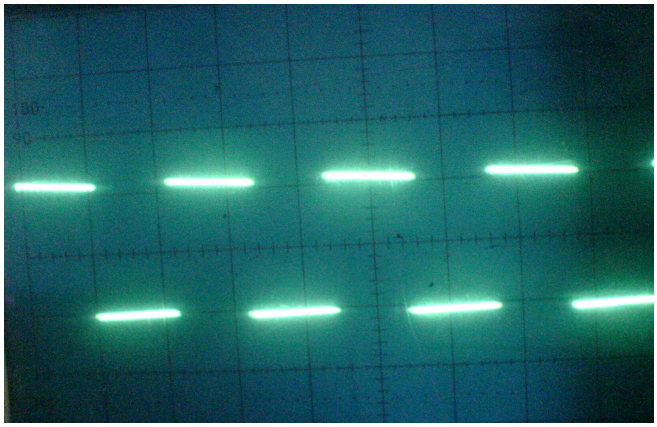

Fig.5c Amplified pulses from the driver IC 2110

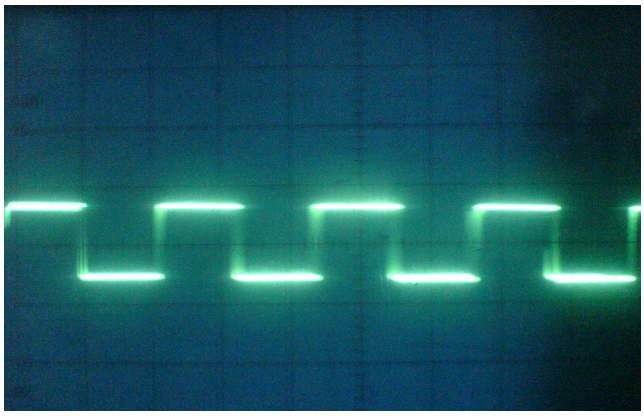

Fig. 5d The output voltage of inverter without filter

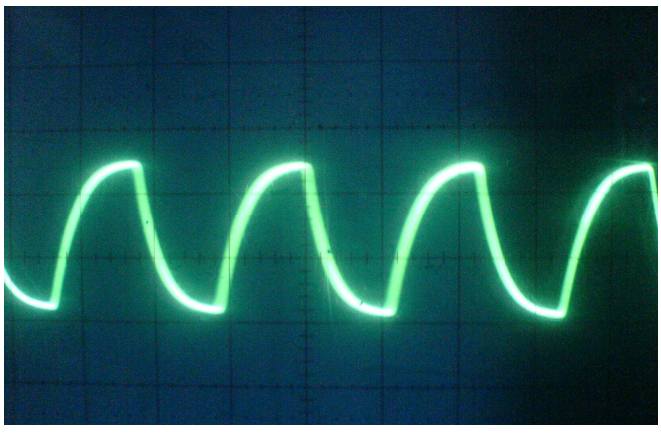

Fig. 5e The output voltage of DVR with LC filter

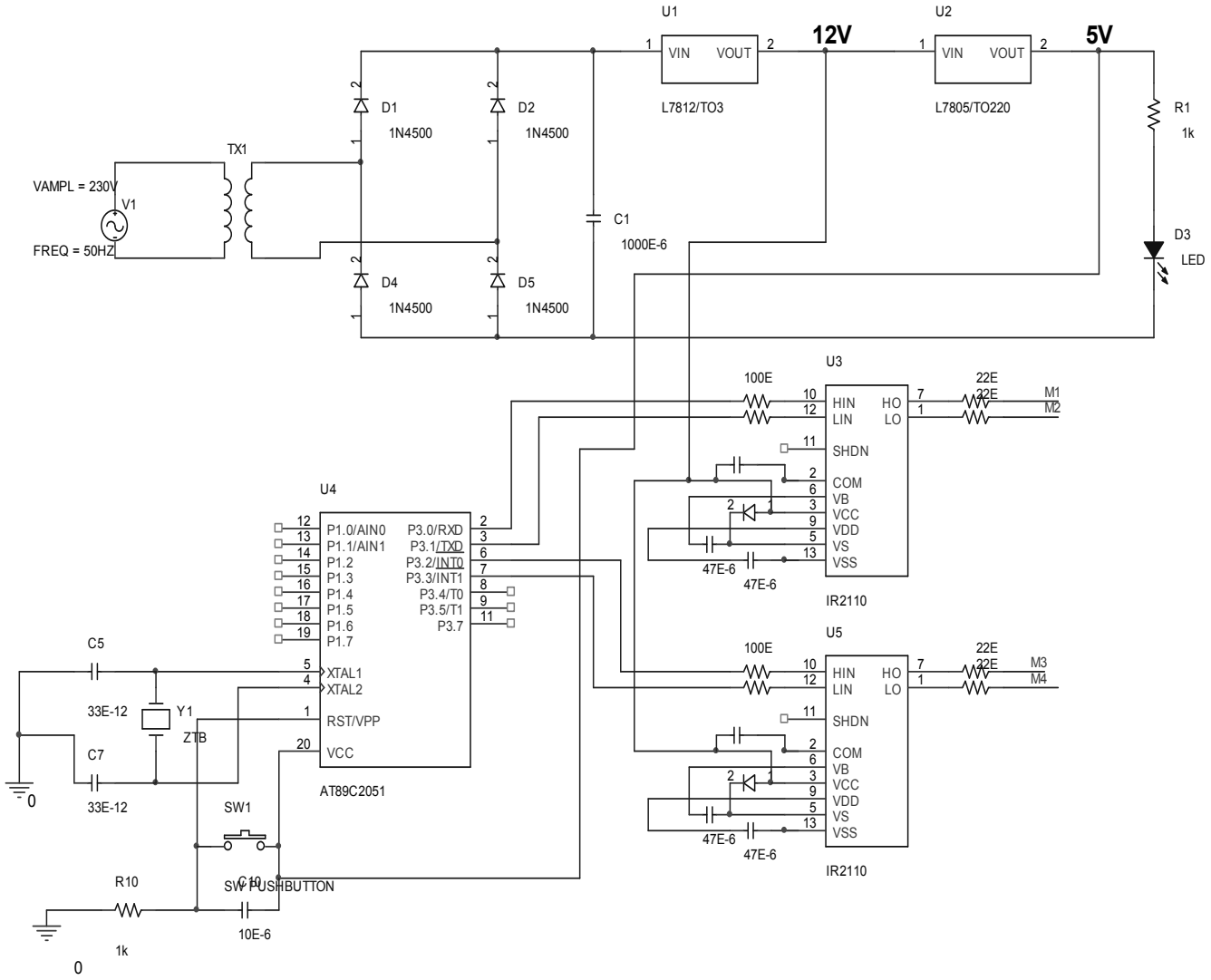

Fig. 5f Microcontroller based control circuit

V.CONCLUSION

The Dynamic Voltage Restorer (DVR) is used to improve voltage sags caused by abrupt increase in loads. The DVR reduces losses associated with irregularities in the production process resulting from power disturbances. DVRs tackle the problem of harmonics caused by non-linear load machinery in manufacturing facilities. The insulation wear on transformers, motors and drivers caused by power irregularities is also reduced by DVR. Therefore most industries use DVR which compensates voltage sag especially at sensitive loads by injecting an appropriate voltage through an injection transformer. The hardware is implemented using an embedded microcontroller and the results are presented. The experimental results closely agree with the simulation results.

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