

Simulation of a Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources Arranged in Matrix Structure

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Abstract: This paper analysis an improved topology of a cascaded multilevel inverter (CMLI) that utilizes less switch count topological structure than that of conventional topology. So with the reduced number of switches, the topological structures is designed by the mould of a matrix for a CMLI. As the numbers of switches are depleted in the conduction path, so both the switching as well as conduction losses are reduced, lower input current distortion and electromagnetic interference are also reduced. Therefore it assists for the higher efficiency of the converter. The propound inverter focus extends the outstretch to produces different number of output voltage levels from the congruent topology, there where it uses the same number of the voltage source and very less number of switches when compared to the conventional inverters. Thus the desired operation of the power modules and firing pulses are generated by the annex pulse width modulation (PWM) techniques strategy. And its changes in the harmonic spectrum will be analyzed. The converter will be modeled with the assist of MATLAB/SIMULINK.

Key words—Matrix structure, CMLI, Level Shifted Carrier PWM, Reduced switch count topology.

1. Introduction

The work of Multilevel inverters (MLIs) during the crisp years have paid a great acknowledgment to a snazzy kind of power converter. The approach to the MLI is done by a consistent switching, thus which can provide a stepped output voltage waveform with low harmonic distortion. The mode of multi voltage source inverter in the medium power voltage application provides of a charge effectiveness amalgamation in the management market [4].

In this converters we can regard capacitors, batteries and renewable energy voltage sources as the multiple DC voltage sources, so these converters can be widely used in power generations, water plants, power quality devices, marine propulsion, liquefied natural gas and energy transmissions. The several DC sources as a input synthesizes a desired output voltage by using MLI as a power interface. This multiple DC sources are aggregate by the commutation of

power switches in verdict to achieve steep voltage at the output.

When contrast to the conventional two level inverters there are diverse advantages for MLI, so these are commonly used for high voltage and high power applications which leads to the reduction in T.H.D [2]. MLI are having the ability to perform power conversion by exploiting the multiple small voltage levels. The content of harmonic at the output voltage is depleted, similarly the filter becomes smaller and cheaper making the system compact when compared to the two level inverters. Moreover these are having lower switching losses, good electromagnetic compatibility, improved power quality, lower electromagnetic interferences than the two level inverters.

There exists the three commercial conventional multilevel voltage source inverters includes [4]: a) diode clamped multilevel converter (DCMLC), b) flying capacitor multilevel converter (FCMLC), and c) cascaded multilevel converter (CMLC) [1-3]. Among these topologies, CMLI having the higher output voltage, less voltage stress, power, and reliability due to modular topology. One aspect which provide the difference between the CMLI and other MLI is, CMLI utilizing the different DC source voltages for the each H-bridges which consequential in dividing the power conversions between H-bridges and output of each bridge are connected in series to obtain stepwise output voltage. CMLI are the most popularly enact topologies in the evolve technological field of the renewable energy [5].

Unfortunately the evaluation tales out that the MLI are having various disadvantages. One of the most conspicuous disadvantages is it utilizes the abundant number of power semiconductor switches are required. The size of overall circuit and the complexity increases because a protection circuit and a gate driver is required for every switch requires. Thus which leads to the general system to be more costly and difficult. Therefore in the practical realization it elucidate sketch a path for declining the utilization of power

switches and gate driver in each cycle of operation to accrue the deliberate level of output load voltage [6-12]. In recent years several number of MLI topologies are presented with reduced number of switches and gate drivers.

This primarily presents the state-of-the-art of a MLI topology. The new topology circumscribes of symmetrical single phase symmetrical CMLI to evolve, where voltage sources are arranged in the matrix and connect in reverse to make easy the synthesis different output load voltage levels. The projected CMLI topology has reduced switch count/gate driver for 'm' level, but it offers same number of DC sources for higher number of steps in the output [13-17]. It espouse to denigrate the related circuitry and less number of power conducting devices are used in each current transmission path to adore the proficient function of power circuitry. To accredit the validity of the new approach towards the proposed MLI by the general level shifted multicarrier, In phase disposition (IPD) to drive the inverter and lucid in the simulation.

2. Conventional CMLI

The topology of the CMLI is provided by series connection of single phase inverter with separate DC sources. The typical single phase 5-level CMLI has shown Fig.1 below. The addition of voltage generated by the different cells is the synthesized resulting phase voltage. The 3-level CMLI is nothing but a H-bridge inverter which generates the output as the three level voltage. By adding the every module to the cascade the inverter will produce two more levels in the output voltage. So the resulting output AC voltage for 5-level swings from -2Vdc to +2Vdc and we can observe here it requires 8 switches. For 7-level resulting output AC voltage it swing between -3Vdc to + 3Vdc. Similarly for 9-level inverter resulting output AC voltage swing from -4Vdc to +4Vdc it uses 16 switches, whereas the proposed model uses only 12 switches. Comparing the conventional CMLI with the proposed we are going to use less number of switches. In order to produce the 9-level output voltage we are using just 12 switches in proposed topology. Thus by using the 12 switches we can obtain the 9-level AC output voltage in the proposed topology.

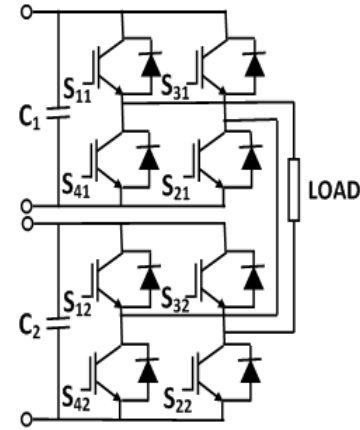


Fig.1. Typical 5-level CMLI circuit.

3. Proposed Topology

When differentiate the existing topology with the proposed topology it is simple in design. The main abstraction is to offer various levels of output voltages by erupting up with a generalized arrangement for a single phase CMLI. In this structure a key philosophy involves where the power switches are arranged in the form of a matrix structure (axb) and the arrangement of voltage sources in order to obtain different output levels.

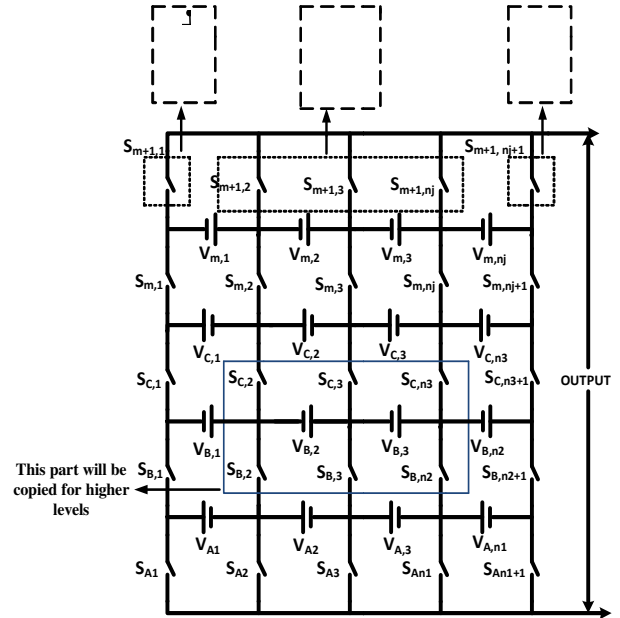


Fig.2. Generalized structure

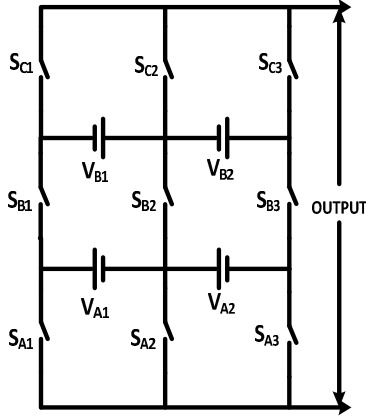


Fig.3. Proposed nine level topology

The generalized structure shown in Fig.2 Quaff voltage sources ($V_{A,1}$ - $V_{A,n,1}$), ($V_{B,1}$ - $V_{B,n,2}$), ($V_{C,1}$ - $V_{C,n,3}$), ($V_{m,1}$ - $V_{m,n,j}$) arranged in each row, thus arranged voltage sources are isolated with each other and these are connected in sequence in the design used for energy storage devices or photovoltaic cells or fuel cells in renewable energy sources [11-14]. This several isolated dc sources can simply be accouter. The architecture contains the switches in the matrix, the front line switches ($S_{A,1}$ - $S_{A,n,1+1}$), ($S_{m+1,1}$ - $S_{m+1,n,j+1}$) encompasses the top and base of the circuit and voltage sources are connect to the load by the intermediate switches (S_{B1} - $S_{B,n,2+1}$), (S_{C1} - $S_{C,n,3+1}$), (S_{m1} - $S_{m,n,j+1}$). With four isolated dc sources in schematic of nine level inverter topology has shown in the Fig.3. Where it uses only 12 switches to produce the nine level when compare to the usual topology. For the sense to generate the output voltage of (V_{A1} and V_{A2}) we need to conduct (S_{A1} , S_{B1} and S_{A3}). In the view of presence of the voltage source (V_{A2}) the body diode of the device (S_{A2}) will be forward biased, where it explode to create inter-looping problem. To avoid inter-looping problem we are going to use bi-directional devices. Several bi-directional configurations has been proposed, but we are using common emitter configuration in the proposed topology. So to defend the voltage source commencing the inter looping problem these are apt only in the intermediate column. In order to obtain the superior voltage levels the central stage as represented in the Fig.2 must be two folded.

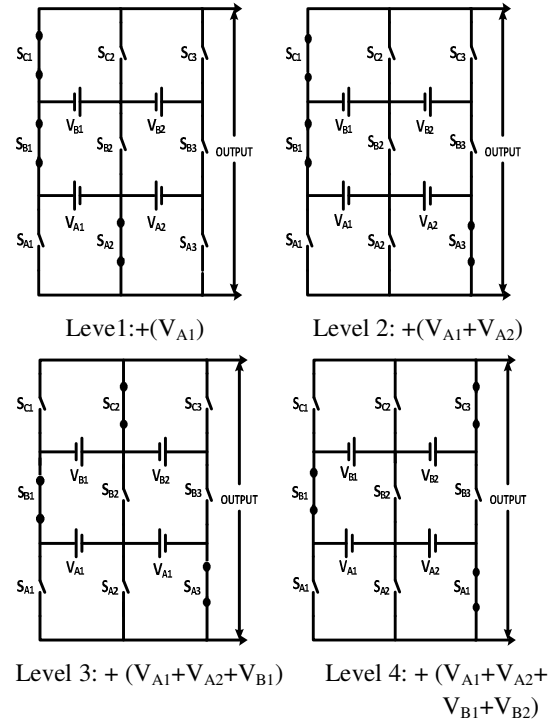


Fig.4. Operation of Positive mode

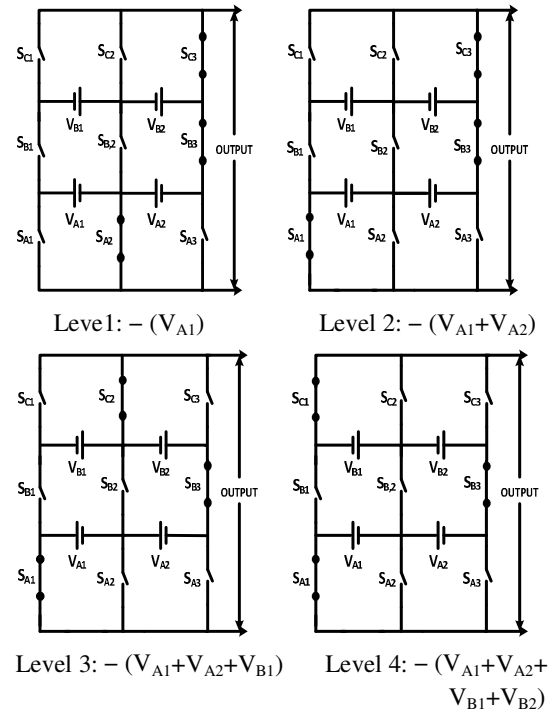


Fig.5. Operation of Negative mode

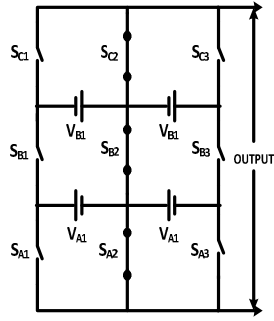


Fig.6. Operation of Zero mode

The operation modes for the proposed schematic nine level inverter topology involves three modes. This three modes of operation shown in Fig.4 to Fig.6 has subtlety in the methodology and transcend realities in the formulation. In the mode-1 in the order to obtain output voltage switches $S_{A,2}$, $S_{B,1}$, $S_{C,1}$ are on. From the Fig.4 to Fig.6 it can be clearly observe the operational pattern where the output voltage is obtained only when the three devices are switched and from this we are going to decrease the switching power dissipation due to the minimal switching transition during each mode of transfer.

Table 1. PWM signals to obtain positive level output voltage

SL.NO	PWM Signals	Positive Output Levels	Signals gated to the switches
1.	PWM 1	Positive Level 1	$S_{A,2}$, $S_{B,1}$, $S_{C,1}$
2.	PWM 2	Positive Level 2	$S_{A,3}$, $S_{B,1}$, $S_{C,1}$
3.	PWM 3	Positive Level 3	$S_{A,3}$, $S_{B,1}$, $S_{C,2}$
4.	PWM 4	Positive Level 4	$S_{A,3}$, $S_{B,1}$, $S_{C,3}$

The proposed topology arrangement when compared with conventional topologies is responsible to produce the output voltage levels in the positive and negative polarities by using the reduced number of power switches. So it required half of the conventional carrier, two sinusoidal reference signals and few power components than the conventional topology. The redundant states are chastises and pliability in the switching sequences are annotated. For the same nine level the conventional CMLI topology requires 16 power switches and to obtain required output level it uses the half of switches for current conduction path at any time of point, to render the each switching mode the proposed topology uses only three power switching during the conduction. Table 1 present how to extract different output voltage levels by using the PWM signals here it represents only for the positive output voltage, while similar arrangement are made to produce PWM single for negative cycle.

Table 2. Comparison of power components for single phase 9 level inverter between conventional topologies and proposed topologies

SL.N O.	Power Compon ents	Diode Clam ped	Flying Capaci tor	Casca ded	Propo sed
1	Main Switches	16	16	16	12
2	Main Diodes	16	16	16	12
3	Gate Drivers	16	16	16	9
4	Clampin g Diodes	56	0	0	0
5	Flying Capacito rs	0	28	0	0
6	DC-link Capacito rs	4	4	4	4
	Total	108	80	52	37

Table 3. Required power components for proposed topology for single phase and three phase

SL.NO.	Power Components	Single phase components	Three phase components
1	Main Switches	$(2 * b) * (a+1)$	$(6 * b) * (a+1)$
2	Main Diodes	$(2 * b) * (a+1)$	$(6 * b) * (a+1)$
3	Gate Drivers	$(a+1) * (b+1)$	$3 * (a+1) * (b+1)$
4	Clamping Diodes	--	--
5	Flying Capacitors	--	--
6	DC-link Capacitors	$(a * b)$	$3 * (a * b)$
7	Devices in conduction path	$(a+1)$	$3 * (a+1)$

The values in Table 2 compare the conventional and proposed topologies, requirements of the power components in order to produce the required nine level output is given by $((2 \times (a \times b)) + 1)$ level. To obtain the different levels using the proposed topology for single/three phase it ingress in Table 3 represents the requirement of number of switches in conduction path, gate drivers, power switches and DC sources thus it corroborate the merits of the proposed topology.

4. Modulation Technique

In the controlling strategy for MLI family pulse width modulation (PWM) control is most widely used method. The modulation technique used in this carrier-based PWM technique. This carrier-based scheme is generally classified into two types a) level-shifted modulation b) phase-shifted modulation. Again the level-shifted modulation is categorized into three technique i) In-phase disposition(IPD) ii) phase opposite disposition(POD) iii) alternative phase opposite disposition(APOD) the PWM used in this paper emphasis on the level-shifted IPD technique shown below Fig.7. For m-level inverter it

requires (m-1) triangular carriers, for all having the same amplitude and frequency where all carrier are in phase with each other [20-21]. The reference waveform is a sinusoidal wave in our case. By controlling the reference wave the amplitude of the phase voltage can be varied. To generate the wave form pulses for upper sequences the reference signal must be greater than all carriers. Similarly To generate the wave form pulses for lower sequences the reference signal must be lower than all carriers. In order to switched to zero level reference must be lower than the upper carrier but greater than the lower carrier waveform. In power circuit logical function has been used for proper turn on of the switches.

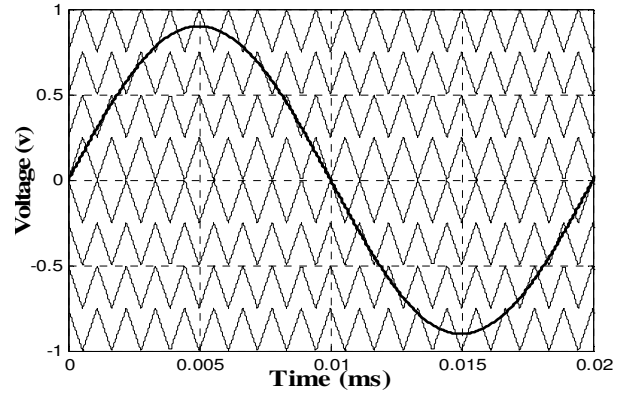
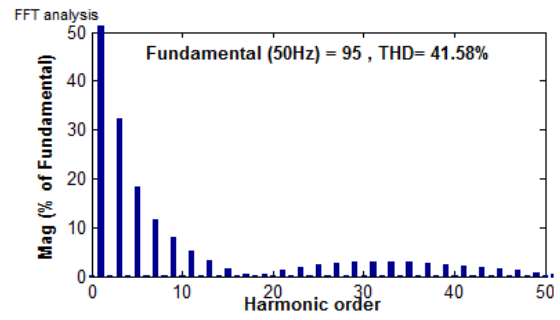
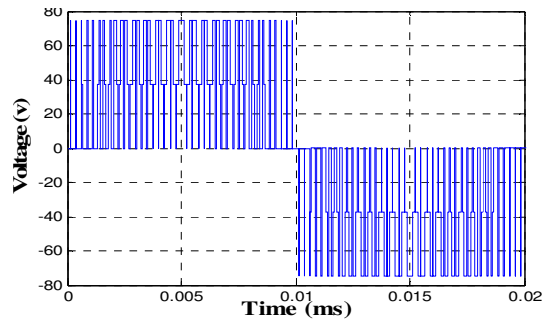


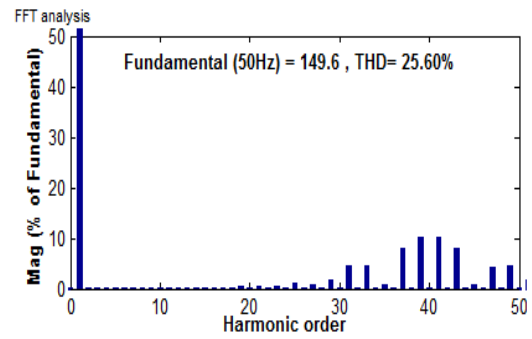
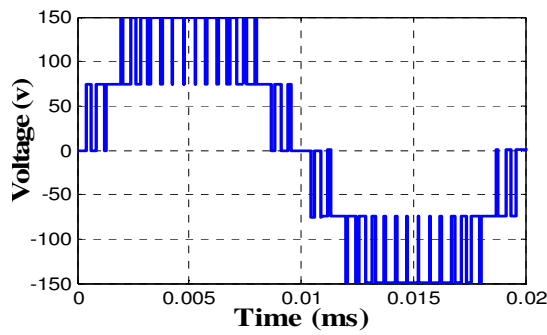
Fig.7. Level-shifted In-phase disposition technique

5. Simulation Results

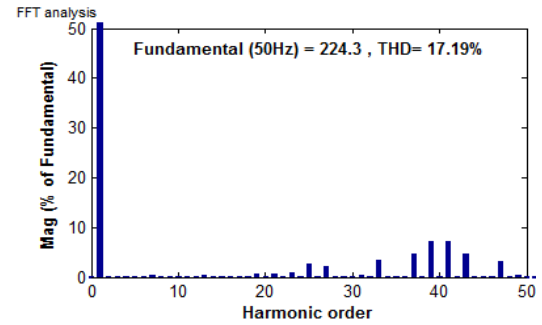
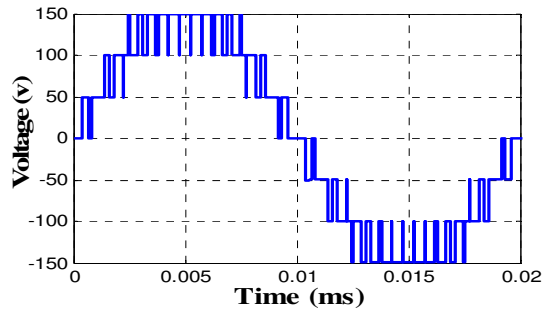
To appraise the performance of the single phase nine level proposed MLI is simulated in the Matlab/Simlink by choosing the input parameters as $V_{A1} = V_{A2} = V_{B1} = V_{B2} = 50V$ and the R-L load is taken as 150Ω and $100mH$. The appropriate switching is produced by the resultant pulses to obtain different levels of staircase waveform. Output voltage of the three, five, seven, nine levels and their individual harmonic spectra are shown in Fig.7. The Table 4 shows the comparison of T.H.D for different levels. The Fig.8 shows the single phase inductive load currents which is of ripple free and distortion less for various loads. The bar chart in Fig.9 shows as the output voltage is varying the number of switches in the conduction path are reduced for the proposed topology, in this chart x-axis represents number of levels and y-axis represents the number of switches in the conduction path. For the proposed CMLI for nine level is taken as $(a \times b) = (2, 2)$.



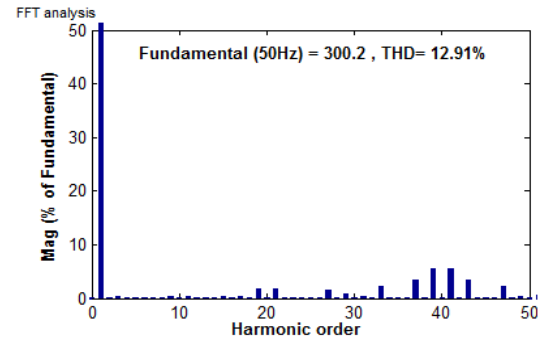
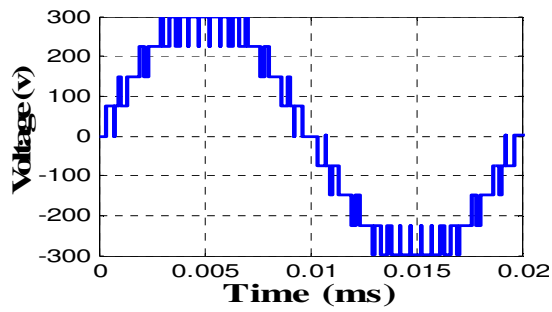
a) Three level



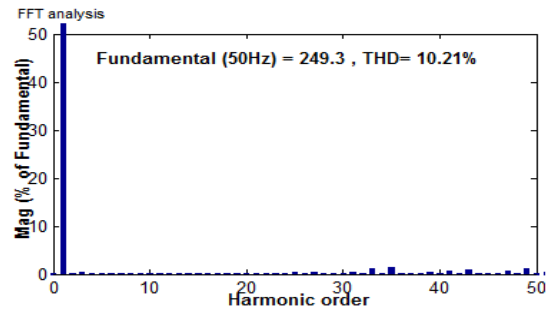
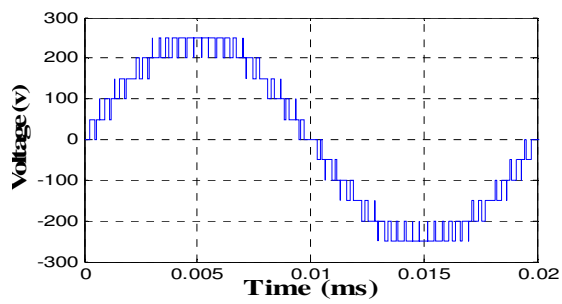
b) Five level



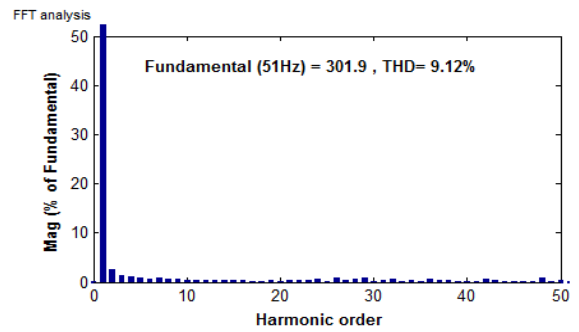
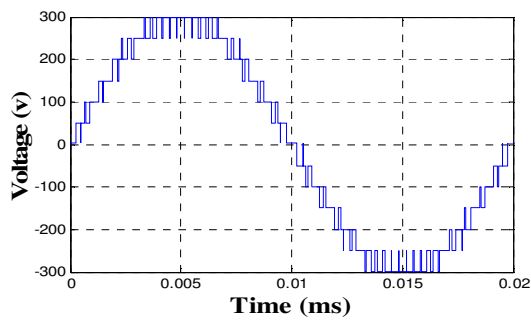
c) Seven level



d) Nine level

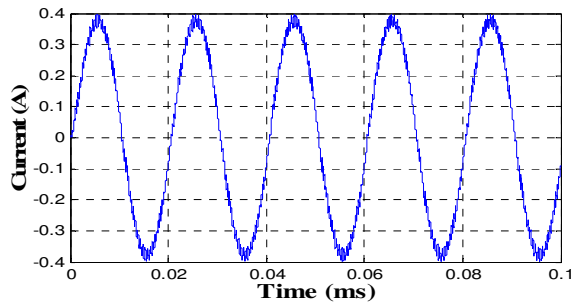


e) Eleven level

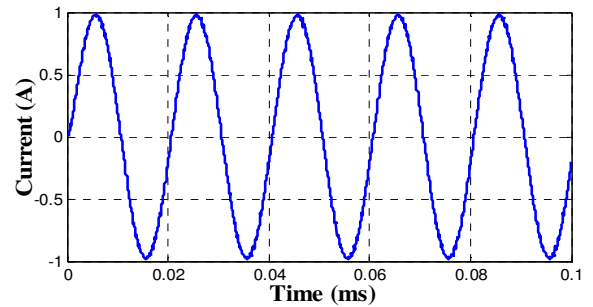


f) Thirteen level

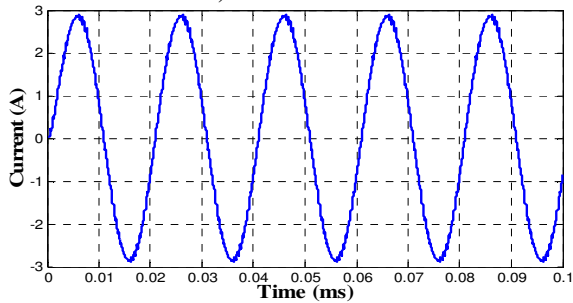
Fig.8. Output voltage of (a) three level, (b) five level, (c) seven level, (d) nine level, (e) eleven level, (f) thirteen level



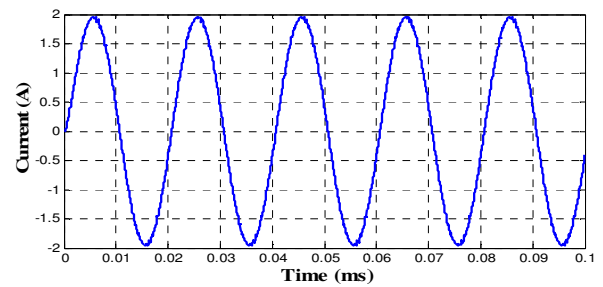
a) Three level



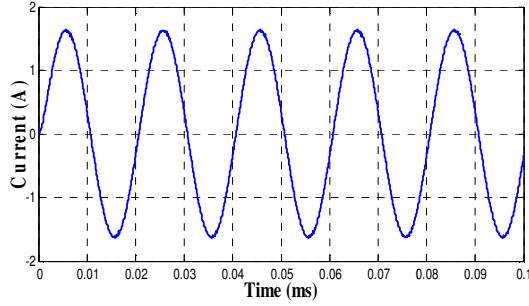
c) Seven level



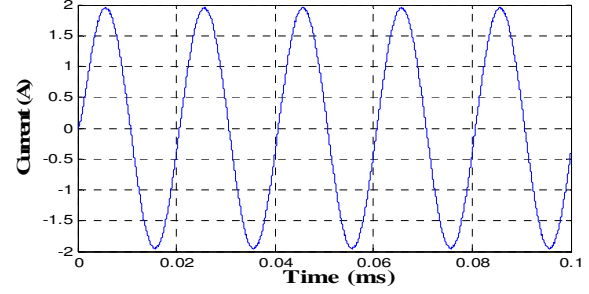
b) Five level



d) Nine level



e) Eleven level



f)Thirteen level

Fig.9. Single phase inductive load current : (a) three level,(b) five level,(c) seven level,(d) nine level,(e) eleven level,(f) thirteen level

Table 4. Shows the comparison of T.H.D for different levels

Sl.No.	No. Of Levels	T.H.D
1.	Three level	41.58
2.	Five level	25.60
3.	Seven level	17.19
4.	Nine level	12.36
5.	Eleven level	10.21
6.	Thirteen level	9.12

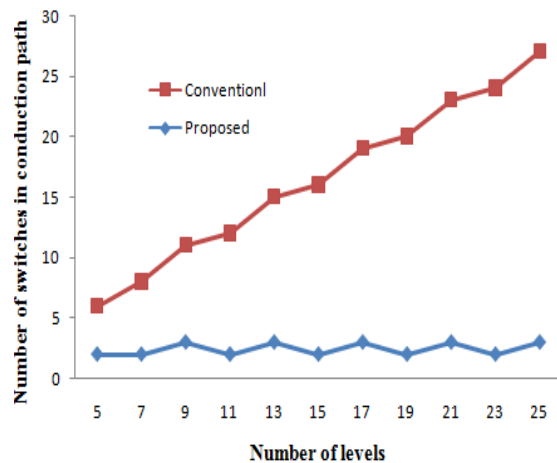


Fig.10. Graph varying for number of switches in the conduction path and number of levels

6. Conclusion

This paper proposes the new CMLI topology structure arranged in a matrix order. The topology has shown that the CMLI had produce the output voltage with reduced number of the power conducting devices when compare with convectional CMLI. The main benefit of the projected structure is the quantity of switching devices as well as the gate drives are reduced, therefore the circuit becomes less complex for control, the size and cost are reduced. In this topology the conduction period is desperately get reduced for switching modes of operation, thus which reduced the conduction losses and electromagnetic interference. To evaluate the operation of proposed topology simulation results have provided that proposed inverter produce less harmonic distortion when compared to the conventional CMLI. This generalized structure can be far-reaching to advanced levels by duplicate the intermediate switches.

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