VLSI IMPLEMENTATION OF VARIABLE BIT RATE OFDM TRANSCEIVER SYSTEM WITH MULTI-RADIX FFT/IFFT PROCESSOR FOR WIRELESS APPLICATIONS

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Abstract: *In this paper, a Variable Bit Rate 64 Subcarrier OFDM Transceiver system is implemented in FPGA and the Modified Multi-radix 64 point FFT/IFFT blocks present in the OFDM design is intended for immense throughput Wireless Personal Area Network (WPAN) applications. The Proposed OFDM architecture is transmitted with different input Bit patterns and modulated by orthogonal frequencies. To scale down the complications of the Twiddle factor multiplications in FFT/IFFT blocks, Radix-2^2, 2^3, 2^4 are devised in it. The FFT algorithm with Single-path Delay Feedback (SDF) structure is made by Vedic multiplier along with compressor adders, in order to decrease the hardware cost and gives better speed performance in the FFT multiplier. The OFDM Transceiver design is implemented using Xilinx Virtex2 xc2v500-6 fg256 FPGA board, acquires 52.4K gates and consumed Power is about 64 mW with the operating frequency of 197MHz. The Cadence Design Tool with 90nm CMOS technology is used only for FFT/IFFT section in OFDM transceiver system, which occupies 25% reduction in total gate count and 33.9% less in Power dissipation as related to other existing FFT algorithms. The Multi-Radix 64-point IFFT/FFT algorithm using Vedic Multiplier can achieve the throughput rate of 162 MS/s along with the working frequency of 162 MHz can be intended for WPAN applications.*

Key words: *FFT, IFFT, OFDM, SDF,MDF,CCM, CBM.*

1. Introduction

In the present scenario, various research centers in the world are working toward the development of Orthogonal Frequency Division Multiplexing (OFDM) in many applications. The OFDM transceiver design is used to enhance the data transmission faster by virtue of its highly efficient Multi-carrier Modulation technique.OFDM is extensively used in many communication protocols such as Wireless Local Area Network (WLAN), Wireless Personal Area Network and Wireless Metropolitan Area Network (WMAN) [1].The WPAN is used to provide high speed data transmission in home network systems and wireless Sensor Networking services. The short distance wireless data transmission completed with WPAN has wireless networking standard IEEE 802.11ad and it provides high data rate up to 2.115 GS/s at 60 GHz. For the Physical layer of sufficient data rate WPAN, Orthogonal Frequency Division Multiplexing design has been preferred as the most suitable modulation technique [2].

Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) processors plays a significant role in the OFDM Transceiver design, which acquires high hardware complexity. In recent years,several FFT processors have been designed based on Pipelined style architectures and Memory-based architectures [3].The Memory-based architectures used in the FFT algorithm cannot be parallelized, as the design takes long latency with 1ow data throughput [4]. The Pipelined style architectures overcome these drawbacks by reducing the hardware complexity. There are two popular design types used in the Pipelined style architectures are Multipath Delay Feedback (MDF) and Single path Delay Feedback (SDF). The Modified IFFT/FFT blocks are constructed using Single path Delay Feedback (SDF) structure, as it requires less hardware cost and Power consumption.

The structure of the FFT processor and its implementation complexity will be depends on the Radix algorithm selection. If Radix selection in the FFT processor is small, it will results a simple Butterfly structure and a higher radix selection in the FFT processor can scale down the area of the twiddle factor multiplication.The FFT processor devised using

Radix-2 algorithm results with a regular butterfly structures with many complex multiplications. The choice of Radix-4 FFT architecture will reduce the count of complex multiplications but it needs a butterfly unit with 4 point structure that yields higher complexity in hardware [5].

In FFT processor, several Radix algorithms like Radix-2^2, Radix-2^3, Radix-2^4 and Radix-2^k, can reduce the complexity of twiddle factor multiplication is discussed in [6 – 8]. The Multiplier unit is the important component in FFT processor, which occupies more hardware complexity. The speed of the FFT processor will depend on the multiplier selection. Sri Bharati Krishna Tirthaji has made the old vedas in the midway through 1911 and 1918 and Vedic mathematics derived by using those vedas, has framed the Vedic multiplier structure [9].

To obtain low hardware complexity, Vedic mathematics formula called Urdhav-Tiryakbhyam (Vertical and Cross wire) method is used in the digital multiplier architecture of the FFT algorithms have been studied [10-14]. Tushar.v.More and Ashish R.Panat [15] present an FPGA Implementation of FFT Processor using Vedic algorithm, but the Radix-4 Butterfly unit structure used in FFT can attain more hardware complexity. Prashant D.Pawale, Venkat N Ghodke [16] proposes a high speed Vedic multiplier design and implementation that consumes more area, when the bit count in the multiplier is increased. The Modified FFT processor is composed of Vedic multiplier besides compressor adder is used to reduce the unnecessary multiplication steps and decrease the critical delay in the multiplier units. As compared to other regular structure adders, the compressed adder is used to enhance the speed of the FFT multiplier [17].

In this brief, a Variable Bitrate OFDM Transceiver system with Radix-2^2,2^3,2^4 IFFT/FFT Processor is implemented using Xilinx Virtex 2 xc2v500-6 fg256 FPGA board, can achieve 52.4K gate count and consumed Power is about 64mW with the operating frequency of 197 MHz. The Multi Radix FFT/IFFT blocks in an OFDM transceiver system are devised and it is implemented using 90-nm CMOS technology has possibly obtained a low hardware complexity and high throughput rate of 162 MS/s can be striving for WPAN applications.

This paper is arranged in such a way that, Section 2 discusses about the Design Consideration of OFDM Transceiver design and Section 3 portrays the Proposed Variable Bitrate OFDM Transceiver system with Radix-2^2, 2^3, 2^4 FFT algorithm employing Vedic multiplier.Section 4 exhibits the comparison and implementation results. At last, the conclusion is inclined in Section 5.

2. Design Consideration of the OFDM Design

The OFDM is the most attractive modulation approach in the wireless transmission because it provides high speed and large data rate in various communication standards depends upon the requirements. The OFDM Transceiver system is used to transmit many subcarriers in parallel with several modulation schemes like 16 QAM, QPSK, OQPSK, BPSK in orthogonal frequencies. There are 64 subcarriers used in the OFDM system and its input data is $x_0(t)$, $x_1(t)$,.... $x_{63}(t)$, can modulate with orthogonal frequencies like $0f_d$, $1f_d$, $2f_d$,….$63f_d$. The Discrete Fourier Transform (DFT) of the given length N is formulated by

Stage 1 :

$$X(t) = \sum_{m=0}^{63} x_m(t).\exp(2\pi jmf_dt) \quad (1)$$

with $f_d = 1/T$

Where,

x_m - Input Data

f_d – Frequency for first sub carrier

T – Pulse Duration

Assume, $t = nr$

Take 64 subcarrier of the pulse X(t) which is of duration T. Let $r = T/64$ and denote $x(nr)$ by $x(n)$ for $n = 0,1,..\ 63$. Let us consider, $x_m(nr) = x_m$ constant for $0 < n < 63$. Then,

$$X(nr) = X(n) = \sum_{m=0}^{63} xm(t)\ \exp(2\pi jmnr/T) \quad (2)$$

Therefore,

$$X(n) = \sum_{m=0}^{63} x_m \exp\ (jm(2\pi/64)n) \quad (3)$$

For $0 < n < 63$; Let $= r/T = 1/64$

$= 64 * \text{IFFT}\ (\{x_m\}0,63\ )$

$$X(t) = \sum_{m=0}^{63} xm\,(t) \exp\,(2\pi jmfdt) \qquad (4)$$

The Equation (4) represents the output of IFFT for the variable Bitrate OFDM Transceiver system.

Stage 2:

The output of IFFT is to modulate the high frequency carrier with the result of performing stage 1 is given by

$$x(t) = \sum_{m=0}^{63} x_m\,(t) \exp\,[2\pi j(fc + mfd)t] \qquad (5)$$

This is the output of OFDM Signal

T – Pulse Duration between subcarriers

1 / T – no of pulses per second on each subcarrier

$f_d = 1 / T$

$T = 1 / f_d$

$= 1/14.285$ KHz

$= 70\ \mu s$ on each sub carrier

Table 1

Specifications of OFDM Transceiver Design

Master clock	48 MHz
Variable Clock Generator	14.285 KHz, 28.571KHz… 914.24 KHz
Variable Data Generator	128, 64 Bits
Sub carriers	64
Modulation Techniques	8- 16QAM 10 - QPSK 4 - OQPSK 4 - BPSK
FFT Processor	Radix-2^2, 2^3, 2^4
Multiplier	16 Bit Vedic Multiplier
Adder	Compressed Adder

The Variable Bitrate OFDM Transceiver system is implemented using Xilinx Virtex 2 FPGA board has 48 MHz crystal with variable frequencies used. As shown in Table 1, the FFT processor is made up of Vedic multiplier, as it decreases the hardware complications and minimize the power consumption.

3. Proposed OFDM Transceiver architecture

The Block diagram of the Variable Bitrate OFDM Transceiver design with Multi-radix FFT algorithm is shown in Fig.1. The proposed OFDM Transceiver design has been designed using Variable Bit Patterns Generator (64 & 128 bits) and it will flow serially as an input to OFDM transmitter. Depends on various modulation techniques (16QAM, BPSK, OQPSK, and QPSK), the digital serial data is encoded by linear feedback shift register logic with four bits, two bits and single bit depend on the modulation scheme and it will flow as an Inphase (I) & Quadrature (Q) streams in the symbol mapper. To minimize the Bit Error Rate (BER) in data transmission, the results of the Inphase (I) and Quadrature (Q) components are sent to Gray Encoder Block. The result bits from the Gray Encoder can take as a symbol and sent into the signal mapper. There are various symbols originated in the signal mapper, which is in the frequency domain.

The 64 Point IFFT block present in the OFDM transmitter is used to convert those frequency domain signal into a time domain signal.To obtain I modulation and Q modulation for each subcarrier, the Inphase (I) and Quadrature (Q) components are multiplied with orthogonal frequencies of sine and cosine carriers. Finally,the summation of these entire subcarrier signals gives the OFDM signal. The major limitation in the wireless data transmission is Inter Symbol Interference [ISI] which is generated by the virtue of multipath reflection in the channel. To counteract the OFDM signal from ISI and to maintain the orthogonality function surrounded by the sub carriers, a cyclic prefix is infused between the OFDM symbols. The Final OFDM transmitter signal is sent through a transmitter antenna.

The OFDM Receiver design is used to demodulate the signals from the transmitter and it works as, inverse operation of the OFDM transmitter design. On the receiver side, the OFDM transmitted signal is collected by receiver antenna and it is moved into the removal of cyclic prefix block to discard the cyclic prefix between the OFDM symbols which is in time domain representation. The 64 point FFT block occurs in the OFDM receiver is used to convert those time domain signal into frequency domain signal.

The Multi Radix structure is used in FFT/IFFT processor with 16 bit Vedic Multiplier along with compressed adder. In OFDM receiver, the Numerically

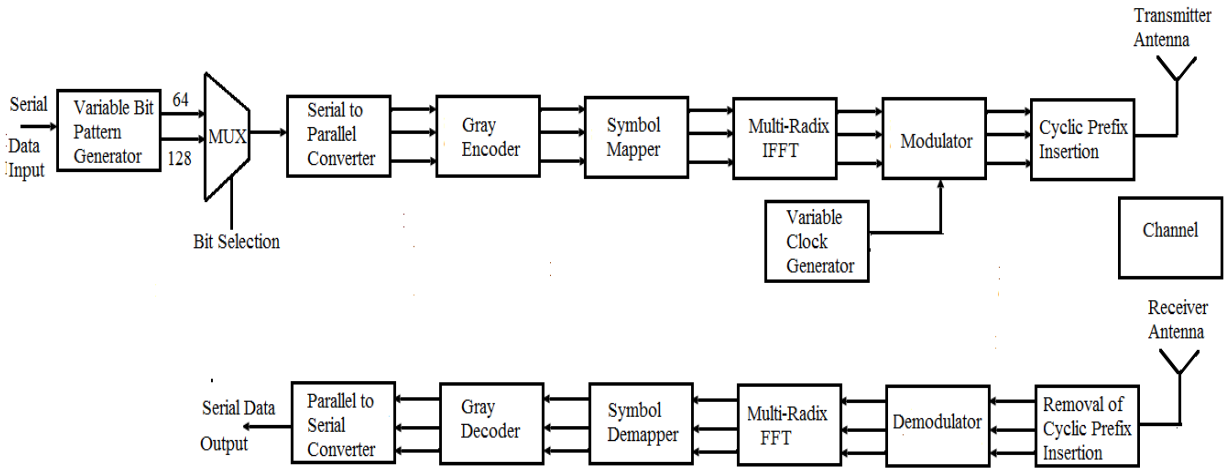

Fig. 1. Block Diagram of OFDM Transceiver Design

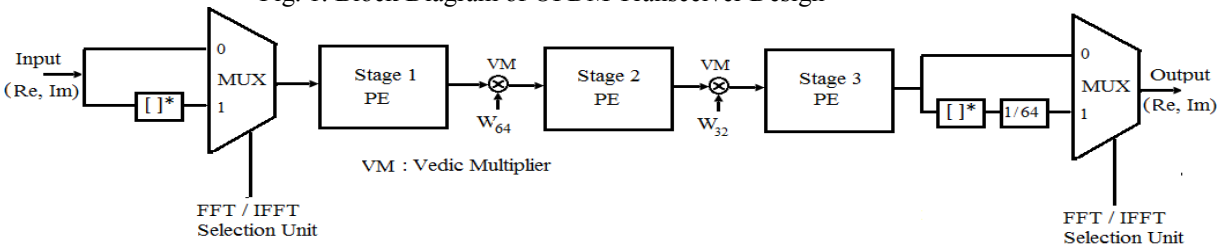

Fig. 2. Block Diagram of the single data path 64 point Multi Radix FFT/IFFT Processor

Controlled Oscillator (NCO) generated sine and cosine carriers are multiplied with the outputs from the FFT block, to obtain Inphase (I) and Quadrature (Q) Demodulation signals. The Low pass filter block is allowed to attenuate the high frequencies of I and Q Demodulation signals and transmit them into low frequency.The filtered demodulated signal is transfused into the signal demapper block to group the data range and receives the transmitted data. Accordingly, the results from the signal demapper will flow through the Gray Decoder block, which is used to Decode I & Q Bits into serial bit pattern data.

3.1. Multi-Radix FFT/IFFT Processor with Vedic Multiplier

The FFT/IFFT is an important block used in the OFDM Transceiver design, which is used to reduce hardware complexity.The Block Diagram for 64 point Multi-Radix FFT/IFFT Processor is shown in Fig 2. In the 64 point IFFT/FFT processor, various Radix is used in each stage with the Butterfly units. The Radix 2^4, Radix 2^2 structure is used in stage 1, stage 2 and it consists of four Butterfly units and two Butterfly units respectively. The structure of stage 3 is made up of Radix 2^3 with three Butterfly units. The twiddle factor calculations in the Multi Radix FFT processor are employed using Vedic Multiplier.

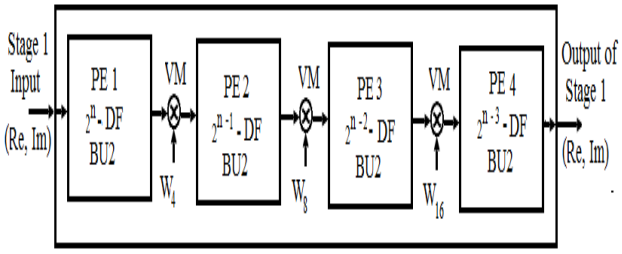

Fig. 3. Signal Flow diagram for Stage 1 Module

The Signal flow diagram for stage 1 Module has four Butterfly units is shown in Fig.3.

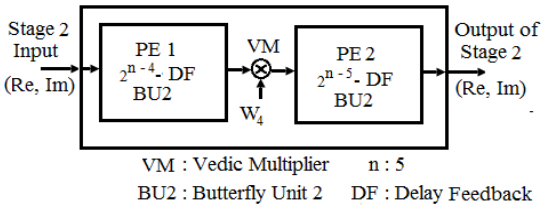

Fig. 4. Signal Flow diagram for Stage 2 Module

The Feedback delay structure is used in stage 1 has twiddle factor values of W_4, W_8, W_{16} and W_{64}. The

stage 2 Module with Feedback delay structure is shown in Fig.4 has twiddle factor values of $W_{4,}$ W_{32}.

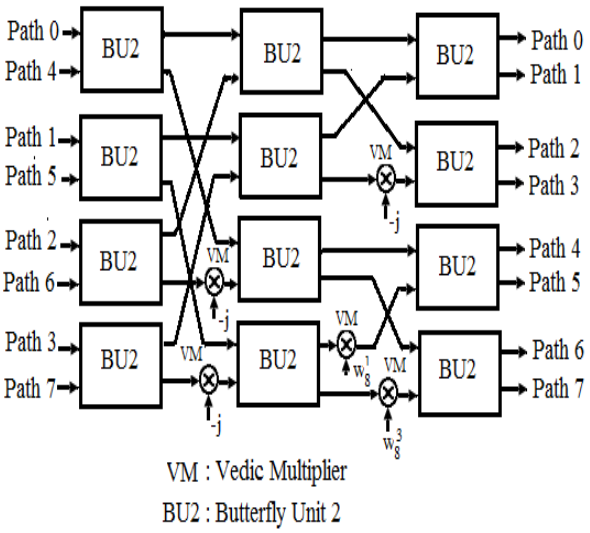

Fig. 5. Signal Flow diagram for Stage 3 Module

There is no Feedback delay structure present in stage 3 and it has three Butterfly units among twiddle factor values of $W_{4,}$ W_8 is shown in Fig.5. In the 64 point FFT/IFFT algorithm, 16 bit Vedic Multiplier is used in the stage1, stage 2 and stage 3 module, can perform computations faster and decrease the hardware complexity of the design.

3.2. Butterfly Unit

The block diagram of Butterfly Unit 2 is shown in Fig. 6 [2]. The Butterfly unit with delayed inputs can achieve complex addition and subtraction. The Real input (Rl_{in}) and Imaginary input(Img_{in}) in the butterfly unit is processed to obtain the Real output (Rl_{out}) and Imaginary output(Img_{out}). In addition, real and imaginary inputs along with delay buffers can be represented by DRl_{in} and $DImg_{in}$ and it is processed to retrieve, the real and imaginary outputs with delay buffers as DRl_{out} and $DImg_{out}$.[5]. The Butterfly Unit can handle the multiplexers and the selection signals. The twiddle factors $W_{4,}$ W_8 $W_{16,}$ W_{32} and W_{512} are calculated using Vedic Multiplier. In Vedic Multiplier, twiddle factor values saved in ROM can be taken as multiplicand of the FFT Multiplier.

3.3. Vedic Multiplier using Compressedadder

The Multiplier unit is the most significant component in FFT/IFFT Processor as it takes more hardware and it is expensive. Based on the multiplier selection, the computational calculations and hardware

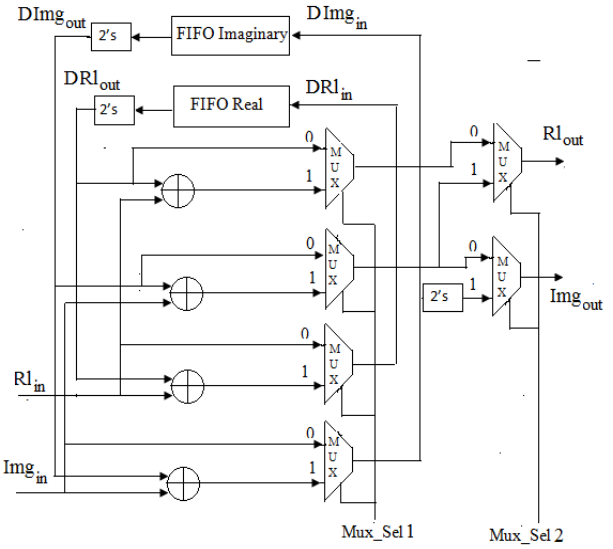

Fig. 6. Block Diagram of Butterfly unit 2 (BU2)

Cost in the FFT processor could be decreased. The Vedic multiplier with compressed adders used in the 64 point FFT architecture, reduces the gate count and minimizes the power with low hardware complexity.

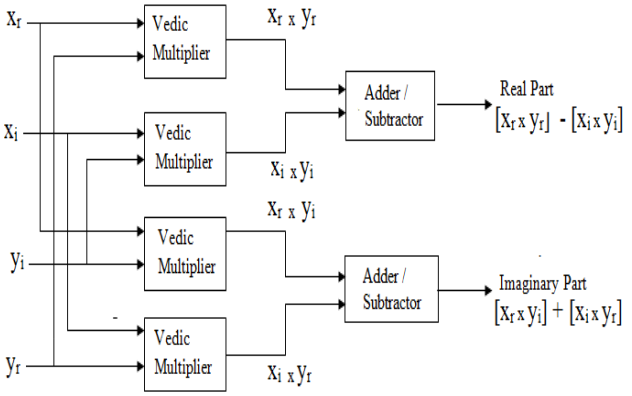

Fig. 7. Complex Vedic Twiddle factor Multiplier [11]

The Indian Vedic sutra called Urdhav-Tiryakbhyam method is allowed in the FFT multiplier to recede the unnecessary multiplication steps and produces parallelism in partial products. To decrease the propagation delay in FFT multipliers,Vedic multipliers are used in the complex multiplier structure. The twiddle factor values are multiplied with complex multiplier can be expressed in the form of [11]

$$(x_r + jx_i).(y_r + jy_i) = (x_r y_r - x_i y_i) + j(x_i y_r - x_r y_{i)} \quad (7)$$

The Vedic Mathematics is generally depends on 16 words formulae's named as Sutras.In the Multi-radix FFT processor, Urdhva Tiryakbhyam Sutra is used to multiply the binary digits in vertical and crosswise method and finally add its partial products using compressed adders. The calculation for Complex

Twiddle factor Multiplication using Vedic multiplier is shown in Fig.7.For n x n bit multiplication can be generated by this algorithmic rule. The compressed adder used in Vedic multiplier can reduce the critical delay in the FFT architectures.

A simple four bit binary multiplier builds using the Urdhav-Tiryakbhyam method is shown in Fig.8. For example, the Urdhav-Tiryakbhyam method is applied to two binary numbers x and y made up of 4 bits each i.e. $[x_0 - X_3]$ $[y_0 - y_3]$ and its final result product is denoted as r which consist of eight bits $[r_0 - r_7]$ [14].

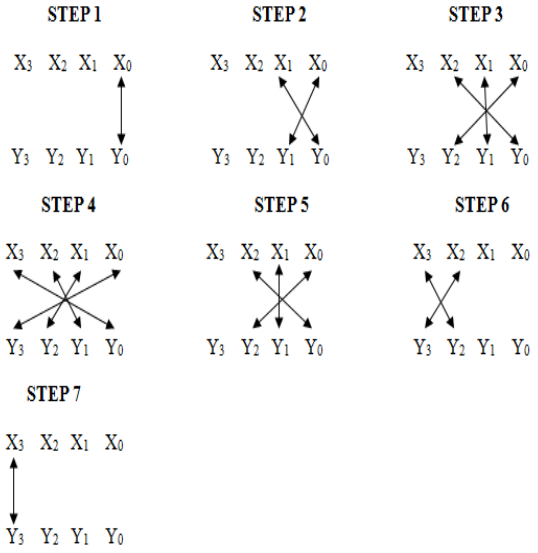

Fig. 8. Binary Number Multiplication based on Urdhva Tiryakbhyam sutra [14]

The multiplication is done with the Least Significant Bits (LSBs) of both x & y (vertical wise) and its product can be added to initial carry to obtain the LSB of the final result product. The initial carry value can be taken as zero. Then the least significant bit of x is multiplied near to the next higher bit of y and the least significant bit of y is multiplied near to the next higher bit of x (cross wise). Then add both the product bits and result of these bits can be added to preceding carry to obtain the final result product of the next bit. These steps are to be repeated for calculating the remaining bits of the final product.

The final product output along with carry for 4 * 4 Vedic multipliers using a vertical and crosswise method with compressed adder is expressed below. Equations (6) – (12) consequently to get the ultimate product.

$$r_0 = x_0y_0; \quad (6)$$

$$c_1r_1 = x_0y_1 + x_1y_0 ; \quad (7)$$

$$c_3c_2r_2 = c_1 + x_0y_2 + x_1y_1 + x_2y_0 ; \quad (8)$$

$$c_5c_4r_3 = c_2 + x_0y_3 + x_1y_2 + x_2y_1 + x_3y_0 ; \quad (9)$$

$$c_7c_6r_4 = c_4 + c_3 + x_0y_4 + x_1y_3 + x_2y_2 + x_3y_1 + x_4y_0; \quad (10)$$

$$c_{10}c_9c_8r_5 = c_6 + c_5 + x_0y_5 + x_1y_4 + x_2y_3 + x_3y_2 + x_4y_1 + x_5y_0; \quad (11)$$

$$c_{13}c_{12}c_{11}r_6 = c_8 + c_7 + x_0y_6 + x_1y_5 + x_2y_4 + x_3y_3 + x_4y_2 + x_5y_1 + x_6y_0; \quad (12)$$

The hardware architecture of 5-3 compressed adder used in 4 * 4 Vedic multiplier is shown in Fig.9. The Compressed adder is used to add more 4 bits at a time and gives improved speed performance in the multiplier unit. The Urdhav-Tiryakbhyam method is used in the Vedic multiplier to generate the parallel partial products and compute equations for each bit in the partial product.

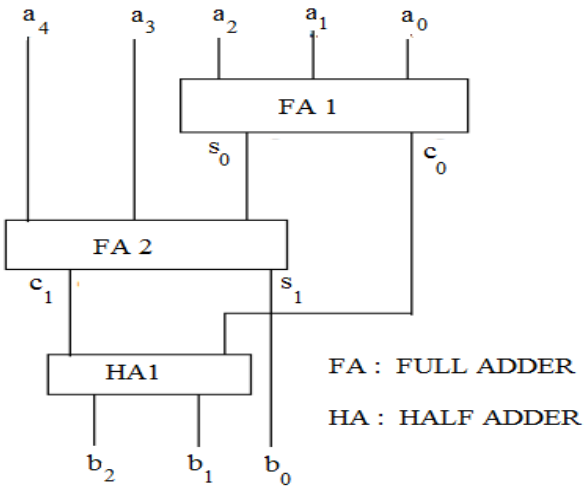

Fig. 9. Compressed Adders with Full adder and Half adder

Here, 5-3 Compressed adder is used to execute those equations (6) – (13) using logic gates, half adder and full adder. The 5-3 compressed adder circuit takes 5 inputs, add them and gives three bit output [17]. In Multi-radix 64 point FFT processor, 16-bit Vedic multiplier is used for computational calculations. To add the partial products in 16-bit Vedic multiplier, four compressed adder namely 5-3, 10-4, 15-4 and 20-5 are used. As compared to other adder architectures, the compressed adder have improvement in speed and reduce the critical delay in multiplier units.

4. Results and Comparisons

The OFDM Transceiver with Multi-Radix 64 point FFT architecture is performed using Vedic Multiplier can be focused on high rate WPAN applications. The arrangement of Urdhva Tiryakbhyam method in Vedic multiplier, can occupy an optimum area in the silicon chip layout. As related to other multiplier algorithms, when the bit count increases in the vertical and crosswise sutra, area and gate delay can be raised gradually. Hence the Urdhva Tiryakbhyam based Vedic multiplier is time, space and power efficient [18].

4.1. Variable Bit Pattern Generator

The Variable digital data Patterns (64 and 128 bits) are generated and it flows serially into an OFDM transmitter design based on FPGA DIP switch selection. The 128 Bit pattern data are shown in Fig.10

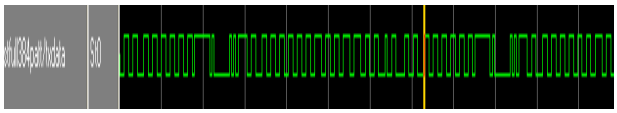

Fig. 10. 128 Bit Pattern Generator

4.2. 16 QAM Modulation output

In OFDM Transceiver design, 64 subcarriers are used. Each subcarrier is transmitted by different modulation schemes with orthogonal frequencies. Here,the result of one subcarrier 16 QAM modulation signal is shown in Fig.11. Depends on the Modulation technique, the input serial data is encoded by four, two bits and single bit. The signal mapper is used to allocate the symbols, Inphase (I) & Quadrature (Q) component for each subcarrier. In 16 QAM, 16 symbols, four bits per symbol is used and it has two bits of I component and two bits of the Q component There are eight 16 QAM Modulations used for OFDM Transmitter.

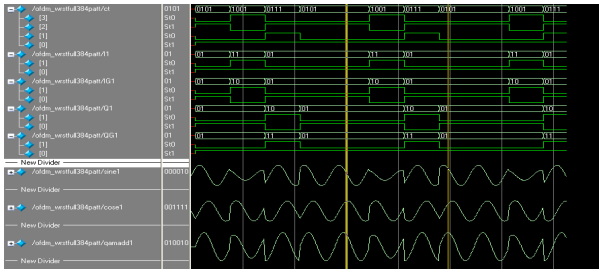

Fig.11. 16 QAM Modulated signal

4.3. QPSK Modulation outputs

There are ten QPSK Modulations used in the OFDM Transmitter design. The signal mapper of the QPSK, has four symbols. Each symbol consist of two bits, i.e one bit of I and Q component. The QPSK modulated signal for 64 bit pattern generator shown in Fig.12.

Fig. 12. QPSK Modulated signal

4.4. OQPSK Modulation output

In OQPSK Modulation, symbols and No. of bits used in I component and Q component are similar to QPSKModulation.There are four OQPSK Modulations used in the OFDM Transmitter.The OQPSK Modulation signal to corresponding I Channel and Q Channel is shown in Fig.13

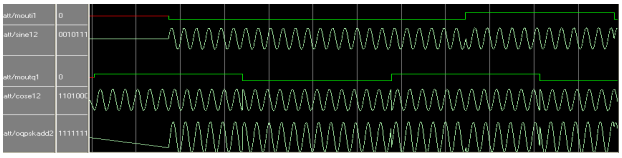

Fig. 13. OQPSK Modulated signal

4.4. BPSK Modulation output

The BPSK Modulation can transmit 1bit/ symbol and it has two phases which are separated by 180° is shown in Fig.14.It provides insufficient large data transmission.There are Four BPSK Modulations used in the OFDM Transmitter design.

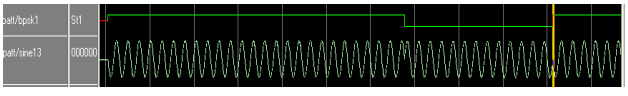

Fig. 14. BPSK Modulated signal

4.5. Fast Fourier Transform

The 16 Bit Vedic Multiplier based on the Urdhav-Tiryakbhyam sutra is used in FFT Processor to diminish the hardware complication. The Vedic Multiplier along with compressed adder is used in the FFT algorithm, to provide the improved performance

in speed. The unnecessary multiplication steps and propagation delay can be reduced by using the Vedic multiplier.The simulation waveform of the Vedic multipler using compressed adder is shown in Fig.15.

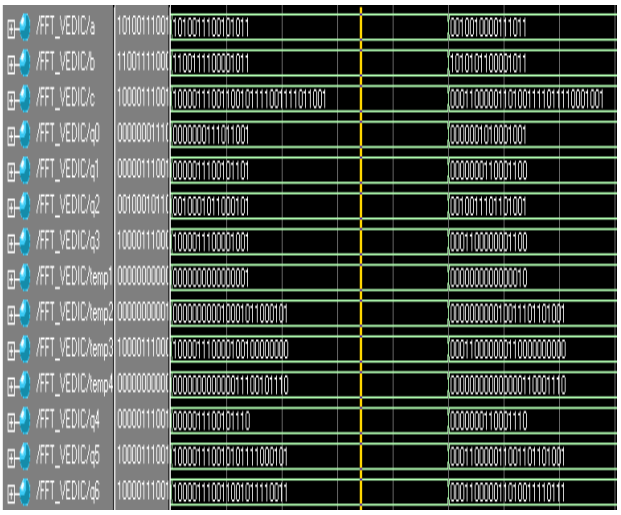

Fig.15. Functional Simulation for Vedic multiplier using Compressed adder

4.6. OFDM Modulated signal

There are 64 Sub-carriers used in OFDM Transmitter.The summation of entire Modulation schemes with orthogonal frequencies will form an OFDM signal is shown in Fig.16

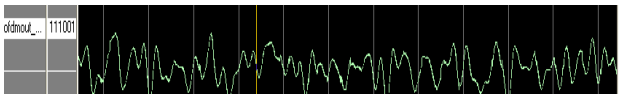

Fig.16. OFDM Transmitter signal

The RTL Schematic for the OFDM Transceiver system is shown in Fig.17.

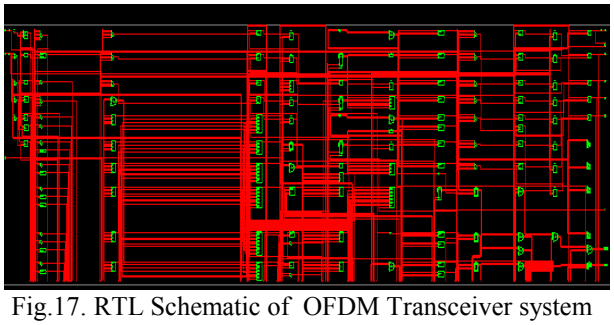

Fig.17. RTL Schematic of OFDM Transceiver system

The modified FFT algorithm hardware model is described using Verilog HDLcoder and its performance is simulated using Modelsim tool. The Power consumption as well as gate count report for the FFT algorithm is exhibited in Fig.18.

```
root@cadence7:~
File  Edit  View  Terminal  Tabs  Help
rc:/> report power

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  Generated by:           Encounter(R) RTL Compiler RC13.10 - v13.10-s006_1
  Generated on:           Apr 21 2017  11:30:33 am
  Module:                 fft_64pt
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------------------------
fft_64pt    21647  8879.121 5203495.513 5212375.219

rc:/> report area

============================================================
  Generated by:           Encounter(R) RTL Compiler RC13.10 - v13.10-s006_1
  Generated on:           Apr 21 2017  11:31:21 am
  Module:                 fft_64pt
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance  Cells  Cell Area  Net Area  Total Area  Wireload
------------------------------------------------------------
fft_64pt  21647  526721  4978   531699     (D)
```

Fig.18. Power and Gate count Report for Multi-Radix FFT Processor

The various parameters obtained from OFDM Transceiver system are listed in Table 2. The OFDM Transceiver design occupies 52.4K gate count and estimated power of 64 mW.

Table 2

OFDM Transceiver Output

Gate count for Design	Estimated Power Consumption	Bandwidth of OFDM signal
52,472	64 mW	914.24 KHz

The Proposed Architecture is synthesized and simulated using Xilinx ISE, Modelsim tool and Xilinx Virtex 2 xc2v500-6 fg256 FPGA device chip. The Device usage summary is listed in Table 3.

Table 3

Device usage summary –Virtex 2 xc2v500-6 fg256 FPGA Board

Logic utilization	Used	Available	Utilization
Number of Slices	751	6144	12%
Number			

of 4 input LUTs	4227	6144	68%
Number of bonded IOBs	95	172	55%
Number of occupied slices	2358	3072	76%

The FFT/IFFT blocks used in the OFDM Transceiver system is simulated and synthesized using 90nm CMOS technology nearby 1.2 supply voltage. The Multi-radix FFT algorithm using Vedic multiplier occupies 21K Gate count and 5.21 mW of Power consumption. The core area obtained from the FFT processor is 0.47 mm^2.

Table 4 exhibits the comparison results of the proposed FFT algorithm with various points of FFT processors. As related to other existing FFT processor [5], the modified FFT algorithm using Vedic multiplier acquires 25% reduction in total gate count and 33.9% less in Power dissipation.The complex constant multiplier and complex Booths multiplier are used in the 512 point FFT processors [2] and [3], can occupy more hardware in the multiplier unit. The Vedic multipliers are used in the FFT algorithm, to eliminate the unnecessary multiplication steps so that the hardware complication is reduced.The Compressed adder used in Vedic Multiplier can reduce critical delays as compared to other existing adders used in the FFT multipliers [4]. The Multi Radix 64 point FFT processor has achieved a throughput rate of 162 MS/s with the operating frequency of 162 MHz can be used for Wireless applications.

Table 4

Comparison results of several FFT Processors

Parameters	This work	[5]	[4]	[3]	[2]
FFT Size	64	64	64	512	512
Technology	90 nm	180	180	130 nm	90 nm
FFT algorithm	Radix 2^4-2^2-2^3	Radix 2^2-2^3	Radix 2	Radix 2^4-2^2-2^3-	Modified radix 2^5
No. of data-paths	1	1	1	8	8
Architecture	SDF	SDF	SDF	MDF	MDF
Internal word length (bit)	I,Q : 16	I,Q : 16	I,Q : 16	I,Q : 14	I,Q : 12
Gate count	21K	28K	33.5K	-	290 K
Core area (mm^2)	0.47	-	0.94	0.76	0.78
Max. Clock rate (MHz)	162	125	80	220	310
Throughput	162 MS/s	125 MS/s	80 MS/s	1.76 GS/s	2.5 GS/s
Power Consumption (mW)	5.21	7.89	9.79	-	92.8
Multipliers used	Vedic	CCM	CCM, Bit Parallel	CCM	CCM, CBM

CCM denotes Complex Constant Multiplier CBM denotes Complex Booths Multiplier
SDF denotes SinglePath Delay Feedback MDF denotes MultiPath Delay Feedback

4. Conclusion

In this paper, the Variable Bit rate 64 subcarrier OFDM Transceiver system with Multi- Radix FFT/IFFT Processor is intended for high performance WPAN applications. The Proposed design is implemented using Xilinx Virtex2 xc2v500-6 fg256 FPGA board, as it acquires 52.4K gates and consumed Power is about 64mW with the operating frequency of 197 MHz. In comparison to the other existing FFT architectures, modified 64 point FFT processor using Vedic multiplier achieves a reduction in the total gate count and Power dissipation. In OFDM system, the FFT/ IFFT blocks with compressed adder can attain a throughput rate of 162 MS/s and it operates with the maximum frequency up to 162 MHz. The throughput rate of the FFT algorithm can enhance further, by placing the suitable pipelined registers in the design. The modified FFT processor has attained the reduction in hardware complexity and power consumption, it can strive for WPAN applications.

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