A CONTROL STRATEGY BASED ON UTT AND PBT OF THREE-PHASE FOUR-WIRE UPQC

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Abstract: *This paper presents the realization of different power quality (PQ) problems and their mitigation using Unified Power Quality Conditioner (UPQC) on a three-phase four-wire distribution system. The proposed control strategy for the control of UPQC is based on the combination of unit vector template technique (UTT) and power balance theory (PBT). The control technique based on UTT is used to get the reference signals for series active power filter (APF), while PBT is used for the control of Shunt APF. The performance of proposed control algorithm is evaluated in terms of power-factor correction, load balancing, neutral source current mitigation and mitigation of voltage and current harmonics, voltage sag ,voltage swell and voltage dip. In this control strategy of UPQC, the current/voltage control is applied over the fundamental supply currents/voltages instead of fast changing APFs currents/voltages, there by reducing the computational delay and the required sensors. MATLAB/Simulink based simulation results are presented, which support the functionality of the UPQC.*

Keywords: *Power Quality, UPQC, Load Balancing, Power Factor Correction, voltage and current harmonic mitigation, voltage saga, voltage swell, voltage dip.*

1. Introduction

The present day distribution systems are facing severe PQ problems like high reactive power burden, poor power-factor, load unbalancing, current harmonics, voltage harmonics, poor voltage regulation, voltage sag, swell and voltage dip etc. The main reason behind this is increasing use of power electronics based and poor power-factor loads for industrial, commercial and domestic purposes. These nonlinear loads draw non-linear current and degrade electric power quality. The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on [1]. In addition to this, the overall load on a distribution system is hardly found balanced, which cause excessive neutral currents of fundamental and as well as other harmonic frequencies, in a three-phase four-wire distribution system. Now days more advanced and sophisticated software and hardware are used for control systems, hence power quality has become one of the most important issues for power electronics engineers. To limit the PQ problems, many standards are proposed such as IEEE-519-1992[2].

On the transmission side ,FACTS [3] devices has been used to enhance the power transfer capabilities of the transmission lines, while a group of devices, called Custom Power Devices(CPD) are used to improve the reliability and quality of the distribution system. The CPD mainly covers three devices namely, D-Statcom [4], DVR [5] and UPQC [6-7]. The D-Statcom is mainly used for the mitigation of current based distortions, while DVR finds its application for the mitigation of voltage based distortions. The UPQC is one of the best solutions to compensate both current and voltage related problems, simultaneously. As the UPQC is a combination of series and shunt APFs, two APFs have different functions. The series APF suppresses and isolates voltage-based distortions. The shunt APF cancels current-based distortions. At the same time, it compensates reactive current of the load and improves power factor.

To mitigate source neutral current along with other power quality problems on a three-phase four-wire distribution system, different topologies of the shunt APF of UPQC, are reported in literature [8], [11-14]. Some of these are three-leg VSI with split capacitor [8], three single-phase VSIs [11], four leg VSI [12]-[13], current source inverter [14] etc. Out of these reported topologies, the four leg VSI topology of shunt APF is most popular due to its simplicity and requires less hardware. The three legs VSI with split capacitor needs extra attention for maintaining the two capacitor voltages equal. Further three single-phase VSI based topology requires more hardware and becomes bulky. Hence, this paper presents a three-phase, four-wire UPQC in which shunt APF is realized using three-phase four-leg VSI, the series APF is realized using a three-phase, three-leg VSI.

There are many control strategies reported in the literature to determine the reference values of the voltage and the current of three-phase four-wire UPQC, the most common are the p-q-r theory[8],modified single-phase p-q theory[9], synchronous reference frame(SRF) theory[10], symmetrical component transformation [11],and unit vector template (UVT) technique [12] etc. In addition to this one cycle control (OCC) [13] (without reference calculation) is also used for the control of three-phase, four-wire UPQC.

This paper proposes a control strategy of a three-phase, four-wire UPQC, based on the combination of UTT and PBT [16]. A control technique based on UTT is used to get the reference signals for series APF, while PBT is used for the control of Shunt APF. In this control strategy of UPQC, the current/voltage control is applied over the fundamental supply currents/voltages instead of fast changing APFs currents/voltages, there by reducing the computational delay and the required sensors. The realization of different power quality problems and comprehensive performance analysis of UPQC with proposed control algorithm is the main focus of the work.

The realization of different PQ problems and the UPQC system are discussed in Section II. The control algorithm for shunt and series APF are discussed in Section III and section IV, respectively. The SIM POWER SYSTEM (SPS), Matlab/ Simulink based simulation results are discussed in Section V and finally Section VI concludes the paper.

2. System Description

The basic block diagram of the UPQC connected on a three-phase four-wire distribution system is shown in Fig.1.The UPQC is connected before the load to make the source currents balanced, sinusoidal and in phase with the supply voltages and at the same time to make the load voltage free from any distortions. The current based distortions are realized using a combination of linear and non-linear load. Single-phase lagging power-factor load is taken as a linear load, where as a three-phase diode bridge rectifier with a resistive load on dc side is considered as a non-linear load. Load unbalancing is created by opening phase 'b' with the help of a switch. The distortions in the source voltage such as harmonics, sag and swell are realized by switching on/off the three-phase rectifier load, R-L load and R-C load, respectively. In order to create a voltage dip in the load voltage an induction motor is switched 'on' suddenly.

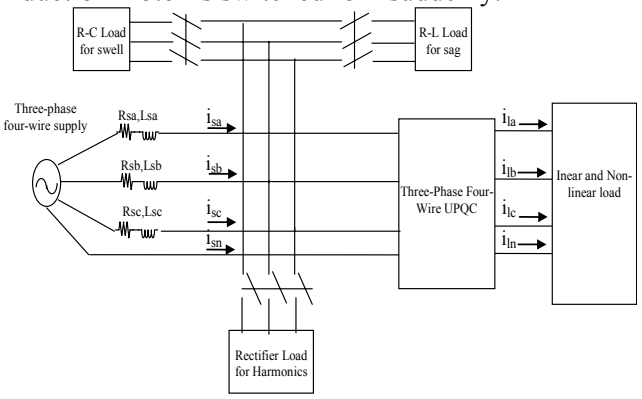


Fig. 1.Basic block diagram of UPQC connected on a three-phase four-wire distribution system

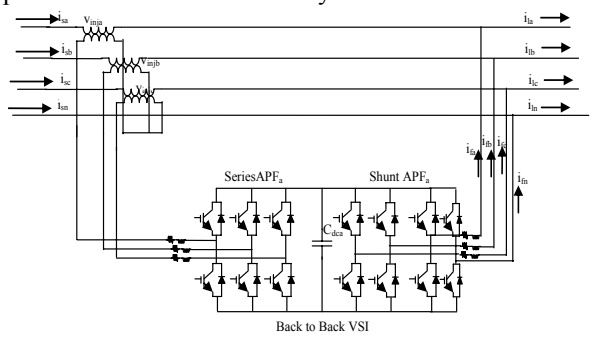


Fig. 2.Block diagram of UPQC

The UPQC, realized by using two voltage source inverters is shown in Fig.2. It consists of three-leg voltage controlled VSI used as a series APF and a four-leg current controlled VSI used as a shunt APF.

The DC link of both APFs is connected to a common DC link capacitor. The series filter is connected between the supply and load terminals using three single phase transformers with turn's ratio of 5:1.The primary winding of these transformer are star connected and the secondary windings are connected in series with the three-phase supply. In addition to injecting the required voltage, these transformers are used to filter the switching ripple content in the series active filter. A small capacity rated R-C filter is connected in parallel with the secondary of each series transformer to eliminate the high switching ripple content in the series APF injected voltage. The VSIs for both the series and shunt APFs are implemented with Insulated gate Bipolar Transistors (IGBTs).

In Fig.2 ($i_{sa,}$ $i_{sb,}$ i_{sc}), ($i_{la,}$ i_{lb}, i_{lc}) and ($i_{fa,}$ i_{fb}, i_{fc}) represents the source currents, load currents and shunt APF currents in phase a, b and c respectively. The source neutral current, load neutral current and shunt APF neutral current are represented by i_{sn}, i_{ln} and i_{fn} respectively. The injected voltages by the series APF in phase a, b and c is represented by v_{inja}, v_{injb} and v_{injc}, respectively. The values of the circuit parameters and the load are given in Appendix.

3. **Control Scheme of Series APF**

The control strategy for the series APF is shown in Fig.3. Since, the supply voltage is distorted, a phase locked loop (PLL) is used to achieve synchronization with the supply voltage [12].Three-phase distorted supply voltages are sensed and given to PLL which generates two quadrature unit vectors (sin*wt,* coswt).The in-phase sine and cosine outputs from the PLL are used to compute the supply in phase, 120^o displaced three unit vectors (u_a ,u_b u_c) using eqn.(4) as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (4)$$

The computed three in-phase unit vectors then multiplied with the desired peak value of the PCC phase voltage (V^*_{lm}), which becomes the three-phase reference PCC voltages as:

$$\begin{bmatrix} v^*_{la} \\ v^*_{lb} \\ v^*_{lc} \end{bmatrix} = V^*_{lm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (5)$$

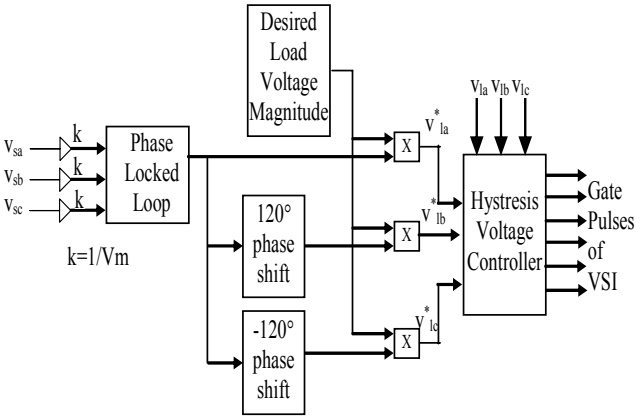


Fig. 3.Control Scheme of Series APF using UTT

The desired peak value of the PCC voltage under consideration is 338V (=415sqrt (2)/sqrt(3)).The computed voltages from reference voltages from eqn.(5) are then given to the hysteresis controller along with the sensed three phase PCC voltages($v_{la,}$ v_{lb} and v_{lc}).The output of the hysteresis controller is switching signals to the six switches of the VSI of series APF. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference voltage. Therefore, the injected voltage across the series transformer through the ripple filter cancels out the harmonics, voltage sag or swell present in the supply voltage.

4. **Control Scheme of Shunt APF**

The control algorithms for shunt APF consists of the generation of three-phase reference supply currents ($i^*_{sa,}$ i^*_{sb} and i^*_{sc}).Fig.4 shows the control algorithm based on power balance theory.

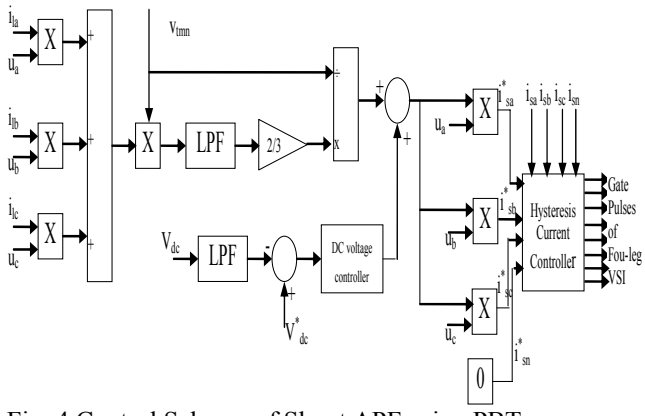


Fig. 4.Control Scheme of Shunt APF using PBT

In this scheme the unit templates are generated using PLL. The active power of load can be calculated as:

$$p_L = V_{tmn}\left(u_a i_{La} + u_b i_{Lb} + u_c i_{Lc}\right) \quad (6)$$

$$p_L = p_{dc} + p_{ac} \quad (7)$$

where V_{tmn} is peak value of the fundamental component of load voltage.

This instantaneous active load power has two components. First one is a DC component and second one is an AC component. The DC component of the load power can be filtered by a set of either a low pass filter or a moving average filter. For power-factor correction mode, only DC component of the load active power must be supplied by the source. The active component of the source currents has two parts. First one is I^*_{smp}, which is required DC component of the load active power and the second one, is I_{loss} which is required for the self supporting DC bus of the UPQC. The I_{loss} component is responsible for meeting the losses of UPQC, which may be calculated using eqn. (8) as:

$$I^*_{loss(n)} = I^*_{loss(n-1)} + K_{pd}\left\{V_{de(n)} - V_{de(n-1)}\right\} + K_{id} V_{de(n)} \quad (8)$$

where $V_{de(n)} = V_{dcr} - V_{dca(n)}$ denotes the error in V_{dc} calculated over reference value of V_{dc}. and average value of V_{dc}.K_{pd} and K_{id} are proportional and integral gains of the dc bus voltage PI controller.

The active component of the load current I^*_{smp} can be expressed as:

$$I^*_{smp} = \left(\frac{2}{3}\right) p_{dc} \,/\, V_{tmn} \quad (9)$$

The amplitude of the active component of the reference source current I^*_{sm} is:

$$I^*_{sm} = I^*_{smp} + I_{loss} \quad (10)$$

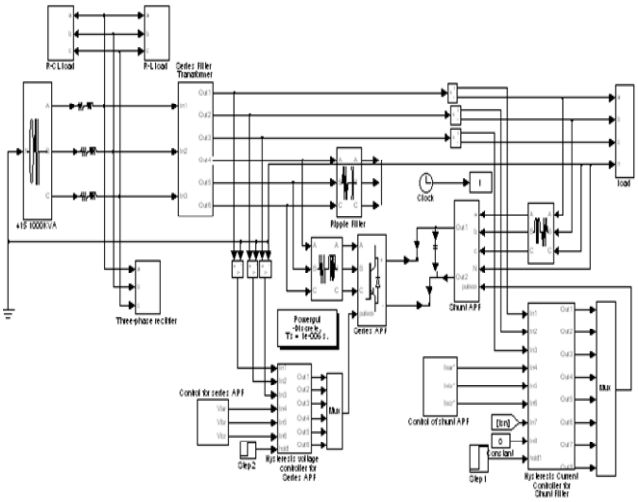
The three-phase reference sources current for power factor correction mode are obtained as:

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = I^*_{sm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (11)$$

In this proposed control algorithm, the sensed(i_{sa}, i_{sb} and i_{sc}) and reference source currents(i^*_{sa}, i^*_{sb} and i^*_{sc}) are compared in a hysteresis current controller to generate the switching signals to the switches of the shunt APF which makes the supply currents sinusoidal, balanced in in- phase with the voltage at PCC. Hence the supply current contains no harmonics or reactive power component. The source neutral current is compensated to fallow a reference signal of zero magnitude by switching the fourth leg of the VSI, through the hysterisis controller. By doing this, the supply neutral current can be eliminated. In this control scheme, the current control is applied over the fundamental supply currents instead of the fast changing APF currents, thereby reducing the computational delay and number of required sensor. In addition to this, the load or the filter neutral current are not sensed, thereby reducing the computational delay.

5. Results and Discussion

The developed model of UPQC with proposed control scheme using MATLAB/ Simulink and its Sim-Power System toolbox is shown in Fig.5. The performance of UPQC is evaluated in terms of voltage and current harmonics mitigation, load balancing, power-factor correction and mitigation of voltage sag, voltage swell and voltage dip under different load conditions.



5.1 Performance of UPQC for load balancing and power-factor correction

Fig. 6 shows the response of UPQC with linear lagging power-factor load for power-factor correction and load balancing. The shunt APF is put into operation at 0.1 sec. Fig.6 (e) shows that after 0.1 sec the source voltage and source current in phase ‘a’ are exactly in phase. At t=0.2 sec the load is changed from three phase to two phase to make the load unbalanced and restored to three-phase balanced load

at t=0.3 sec. During this period, a current 19.22A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.6 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.6 (f). It is also observed from Fig.6 (h) that during unbalanced load operation, the dc voltage is maintained to its reference value.

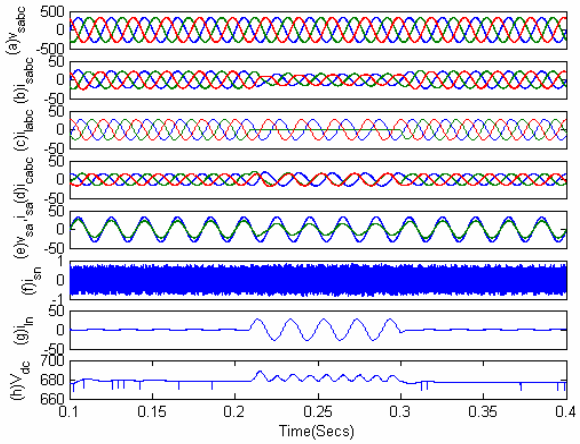


Fig. 6.Performance of UPQC for load balancing and power-factor correction

5.2 Performance of UPQC for load balancing, power-factor correction and current harmonic mitigation

Fig.7. shows the response of UPQC for power-factor correction, load balancing and current harmonic mitigation. In order to demonstrate the response of UPQC for load balancing, power factor correction and current harmonic mitigation, the load under consideration is a combination of a three-phase diode bridge rectifier with resistive load and two single phase lagging power factor load in phase 'a' and 'b' only. Because of this unbalanced load, a current 18.26A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.7 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.7 (f). It is observed that the supply currents are balanced, sinusoidal and in-phase with the voltages as is shown in Fig.7 (b).

5.3 Performance of UPQC for load balancing, power-factor correction, current and voltage harmonic mitigation

Fig.8 shows the response of UPQC for load balancing, power factor correction, voltage harmonic mitigation and current harmonic mitigation. In order to verify the effectiveness of control algorithm for voltage harmonic mitigation, a three-phase diode bridge rectifier with resistive load on dc side is switched on at 0.05 sec. Because of this the voltage across the load becomes distorted. To visualize the shunt APF and series APF performance individually, both APF's are put into operation at different instant of time. At time t_1=0.1 sec, shunt APF is put into operation first. It is observed from Fig.8 (d) that the supply currents are balanced; sinusoidal and in-phase with the voltages even under non-sinusoidal utility voltage. The source current THD in phase 'c' is improved form 15.30 % to 2.97 %. At time t_2=0.25 sec the series APF is put into the operation. The series APF starts compensating voltage harmonics immediately by injecting out of phase harmonic voltage, making the load voltage at load distortion free. The voltage injected by series APF is shown in Fig.8(c). Here load voltage THD is improved form 6.26 % to 0.85 %. The harmonic spectra of the source current and the load voltage in phase 'c' with compensation and without compensation are shown in Fig. 9. Because of unbalanced load, a current 18.75A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.8 (i).This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.8 (h).

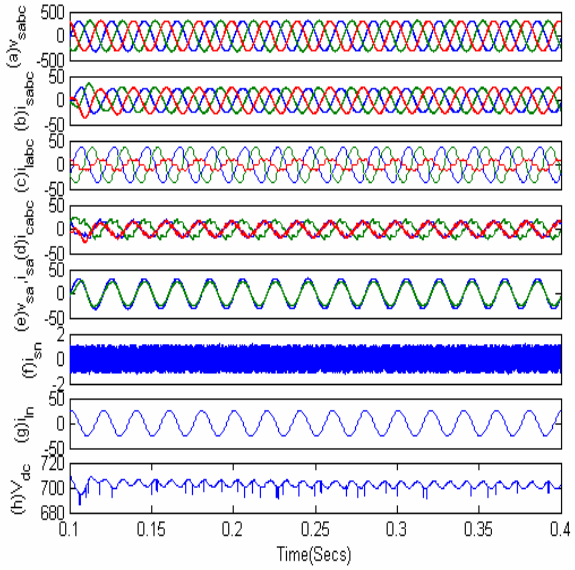


Fig. 7.Performance of UPQC for load balancing, power-factor correction and current harmonic mitigation

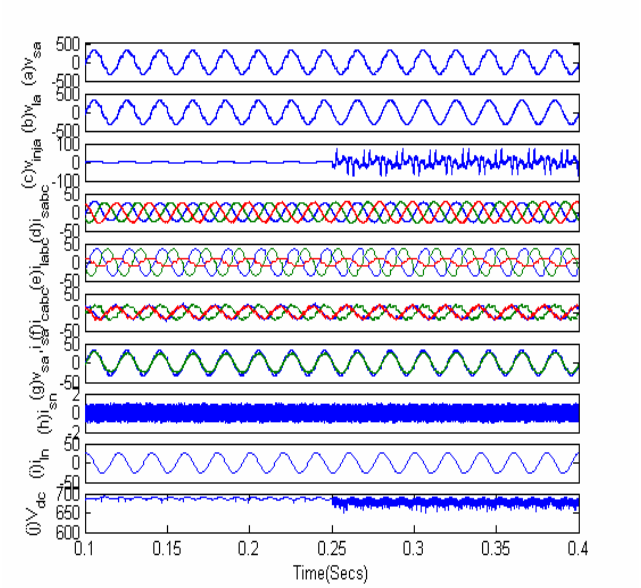


Fig. 8.Performance of UPQC for load balancing, power-factor correction, current and voltage harmonic mitigation

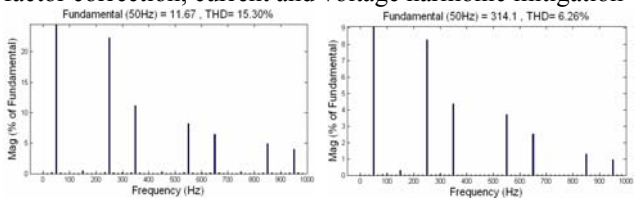


Fig. 9.(a) - (b) Source current and Load voltage without compensation

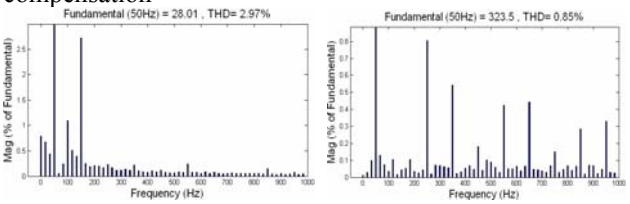


Fig. 9.(c) - (d) Source current and Load voltage with compensation

5.4 Performance of UPQC for load balancing, power-factor correction, current harmonic and voltage sag mitigation

The simulation results for voltage sag compensation are shown in Fig. 10. There are four instants; t_1, t_2, t_3 and t_4. At time t_1=0.10 s, the shunt APF is put into the operation and its operation is as discussed previously. At time t_2=0.20 s, series APF is put into operation. Now a 10 kW, 40 KVar (inductive) load is switched on at t=0.35 s and switched off at t=.045 sec. Because of this a sag is developed on the system at time t_3=0.35 s. This sag lasted till time t_4=0.45 s, as shown in Fig. 10 (a). After time t_4=0.45 s, the system is again at normal working condition. During this voltage sag condition, the series APF is providing the required voltage by injecting in phase compensating voltage equals to the difference between the reference load voltage and supply voltage, as shown in Fig. 10 (c). The load voltage profile in Fig. 10 (b) shows that UPQC is maintaining it at desired constant voltage level at load even during the sag on the system such that the loads cannot see any voltage variation. Because of unbalanced load, a current (i_{ln}) flows in the neutral conductor as shown in Fig.10 (i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.10 (h).

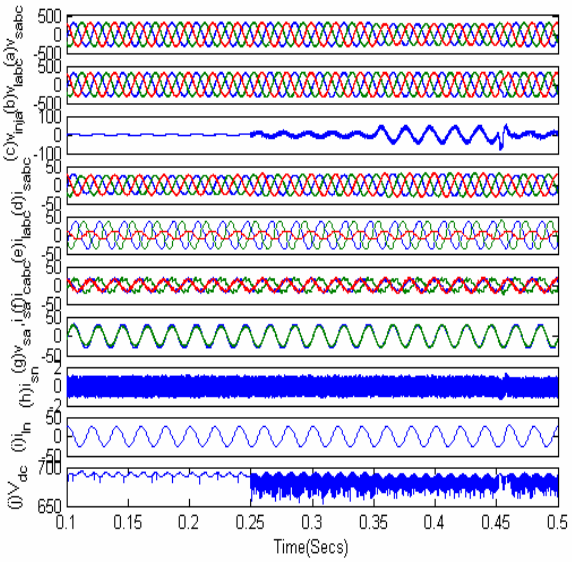


Fig. 10.Performance of UPQC for load balancing, power-factor correction, current harmonic and voltage sag mitigation

5.5 Performance of UPQC for load balancing, power-factor correction, current harmonic and voltage swell mitigation

At time t_1=0.10 s, the shunt APF is put into the operation and at time t_2=0.20 s, series APF is put into operation. A swell is now introduced on the system by switching on a 10 kW, 40 KVar (capacitive) from time t_3=0.35 s to t_4=0.45 s, as shown in Fig. 11. Under this condition the series APF injects an out of phase compensating voltage in the line through series transformers, equal to the difference between the reference load voltage and supply voltage, as shown in Fig.11 (c). The load voltage profile in Fig.11 (b)

shows the UPQC is effectively maintaining the load bus voltage at desired constant level. Fig.11 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.11 (h).

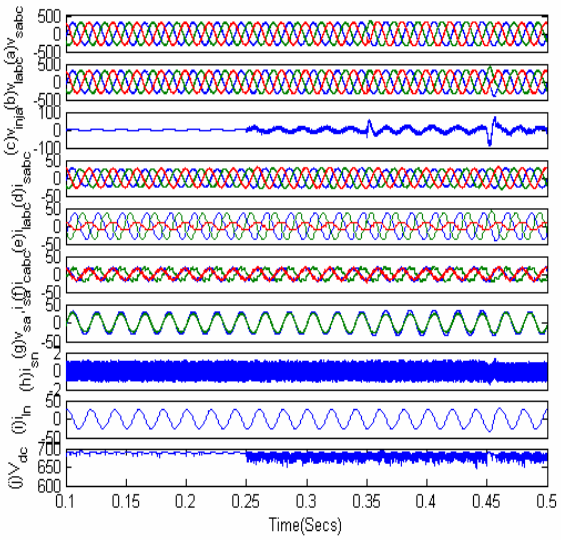


Fig. 11.Performance of UPQC for load balancing, power-factor correction, current harmonic and voltage swell mitigation

5.6 Performance of UPQC for power-factor correction and voltage dip mitigation

Fig 12 shows the response of the UPQC during the stat up of an induction motor. An induction motor load is a typical load on the supply system. An induction motor draws a heavy inrush current, which leads to a voltage dip. Both the shunt and series APF are switched on at 0.05sec. An induction motor load is connected at t=0.15sec.There is high inrush current during the starting of the induction motor as shown in Fig.12 (d). The series APF injects in phase compensating voltage equals to the difference between the reference load voltage and actual load voltage, as shown in Fig. 12 (c). The load voltage profile in Fig.12 (b) shows the UPQC is effectively maintaining the load voltage at desired constant level even during starting of an induction motor and there is no voltage dip. In addition to this, Fig.12 (g) shows that the voltage and current are in phase even during heavy inrush current.

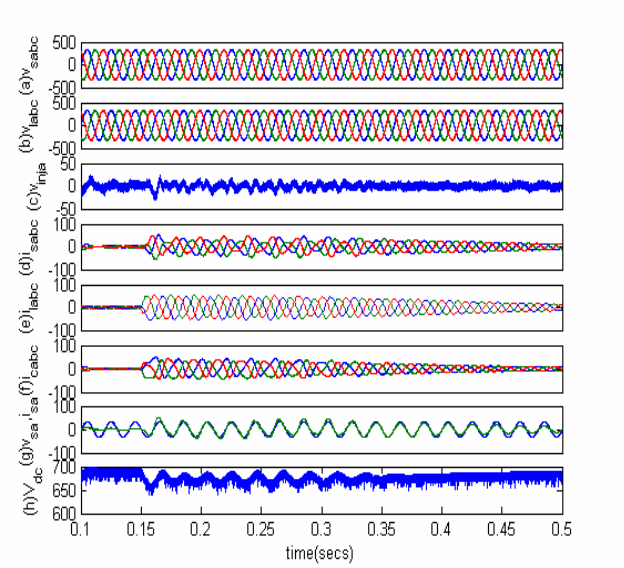


Fig. 12.Performance of UPQC for power-factor correction and voltage dip mitigation

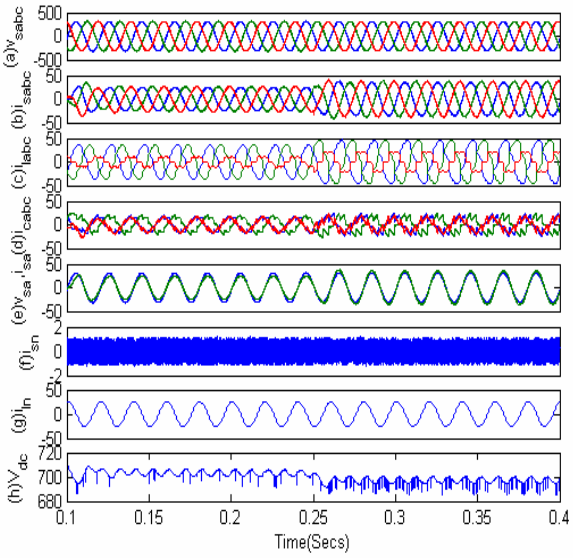


Fig. 13.Performance of UPQC during sudden load change

5.7 Performance of UPQC for sudden load change

In order to show the response of UPQC for sudden load change the load across the dc side of the rectifier is increased at t=0.25 s. It is observed from Fig.13(b) that in addition to the load balancing, power factor correction and current harmonic mitigation, the UPQC controller acts immediately without any delay in the operation and gain the new steady state. It is also observed from Fig. 13 (f) that there is small dip in dc

voltage at t=0.25 s, but dc link is able to regulate the dc voltage to its previous value. Fig.13 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.13 (h).

5. Conclusion

Realization of different power quality problems and their mitigation using three-phase four-wire UPQC has been validated using MATLAB software along with simulink and sim-power system toolbox. The performance of the proposed control strategy of UPQC has been observed to be satisfactory for various power quality improvements like load balancing; source neutral current mitigation, power-factor correction, voltage and current harmonic mitigation, mitigation of voltage sag , swell and voltage dip. The source current THD is improved from 15.30 % to 2.97 %, while the load voltage THD is improved form 6.26 % to 0.85 %. In addition to this the performance of UPQC has been found satisfactory during transient conditions.

Appendix

The system parameters used are as follows:

Supply voltage and line impedance: 415 V L-L, f=50 Hz, R_s=0.1ohm, L_s=1.5mH

Ripple Filter: R=7ohm,C=5μF

DC bus capacitance: C_{dc}=3000μF

Transformer: 250MVA, 58kV/12kV

K_p=2 and K_i=2

Loads: Two single-phase linear load of 12KW, 8KVar in phase ‘a’ and ‘b’ only and a Three-Phase Rectifier Load R=50 ohm on dc side.

Induction Motor Load: 3 HP, 50 Hz, 415 V L-L, wound rotor

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