

AN IMPROVED CURRENT SHARING METHOD FOR PARALLELED DC/DC CONVERTER USING FUZZY LOGIC CONTROL

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Abstract: This paper introduces a new fuzzy logic control application, associated mathematical theory and the concept and its advantages through comparative simulation with existing classical methods. A stable fuzzy logic controller for the master-slave current sharing loop of a paralleled DC-DC system is presented that exhibits a considerably improved large signal performance over the presently employed small signal designed compensators. Because of high system complexity, the present small signal designs are unable to give a good response for large load changes and line transients. Fuzzy logic, by dealing naturally with nonlinearities, offers a superior controller type for this type of applications. The design uses a type-2 compensator to derive the fuzzy inference rules, and simulation results show a good parameter insensitive transient response over a wide range load-step responses, e.g., from 25% to 50% of the nominal load. Current sharing control is formulated as a tracking problem.

Keywords–DC- DC converter, Fuzzy logic, current sharing control, paralleling.

1. Introduction

Paralleling operation of DC/DC converters is widely used in today's distributed power systems due to the request of high reliability and ease of standardization. Usually, it is desired to distribute the load equally among paralleled converters. However, because of limited component tolerances, as well as asymmetric layout or position of converters, their output currents might be significantly different. Therefore, special provisions are usually necessary to balance the load current equally among the paralleled modules. For this purpose, different current sharing control methods have been proposed and practiced by the industry [1-5].

Paralleling for both front-end and point of load (POL) converters, has been used successfully in various power systems. The paralleled modules can be centrally located to replace a centralized power supply. Such a configuration is often referred to as a modular power supply system. In a DPS with an

intermediate bus, paralleled modules can be used for the front-end and/or load converters. In either case,

paralleling is used to achieve the following characteristics: thermal management, reliability redundancy, modularity and maintainability [6]. However, it is the nature of voltage sources that only one unit can establish the voltage level in a paralleling system. The output resistances of the power supplies are extremely low. Thus, even a small difference in the output voltage between the paralleled modules will cause the one that is a few milli-volts higher to hog all the current. The lower the output voltage of the module, the more severe this problem is. Besides, even with the same voltage references, the steady-state current sharing error is determined by the difference of two parallel modules' output DC resistance [7-10].

2. State of Art

In the literature various current sharing methods[4-5] are proposed like passive droop current sharing method is accomplished by designing the individual power modules with a finite output resistance so that the output voltage falls slightly as the load current is increased. the voltage regulation has to be degraded to achieve fairly good current sharing, and it's difficult to achieve current sharing between modules with different power ratings [11].

Because of the aforementioned drawbacks regarding current sharing issues of the droop scheme, the active current sharing technique has been developed for systems requiring precise regulations. The basic feature of active current sharing methods is the existence of a current sharing bus communicating among the paralleled power modules. It usually provides a common current reference. Each module then adjust its own control to follow this common reference thus the load current will finally evenly distributed among these modules.

To avoid the conflict between voltage regulation and current sharing, the "master-slave" concept has been used since early 1980s. In a master-slave system, only one module is regulating the output voltage, while the others provide equal amount of the load

current[11-15]. After that, the democratic current sharing approaches are developed to improve the reliability of the system. From the system reliability aspect, the most attractive current sharing approaches are those providing desired current sharing accuracy without implementing a master-slave configuration or requiring a separate current-share controller. These “democratic” (also referred to as autonomous or independent) current sharing approaches, which allow each module to operate either as a stand-alone unit or in parallel with other modules, make it possible for the implementation of the true $N+1$ redundant system [16-19].

Generally, the democratic current sharing can be implemented using two approaches. The first approach is the passive droop method discussed in the previous section, which is simple to realize and does not require any communication among the paralleled modules. However, the major deficiency of the droop method, as demonstrated above, is the poor load regulation, which makes it not suitable for applications requiring tight output voltage regulations.

The other method ensures desired current sharing by active feedback controls. This current sharing technique requires a single-wire communication (current sharing bus) to provide the current reference for each module. Meanwhile, although each module must have its own voltage sensing and reference circuitry, they all need to be regulated to the same common output voltage level. Since there will always be differences between the individual voltage references – no matter how slight – this technique need to solve the voltage regulation conflict problem. There are many different means proposed in the past.

3. Modeling of Paralleled DC-DC Converter

This section introduces and elaborates design of paralleled DC/DC converter with Master-Slave control. The voltage regulated boost converter is the basic module in the considered paralleled converter system and “Type 2” compensator which is a classic current sharing controller. By taking Type 2 compensator as an expert, we design the rule base for fuzzy controller with the objective of deriving a new, improved, current sharing control method for master – slave type systems.

3.1. Design of Voltage Regulated Boost Converter

The basic module considered here is a boost converter with a voltage regulated loop. The small signal transfer function of a boost converter is given

as

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = V_{dc} \frac{D'}{L \cdot C} \cdot \frac{(1+s \cdot C \cdot R_c)}{\left(s^2 + s \left[\frac{R_{ld} + D'^2 \cdot R_c}{L} + \frac{1}{R_L \cdot C} \right] + \frac{D'^2}{L \cdot C} \right)} \quad (1)$$

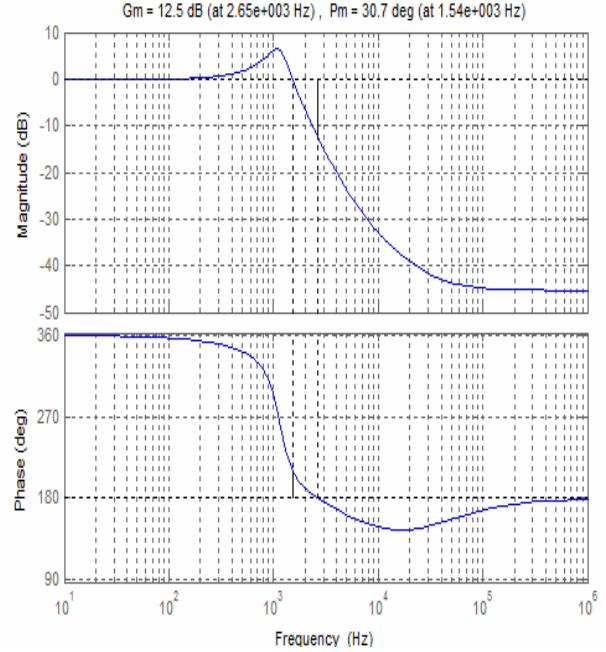


Figure.1 Gain and phase plot of uncompensated boost converter

The boost converter has a right hand zero which causes serious stability problems. So, designing of voltage regulated controller is a risky task. The boost converter considered has a supply voltage of 28V and gives an output voltage 48V with a load of 24A. The parameters of boost converter are as follows:

$L = 10\mu\text{H}$, $R_L = 20\text{m}\Omega$,

$C = 500\mu\text{F}$, $R_c = 10\text{m}\Omega$

Switching frequency $f_s = 200\text{ kHz}$

The gain and phase plot of the boost converter with above parameters is shown in figure 1. The uncompensated boost converter has a gain margin of 12.5dB and phase margin of 30.7deg. To regulate the output voltage, we go for voltage feedback with type 2 compensator. The type 2 compensator has following transfer function,

$$H(s) = k \cdot \frac{1}{s} \cdot \frac{s + w_z}{s + w_p} \quad (2)$$

The compensator adds a zero and two poles, one at origin and the other at higher frequencies. The compensator gives very high gain at lower frequency to reduce steady state error and a 20dB attenuation at

higher frequencies to reduce the effect of noise. At middle frequencies, it gives a sufficient phase lead which improves stability. The parameters of the compensator considered for voltage regulation are,
 $k = 10,587.6 \text{ rad/sec}$,
 $w_z = 1,851.9 \text{ rad/sec}$,
 $w_p = 85,185 \text{ rad/sec}$

The gain and phase plot of compensated boost converter are shown in figure 5.2. The compensated boost converter has a gain margin of 22.4dB and a phase margin of 95.9deg. so, the compensated converter is relatively more stable than the uncompensated and has good voltage regulation.

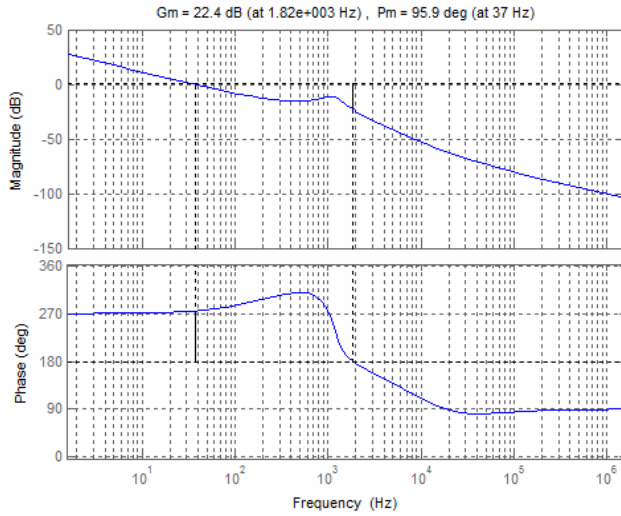


Figure.2 Gain and phase plot of compensated boost converter

3.2 Fuzzy Logic Controller Design using a Type 2 Compensator as Expert

Present control schemes make use of a “Type 2” compensator for the active current sharing loop. The transfer function of “Type 2” compensator is given in equation 3, same is taken here,

$$H(s) = k \cdot \frac{1}{s} \cdot \frac{s + w_z}{s + w_p} \quad (3)$$

The structure of Type 2 compensator is shown in figure.3, which is used as a common current sharing controller (CSC) in paralleled dc/dc converters.

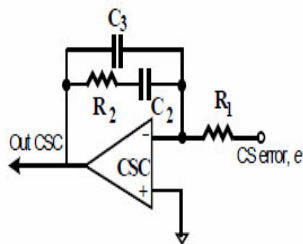


Figure. 3 Classical CSC structure

The parameters of CSC are,

$$k = 500 \text{ rad/sec},$$

$$w_z = 500 \text{ rad/sec},$$

$$w_p = 20,000 \text{ rad/sec}$$

This classic CSC results are used as an expert system in developing the consequents values, in the Inference rules section of the FLC. Figure 5.4 shows the block diagram of a generic FLC, which uses the current share error, e , into a PD fuzzy scheme.

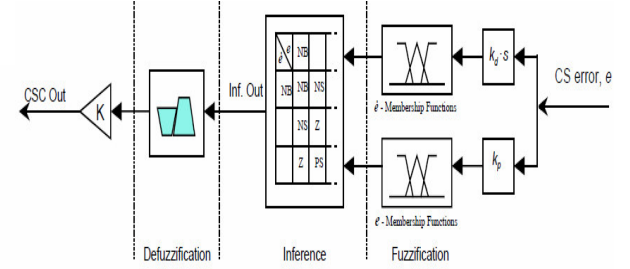


Figure. 4 Fuzzy logic implementation of CSC

A seven range partition, Negative Big (NB), Negative Medium (NM), Negative Small (NS), zero (Z), Positive Small (PS), Positive Medium (PM), Positive Big (PB) can be chosen for the inputs, e , de and output.

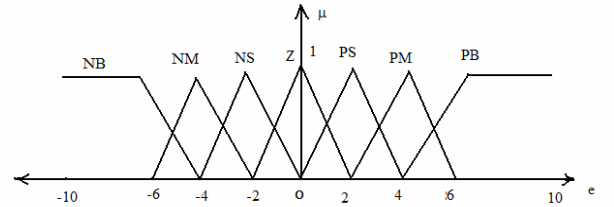


Figure.5 Membership functions for e , de and output error (e)

Based on the usual action of a PD cell, by looking at its output range as a function of the input range, a rule-based inference is chosen for each consequent; the membership functions and respective rules are shown in figure 5 and table 1

Table I : Rule Table of the Fuzzy Controller

| Error (e) | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|
| Derivative Error (de) | | NB | NM | NS | Z | PS | PM | PB |
| | NB | NB | NB | NB | NB | NM | NS | Z |
| | NM | NB | NB | NM | NM | NS | Z | PS |
| | NS | NB | NM | NS | NS | Z | PS | PM |
| | Z | NB | NM | NS | Z | PS | PM | PB |
| | PS | NM | NS | Z | PS | PS | PM | PB |
| | PM | NS | Z | PS | PM | PM | PB | PB |
| | PB | Z | PS | PM | PB | PB | PB | PB |

We employ a Mamdani fuzzy inference engine, Triangular fuzzifier and centroid defuzzifier. The inner membership functions are triangular and outer membership functions are trapezoidal, laid out symmetrical within the ranges for each variable's universe of discourse, i.e., e , de and the output of the inference section respectively. The range of e, de and output are decided between -10 and 10 by simulating the system in MATLAB with classical CSC. The gain block K is the general gain used for the output of the FLC, being adjusted depending on each application case. The surface viewer of the rule table 1 is shown below.

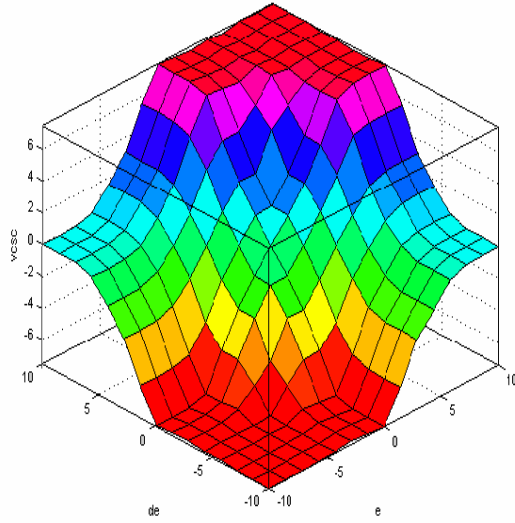


Figure 6 Surface viewer of the rule table I

4. Implementation of fuzzy logic control

This section shows the implementation and simulated results for fuzzy logic control [20] of two parallel DC/DC boost converters, designed based on the concepts introduced and analyzed in all previous chapters. The simulated results show good current sharing among the paralleled converters with fuzzy current sharing control compared to classical CSC.

4.1. Individual Converter Module Design Analysis

The DC/DC converter used in the simulation is a boost converter that is supplied from 28V input voltage and delivers a 48V output voltage at 24A load; these used to be traditional aerospace bus lines applications. The modules are chosen with relevant parasitics and tolerances, as listed below, so the effect of the unmatched parameters is present, which is even more important in the paralleled system. Their nominal values are $f_s = 200$ KHz, $L = 10\mu\text{H}$, $R_L = 20\text{m}\Omega$, $C = 500\mu\text{F}$, $R_C = 10\text{m}\Omega$. The internal loop compensator has the same architecture as the CSC in

Figure 7 and, after design, has the parameters: $k = 10,587.6$ rad/sec, $w_z = 1,851.9$ rad/s, $w_p = 85,185$ rad/s. In the large signal simulations, the OpAmp compensators are assumed supplied from 12V and operate around a reference voltage of 6V.

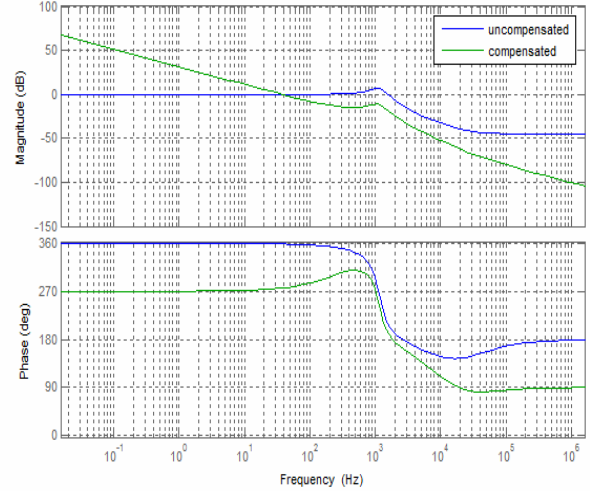


Figure 7 Gain and phase plot of uncompensated and compensated single converter module.

Figure 7 shows the gain and phase plot of compensated and uncompensated individual converter module. From figure 7, the compensated system has improved gain and phase margin.

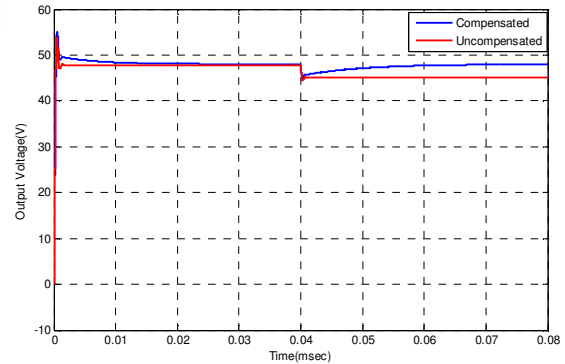


Figure 8. Comparison of output voltage of uncompensated and compensated individual converter module.

The closed loop system has very high DC gain which helps to reduce the steady state error and has steep attenuation at higher frequencies which reduces the effect of noise. The compensated converter is relatively more stable than the uncompensated one. The comparison of output voltage of uncompensated and compensated is shown in figure 8.

The uncompensated system didn't regulate its output voltage when the load increased by a step of 50% of nominal load at 40 msec, but the compensated system regulated its output voltage as

shown in figure 8. So, the voltage compensator design is satisfied. This compensated converter is used as basic module in the paralleled DC/DC converters in the next section.

4.2 Paralleled System

The Master-Slave control technique is used for proper current sharing. Figure 9 shows the generic MSC scheme with converter #1 as master.

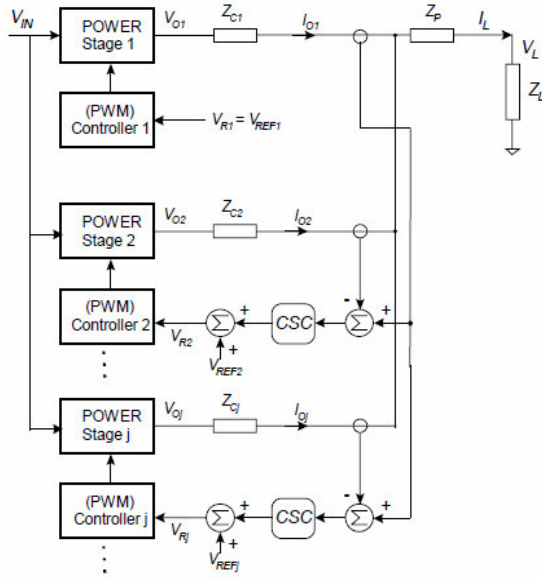


Figure 9 Control scheme used for paralleling N converter modules with MSC [21]

The difference of Master converter current and Slave converter is given as input to the current sharing converter and the output of current sharing converter is used to modify the reference to the Slave converter so that the Slave converter can track the Master converter current. The output voltage is regulated by the Master converter only whose V_{ref} is maintained constant for a constant output voltage.

The structure of classical current sharing compensator is shown in figure.3 and the transfer function is given in (1). The parameters of classical CSC considered are

$$\begin{aligned} k &= 500 \text{ rad/sec,} \\ \omega_z &= 500 \text{ rad/sec,} \\ \omega_p &= 20,000 \text{ rad/sec} \end{aligned}$$

Figure 10 shows total current and individual currents of two voltage regulated converters which are connected in parallel to share a load of 48A without current sharing compensator. Because of the difference in output impedance, the two converters

share 48A unequally. When the load increased by 50% at 30msec, the difference in currents of two converters is more, then the converter which is sharing more current may damage. Figure.11 shows the difference in currents of the two converters.

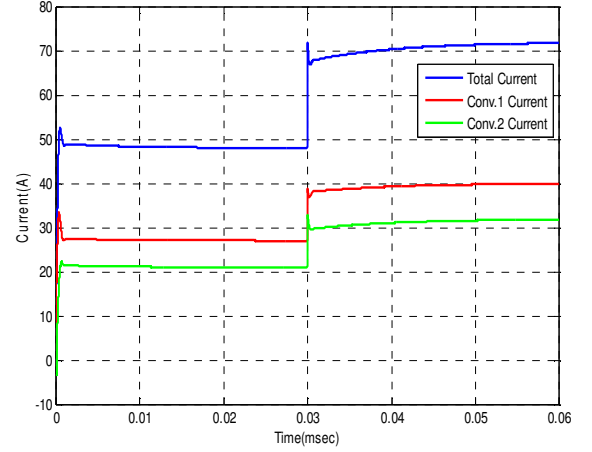


Figure 10 Total current and currents shared by individual converters connected in parallel without current sharing compensator.

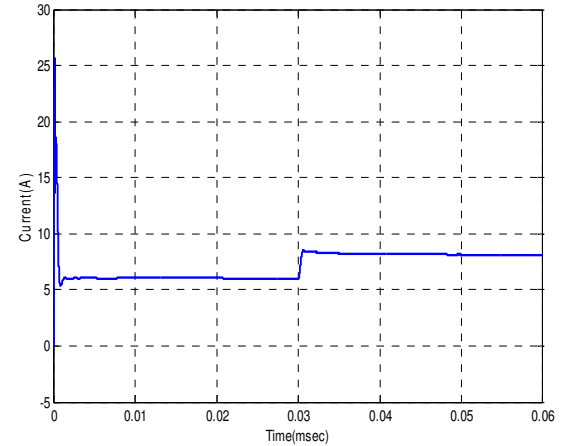


Figure 11 Difference in currents of two converters connected in parallel without CSC

Figure 12 shows total current and individual currents of two voltage regulated converters which are connected in parallel to share a load of 48A with classical current sharing compensator. The Slave converter can track master converter current in steady state, but in transient period, the difference in currents is considerable. The current sharing is good in steady state even when the load increased by 50% at 30 msec. Figure 11 shows the difference in currents of the two converters. The difference in currents is zero in steady state i.e., the two converters share total load equally.

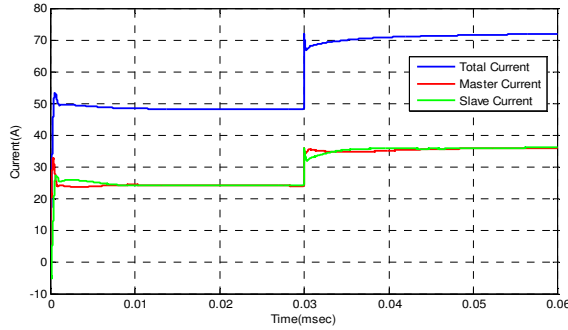


Figure 12 Total current and currents shared by individual converters connected in parallel with classical current sharing compensator.

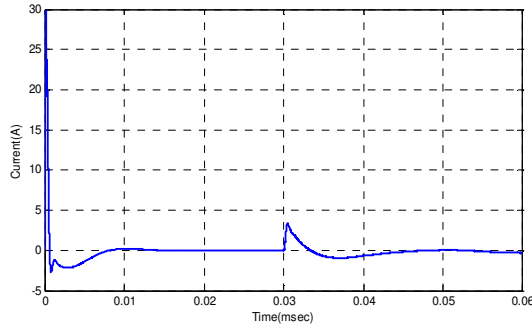


Figure 12 Difference in currents of two converters connected in parallel with classical CSC

Figure 13 shows total current and individual currents of two voltage regulated converters which are connected in parallel to share a load of 48A with fuzzy current sharing controller. The tracking ability of Slave converter in transient period is very much improved compared to the previous case. The current sharing is good even when the load increased by 50% at 30 msec. Figure 14 shows the difference in currents of the two converters. The difference in currents is vanished very quickly.

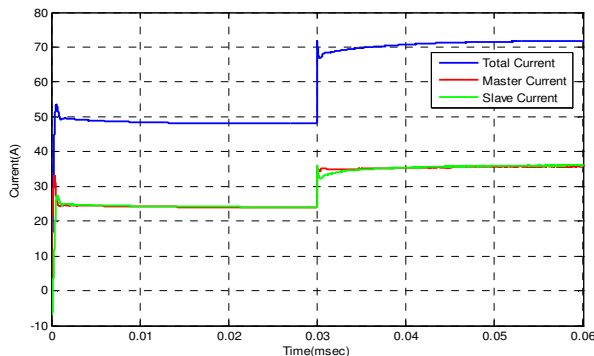


Figure 13 Total current and currents shared by individual converters connected in parallel with fuzzy logic current sharing controller.

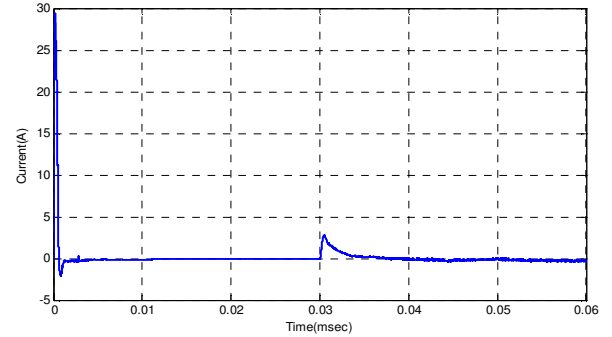


Figure 14 Difference in currents of two converters connected in parallel with fuzzy logic current sharing controller.

Figure 15 shows the comparison of Master and Slave converter currents with fuzzy current sharing controller and classical current sharing controller for 25% step increase in nominal load current. The results show that fuzzy controller gives a better transient response compared to classical current sharing controller. Therefore, the analysis done in chapter 3 is verified with simulation results.

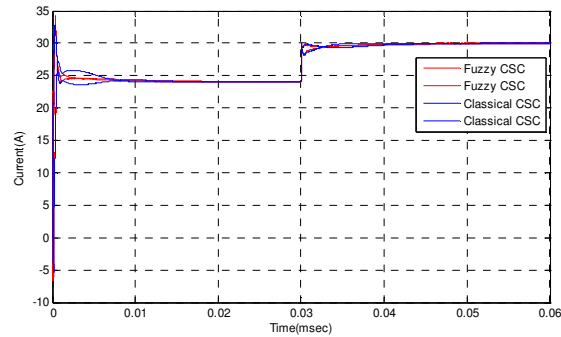


Figure 15 Comparison of Master and Slave converter currents with fuzzy current sharing controller and classical current sharing controller for 25% step increase in nominal load current.

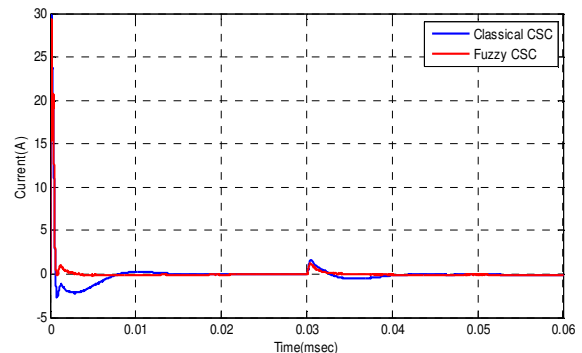


Figure 16 Comparison of Difference in currents of two converters connected in parallel with classical and fuzzy logic CSC for 25% step increase in nominal load.

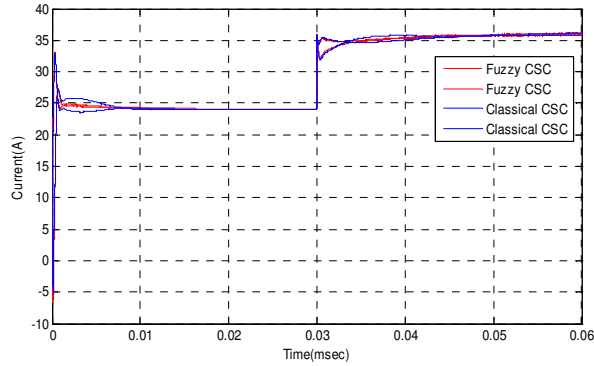


Figure 17 Comparison of Master and Slave converter currents with fuzzy current sharing controller and classical current sharing controller for 50% step increase in nominal load.

Figure 17 shows the comparison of Master and Slave converter currents with fuzzy current sharing controller and classical current sharing controller for 25% step increase in nominal load current. The results show that fuzzy controller gives a better transient response compared to classical current sharing controller.

Figure 18 shows the comparison of difference in currents of two converters connected in parallel with classical and fuzzy logic CSC for 50% step increase in nominal load.

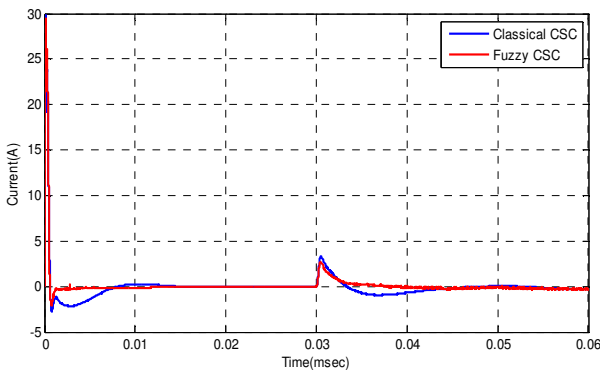


Figure 18 Comparison of Difference in currents of two converters connected in parallel with classical and fuzzy logic CSC for 50% step increase in nominal load.

5. Conclusion

The primary subject and contribution of this paper is to introduce, analyze and design fuzzy logic controllers for the current sharing compensator of master-slave DC/DC paralleled converter systems. Even though explored in the past for individual modules, no investigation had yet been done for applying the same concept to the more complicated parallel system; the work here offers the novel study

in this direction. Individual converter modules are well established in the industry in terms of control implementation and size, where a complex digital controller does not offer a viable alternative. However, in the case of large, distributed systems, due to their complex, nonlinear behaviour, especially for large load and line variations, modern digital controllers are fully justified and needed during the next generation of improved DC/DC power conversion and management.

The implementation offers a significantly improved performance over solidly developed classical OpAmp designs. One approach is to first introduce a “Type 2” OpAmp compensator and then, to employ the “Type 2” compensator as an expert system in partially developing the rules for the Fuzzy Logic Controller. A substantial improvement in the transient performance and control effort is noted in the case of the fuzzy logic controller. The simulation results show a very good parameter insensitive transient response in load step responses from 25% to 50% of the nominal load. The technique benefits also from the heuristic approach to the problem that overcomes the complexity in modeling such systems and, hence, offers a practical engineering tool, amenable to both analog and digital implementations. Almost identical responses for widely different step load cases, when using the FLC, shows its validity in dealing naturally with the nonlinear character of the system.

6. Future Scope

Based on extensive experience, the simulated results give a high degree of confidence that the proposed fuzzy logic control methods will work successfully in practice. However, it will be of interest in a future research path, to implement in hardware some of the control schemes that were proposed. The experimental work will undoubtedly generate new research directions as well as exposing some limitations.

As part of any practical design, one should consider also the effects of highly unmatched parameters among the different converters. This can include the case when different power levels and topology designs are employed and analyze not only the nominal case but include also the situation when one or several modules would fail or go into current limiting, for example.

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References

1. J.D. van Wyk, F.C. Lee: *Power Electronics Technology at the Dawn of the new Millennium-Status and Future* In: Proc. of IEEE PESC'99, Vol. 1, pp. 3–13.
2. W. A. Tabisz, M. M. Jovanovic, and F. C. Lee: *Present and future of distributed power systems* In: Proceedings of IEEE APEC, 1992, pp. 11–18.
3. F. C. Lee, P. Barbosa, P. Xu, J. Zhang, B. Yang, and F. Canales: *Topologies and design considerations for distributed power system applications* In : Proceedings of IEEE, vol. 89, no. 6, Jun. 2001, pp. 939–950.
4. S. Luo, Z. Ye, R. L. Lin, and F. C. Lee: *A classification and evaluation of paralleling methods for power supply modules* In: Proceedings of IEEE PESC, 1999, pp. 901–908.
5. B. Choi: *Comparative study on paralleling schemes of converter modules for distributed power applications* In : IEEE Transactions on Industrial Electronics, vol. 45, no. 2, Apr. 1998, pp. 194–199.
6. B. T. Irving and M. M. Jovanovic : *Analysis, design and performance evaluation of droop current-sharing method* In : Proceedings of IEEE APEC, 2000, pp. 235–241.
7. R. Wu, T. Kohama, Y. Koderu, T. Ninomiya, and F. Ihara: *Load-current-sharing control for parallel operation of DC-DC converters* In: Record of IEEE PESC, 1993, pp. 101–107.
8. K. Siri, C. Q. Lee, and T. F. Wu: *Current distribution control for parallel connected converters: part I* In: IEEE Transactions on Aerospace and Electronic Systems, vol. 28, no. 3, Jul. 1992, pp. 829–840.
9. K. Siri, C. Q. Lee, and T. F. Wu: *Current distribution control for parallel connected converters: part II* In : IEEE Transactions on Aerospace and Electronic Systems, vol. 28, no. 3, Jul. 1992, pp. 841–851.
10. M. M. Jovanovic, D. E. Crow, and F.-Y. Lieu: *A novel low-cost implementation of 'democratic' load-current sharing of paralleled converter modules* In: IEEE Transaction on Power Electronics, vol. 11, no. 4, Jul. 1996, pp. 604–611.
11. R. Tymerski, D. Li: *State-Space Models for Current Programmed Pulsewidth- Modulated Converters* In: IEEE Trans. PE, Vol. 8, No. 3, July 1993, pp. 271 – 278.
12. S. Hiti and D. Borojevic: *Robust Nonlinear Control for Boost Converter* In: IEEE Trans. PE, vol. 10, No.6, November 1995, pp.651 – 658.
13. B. Tomescu and H.F. VanLandingham: *Disturbance Rejection and Robustness Considerations in DC/DC Converters* In: IEEE PESC Proc., Charleston, SC, June 1999, pp. 1204 – 1210.
14. V.J. Thottuvelil and G. Verghese: *Analysis and Control Design of Paralleled DC-DC converters with current sharing* In : Proc. of APEC 97, pp. 638–646.
15. Y. Panov, J. Rajagopalan and F.C. Lee: *Analysis and Design of N Paralleled DC-DC Converters with Master-Slave Current Sharing Control* In: Proc. of APEC 97, pp. 436–442.
16. J. Rajagopalan, K. Xing, Y. Guo and F.C. Lee: *Modeling and Dynamic Analysis of Paralleled DC/DC Converters with Master/Slave Current Sharing Control* In : Proc. APEC'96, pp. 678–684.80
17. V. J. Thottuvelil and G. C. Verghese: *Stability analysis of parallel DC/DC converters with active current sharing* In : Proceedings of IEEE PESC, 1996, pp. 1080–1086.
18. P. Mattavelli, L. Rossetto, G. Spiazzi, P. Tenti: *General - Purpose Fuzzy Controller for DC/DC Converters* In : IEEE PESC 1995 Record, pp. 723 - 730.
19. F. Ueno, and al.: *Regulation of Cuk Converters using fuzzy Controllers* In: Proc. Intelec'91, pp. 261 - 267.
20. W.-C. So, C.K. Tse and Y.-S. Lee: *Development of a Fuzzy Logic Controller for DC/DC Converters: Design, Computer Simulation and Experimental Evaluation* In: IEEE Trans. PE, vol. 11, No.1, January 1996, pp. 24 - 32.
21. B. Tomescu and H.F. VanLandingham: *Improved Large Signal Performance of Paralleled DC/DC Converters Current Sharing Using Fuzzy Logic Control* In: IEEE Trans. PE, vol. 14 No. 3, May 1999, pp. 573–577.
22. S. N. Sivanandam, S. Sumathi and S. N. Deepa: *Introduction to Fuzzy Logic using MATLAB* In: Springer- Verlag Berlin Heidelberg 2007.
23. *MATLAB 7.4 Documentation and help files.*

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