

COMPARATIVE ASSESSMENT OF PWM STRATEGIES FOR THREE PHASE TRINARY SOURCE NINE LEVEL INVERTER WITH RECTIFIED SINE CARRIERS

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Abstract: This paper presents the performance assessment of various bipolar rectified sine Multi-Carrier Pulse Width Modulation (MCPWM) strategies with Trapezoidal reference for three phase Nine level cascaded Trinary Source multilevel inverter (TSMLI). TSMLI have been developed using MATLAB-SIMULINK and tested for different modulation indices 0.8-1 and real time implementation for same modulation strategies have been carried out using Field-Programmable Gate Array (FPGA) and results are presented and analyzed. The most popular cascaded multilevel inverter exhibits several other attractive features such as simple circuit layout, less component counts and modular structure which prevents unbalance in capacitor voltage. Two unequal Direct Current (DC) sources in the ratio 1:3 with twenty four switches are used in the chosen three phase trinary source multilevel inverter which produces nine voltage levels at the output whereas the conventional symmetric three phase nine level inverter uses 48 switches. Performance factors such as Percentage Total Harmonic Distortion (%THD), Voltage Root Mean Square (VRMS) where measured and harmonic spectra Percentage Distortion Factor (%DF) of output voltage are calculated for above different modulation indices. The results are compared both virtually and experimentally which reveals that Phase Disposition Pulse Width Modulation (PDPWM) strategies provides low THD and less Distortion Factor (DF) whereas Carrier Overlapping Pulse Width Modulation (COPWM) strategy is found to perform better since it provides relatively higher fundamental VRMS output voltage.

Key words: Rectified Sine, THD, MCPWM, Bipolar, minimum switches, FPGA.

1. Introduction.

Multilevel inverters have been extensively used in high power applications because they can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. In conventional multilevel inverters, the DC voltages of each cell are equal. However it is possible to have unequal DC voltages, which increase the number of voltage levels without increasing the number of switches and such configuration, is called as asymmetrical multilevel inverter. The trinary nine level inverter chosen with this work has 1:3 DC source

voltage ratios. The trinary multilevel inverter generates nine level output voltage without any supplemental complexity to the existing topology with asymmetrically distributed DC source voltages. Amir Farakhor et al [1] portrayed symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components. Ataollah et al [2] developed symmetric and asymmetric design and implementation of new cascaded multilevel inverter. Balamurugan et al proposed advanced references and carriers based PWM in a symmetrical multilevel inverter and explained control techniques for various bipolar PWM strategies of three phase five level cascaded inverter in [3,4]. Ebrahim et al [5] designed a new cascaded multilevel inverter using sub-multilevel cells. Espinosa et al [6] depicted a new modulation method for a 13-level asymmetric inverter toward minimum THD. Euzeli et al [7] discussed about nested multilevel topologies. Ilhami Colak et al [8] proposed a review of multilevel voltage source inverter topologies and control schemes. Jin-sung choi and Feel-Soon Kang [9] presented seven-level PWM inverter employing series connected capacitors paralleled to a single DC voltage source. Krishna Kumar Gupta and Shailendra Jain introduced a novel multilevel inverter based on switched D.C sources, various topologies for multilevel inverters to attain maximum number of levels from given D.C sources and also made a comprehensive review of a recently proposed multilevel inverter in [10, 11 & 12]. Mohammad et al presented a generalized cascaded multilevel inverter topology using series connection of sub multilevel inverters and a cross-switched multilevel inverter in [13,14]. Banaei et al discussed reconfiguration of semi-cascaded multilevel inverter to improve systems performance parameters in [15]. Prathiba and Renuga described about the performance analysis of symmetrical and asymmetrical cascaded H-bridge inverters in [16]. Rajasekar et al [17] developed hybrid multi-carrier modulation to reduce leakage current in a transformer less cascaded multilevel inverter for photovoltaic systems. Rosli Omar et al [18] presented a survey of multilevel inverter based on cascaded H-bridge topology and control schemes.

Sureshpandiarajan et al [19] discussed about the assessment of fixed and variable amplitude bipolar carriers for a single phase ternary multilevel inverters. This paper aims at comprehensively analysing the proposed topology three phase nine level cascaded Trinary DC source multilevel H-bridge inverter using various bipolar Trapezoidal PWM Strategies with Rectified Sine Carrier. In this paper, the aforesaid topology was developed using MATLAB-SIMULINK.

2. Three phase nine level cascaded trinary DC source multilevel inverter

The fundamental H-Bridge cascaded topology increases the number of components required, which in turn makes the design complexity and increases the cost. It is also to be establishing that the maximum output voltage cannot go beyond the sum of voltage of individual sources which becomes the most important setback of this topology. Because of the foresaid reason in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers. To accomplish this problem a new topology proposed is shown in Fig.1 to reduce component count.

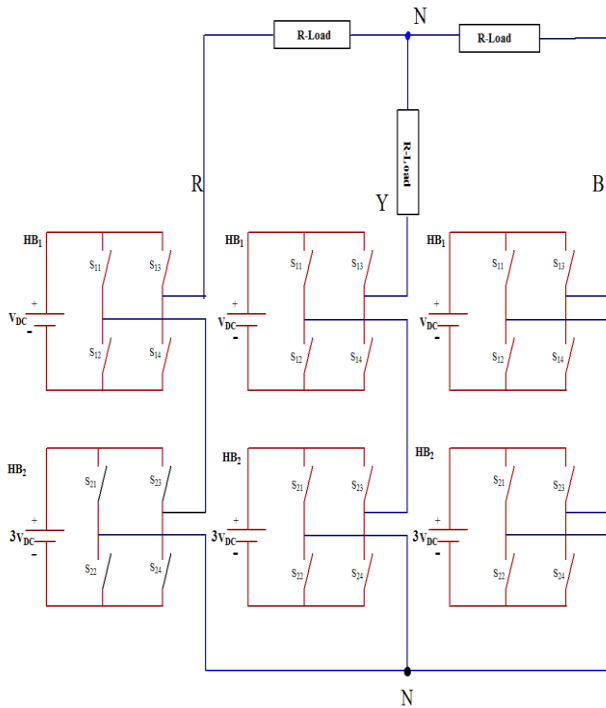


Fig.1. Three phase trinary source nine level inverter

Fig.1 shows the topology of the proposed three phase nine level cascaded TSMLI. The chosen trinary nine level inverter consist of two H-bridges that are connected in series to achieve the desired number of output voltage levels. Each H-bridge has its own DC

source (VDC and 3VDC) and consists of four power devices designated as S11, S12, S13 and S14 for the upper H-bridge HB1 and as S21, S22, S23 and S24 for the lower H-bridge HB2 (Fig.1). The upper H-bridge generates a fundamental output voltage with three levels, and then the lower H-bridge adds or subtracts one level from the fundamental wave to synthesize stepped waves. The final output voltage levels are the sum of terminal voltage of each H-bridge. Table.I lists the output voltage for one phase with the corresponding switching states. It views like a conventional cascaded H-bridge multilevel inverter apart from input DC sources. The topology comprises of floating input DC sources connected through power switches. The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. By using VDC and 3VDC, it can synthesize nine output levels; -4VDC, -3VDC, -2VDC, -VDC, 0, VDC, 2VDC, 3VDC and 4VDC. The lower inverter generates an elementary output voltage with three levels and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. At this point, the final output voltage level becomes the sum of each terminal voltage of H-bridge [1] and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

In the proposed circuit design, suppose the n number of H-bridge component has self-governing DC sources in sequence of the power of 3, a predictable output voltage level is given as

$$V_n = 3^n, n = 1, 2, 3, \dots \dots \dots (2)$$

Where; n is number of H bridge Switching functions of the upper H-bridge inverter (HB1) and the lower H-bridge inverter (HB2) are expressed respectively. Waveforms of output voltage are denoted as (Vout), upper terminal voltage is (VHB1) and the lower voltage is (VHB2) inverter in sequence. The output voltage has nine levels include zero level. Though it is close to a sinusoidal wave, it has lower order harmonics. So it needs more H-bridge modules or output filter to obtain high quality output voltages. Advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic

power generating systems equipped with distributed power sources.

Table I. Switching states and output voltage levels of one phase of trinary source nine level inverter

S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	$V_{out}(1\Phi)$
1	0	0	1	1	0	0	1	$+4V_{DC}$
0	1	0	1	1	0	0	1	$+3V_{DC}$
0	1	1	0	1	0	0	1	$+2V_{DC}$
1	0	0	1	0	1	0	1	$+V_{DC}$
0	1	0	1	0	1	0	1	0
0	1	1	0	0	1	0	1	$-V_{DC}$
1	0	0	1	0	1	1	0	$-2V_{DC}$
0	1	0	1	0	1	1	0	$-3V_{DC}$
0	1	1	0	0	1	1	0	$-4V_{DC}$

3. Multicarrier Trapezoidal Pulse Width Modulation Strategies

The most popular method of controlling the output voltage is by incorporating Pulse Width Modulation (PWM) control within the inverters. In this paper four different modulation strategies are introduced in order to increase the output voltage and also to reduce the THD in which the fixed DC is converted into continuous Alternating Current (AC) signal efficiently by controlling the ON and OFF time of PWM signal. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonics. This paper includes reference waveform as trapezoidal and m-1 rectified sine carriers. To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the TSMLI. Among all the PWM methods for cascaded TSMLI, carrier based PWM methods and space vector methods are often used but when the number of output levels is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM method is preferred under this condition in TSMLI. This paper focuses on carrier based PWM strategies which have been extended for use in TSMLI by using multiple carriers. MCPWM strategies have more than one carrier that can be triangular waves or sawtooth waves and so on. The carrier waves can be either bipolar or unipolar. In this paper, a comprehensive analysis of the aforementioned topology is carried out using bipolar MCPWM strategies. The modulating/reference wave of multicarrier based PWM strategy is trapezoidal in this paper but it can be sinusoidal also. In this paper, various multicarrier PWM strategies like

Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and Carrier Overlapping (CO) are proposed for three phase nine level cascaded TSMLI. Several Control Freedom Degrees (CFDs) exist in MCPWM strategies for (Multi-Level Inverters) MLIs. These strategies have more than one carrier option that can be triangular, saw tooth, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFDs including function, frequency, amplitude, phase of each carrier and offset between carriers. CFDs exist for references also. This paper presents RSC based bipolar PWM strategies with trapezoidal references. To generate m levels, (m-1) carriers are needed in multi-carrier bipolar PWM strategies. They have the same peak to peak amplitude of carrier signal (A_c) and the carrier frequency (f_c). The reference wave has a modulating frequency/frequency of reference signal (f_m) and an peak amplitude of modulating signal (A_m). At each instant the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level. This paper employs PDPWM, PODPWM, APODPWM and COPWM strategies to get nine level output voltage from chosen TSMLI.

Fig.(2-5) shows the bipolar fixed amplitude multiple carrier pattern for rectified sine carrier. In this paper, rectified sine carrier can be generated by using (i) sinusoidal voltage source and rectifier blocks in simpower system module of SIMULINK or (ii) sine wave generator block and s-function based rectifier block and latter technique is employed in this work. For an m-level inverter using bipolar multicarrier strategy, $(m-1)$ carriers with same carrier frequency f_c and same peak-to-peak amplitude of carrier signal A_c are used. The reference waveform has amplitude A_m and frequency f_m are placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio (m_f) is the ratio of carrier frequency and modulating frequency, $m_f = 40$ and modulation index m_a is varied from 0.8 to 1

$$m_f = \frac{f_c}{f_m} \quad (3)$$

$$m_a = 2A_m / (m-1)A_c \quad (4) \text{ Except for COPWM}$$

a) Phase Disposition (PD) PWM Strategy

The principle of the PDPWM strategy is to use

several carriers with single reference wave. The carriers of same frequency and same peak-to-peak amplitude are disposed so that the bands they occupy are contiguous. The modulating wave of the fundamental frequency is placed at zero reference. The carrier set is placed above and below the zero reference. If the reference is greater than a carrier signal, then the active devices corresponding to that carrier are switched on, otherwise the devices switch off. The carrier arrangement for Phase Disposition PWM strategy having trapezoidal reference with rectified sine carrier is shown in Fig.2. for $m_a = 0.9$ and $m_f = 40$.

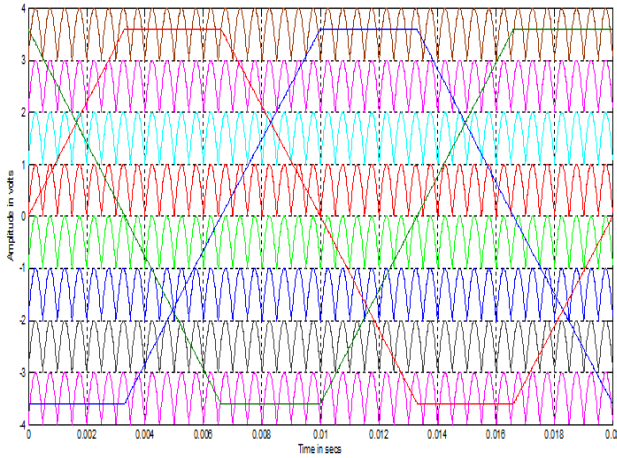


Fig.2. Carrier arrangement for PDPWM Strategy

b) Phase Opposition and Disposition (POD) PWM Strategy

In PODPWM strategy, the carrier waveforms above the zero reference value are in phase and the carrier waveforms below zero are in phase but are 180° phase shifted from those above zero. PODPWM strategy is illustrated in Fig.3 for the chosen reference. Fig.3 shows the multicarrier arrangement for PODPWM method for $m_a = 0.9$ and $m_f = 40$.

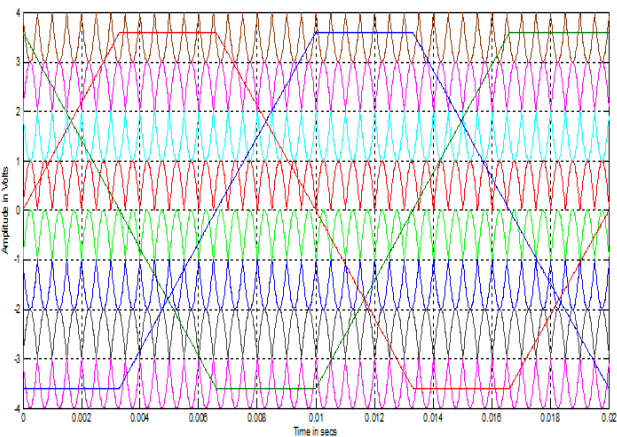


Fig.3. Carrier arrangement for PODPWM Strategy

c) Alternative Phase Opposition and Disposition (APOD) PWM Strategy

In APODPWM strategy, the carriers of same amplitude and same frequency are arranged in such a manner that each carrier is out of phase with its neighbor by 180° . Figs.4 show the carrier arrangement for APODPWM strategy for $m_a = 0.9$ and $m_f = 40$.

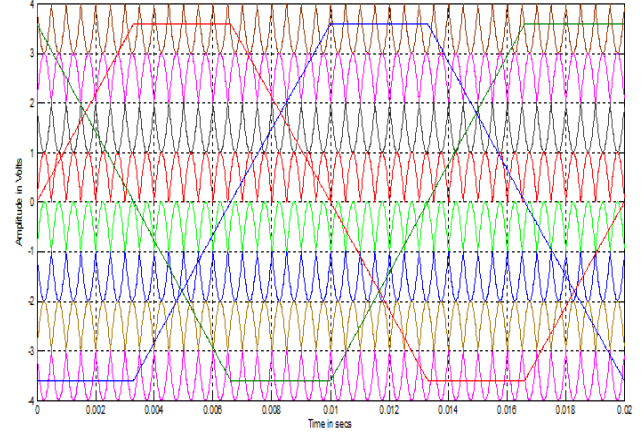


Fig.4. Carrier arrangement for APODPWM Strategy

d) Carrier Overlapping (CO) PWM Strategy

The principle of COPWM is to use several overlapping carriers with single modulating signal. The carriers having same frequency and same peak-to-peak amplitude are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$ in this work. The vertical offset of rectified sine carrier for chosen TSMLI having trapezoidal reference is illustrated in Fig.5 for $m_a = 0.9$ and $m_f = 40$.

The amplitude modulation index:

$$m_a = \frac{A_m}{(2.5) A_c} \quad (5)$$

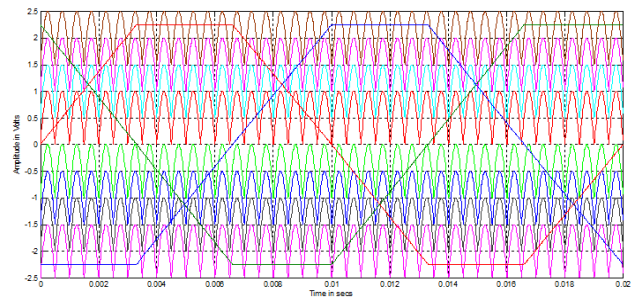


Fig.5. Carrier arrangement for COPWM Strategy

4. Simulation Results

A three phase nine level TSMLI is modeled in SIMULINK by using power system block set. Switching signals for chosen inverter were developed using different MCPWM strategies discussed

previously. Simulations are carried out for different values of m_a ranging from 0.8 – 1. The chosen TSMLI does not provide the specified number of output voltage levels for m_a less than 0.8. The %THD and RMS values of output voltage for different values of m_a are measured using Fast Fourier Transform (FFT) block of SIMULINK and tabulated. The simulation results presented in this work in the form of the PWM outputs and FFT plot of chosen TSMLI are compared and evaluated. Percentage Distortion Factor (%DF) and harmonic spectra are also evaluated. Results are displayed only for a sample $m_a = 0.9$ for all the chosen references but only for the PWM strategy which provides relatively less THD. Figs.6 and 7 respectively show the nine level output voltage generated by PDPWM strategy with trapezoidal reference and its FFT plot. Figs. 8 and 9 respectively show the nine level output voltage generated by PODPWM strategy with trapezoidal reference and its FFT plot. Figs. 10 and 11 respectively show the nine level output voltage generated by APODPWM strategy with trapezoidal reference and its FFT plot. The comparison of %THD of output voltage with different PWM switching strategies for various values of modulation index obtained through simulation are shown in Table II and Fig. 14. Variations of Root Mean Square (RMS) value of fundamental output voltage (a measure of DC bus utilization) for various modulation indices are listed in Table IV. Table III shows the DF of the output voltage and Table V shows the harmonic contents of output voltage for a sample value of $m_a = 0.9$. The following parameters values are used for simulation: $V_{DC} = 100V$, $R(\text{load}) = 100\text{ohms}$, $f_c = 2000\text{ Hz}$ and $f_m = 50\text{ Hz}$.

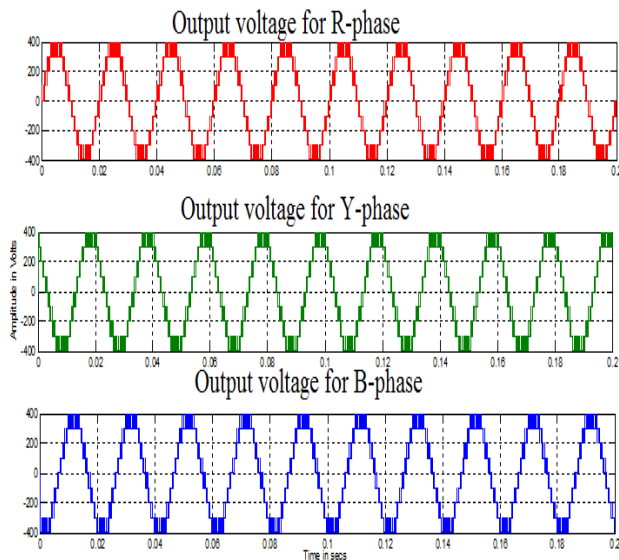


Fig.6.Output Voltage generated by PDPWM Strategy

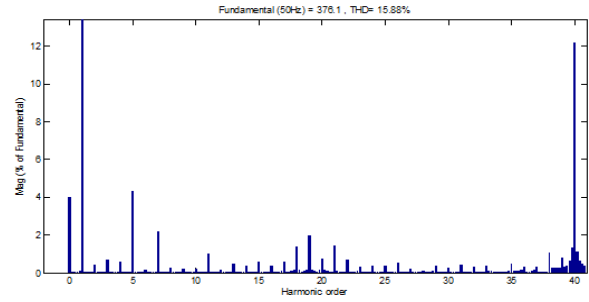


Fig.7.FFT Plot for Output Voltage of PDPWM Strategy

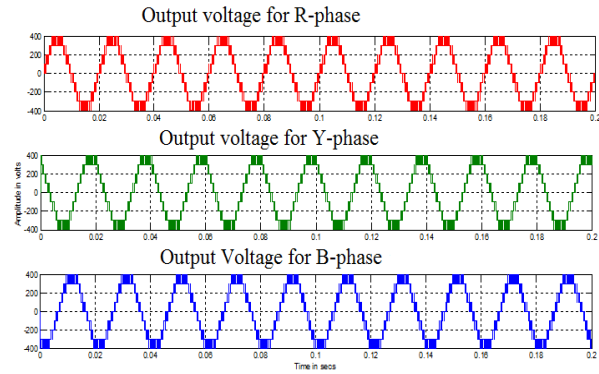


Fig.8.Output Voltage generated by PODPWM Strategy

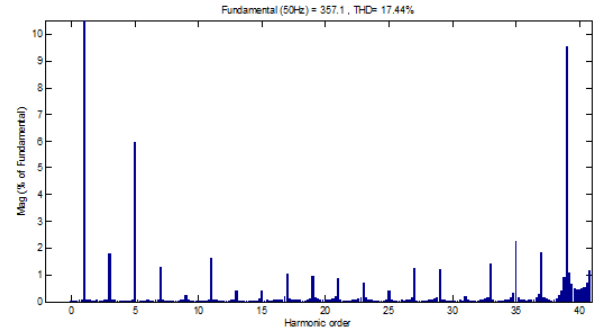


Fig.9.FFT Plot for Output Voltage of PODPWM Strategy

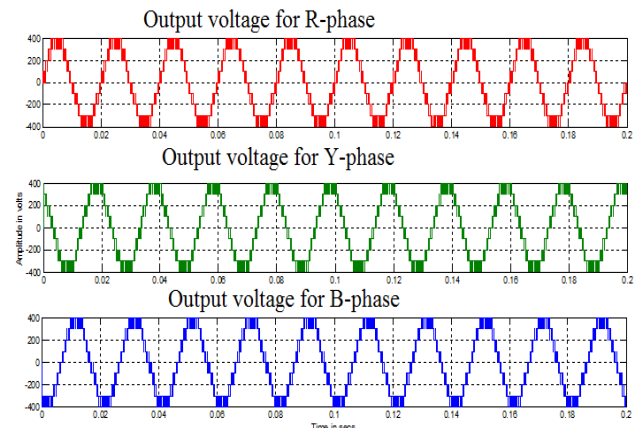


Fig.10.Output Voltage generated by APODPWM Strategy with trapezoidal reference

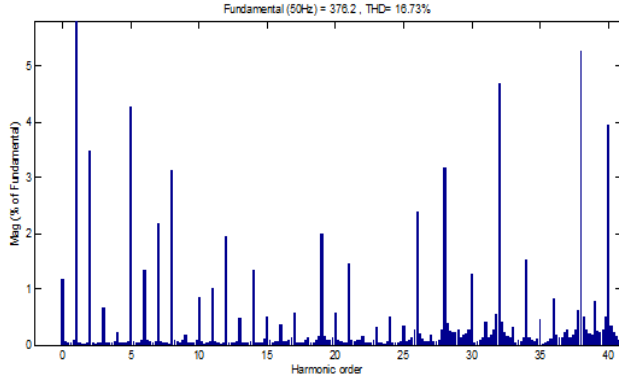


Fig.11.FFT Plot for Output Voltage of APODPWM Strategy

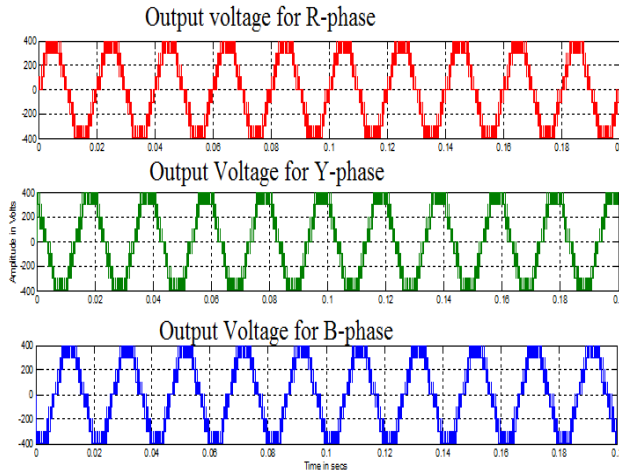


Fig.12.Output Voltage generated by COPWM Strategy with trapezoidal reference

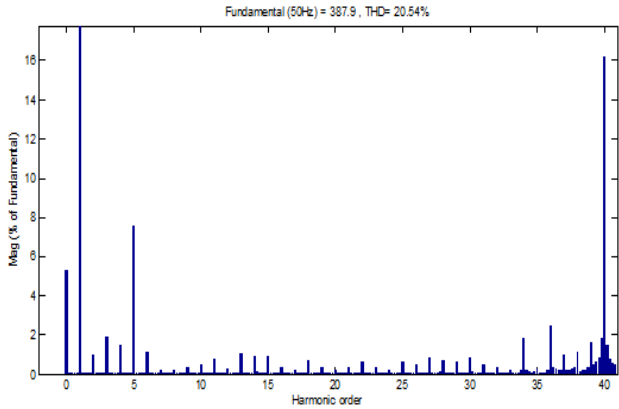


Fig.13.FFT Plot for Output Voltage of COPWM Strategy

Table II. % THD for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	11.71	12.20	12.15	17.03
0.95	14.64	16.32	15.37	19.23
0.9	15.92	17.44	16.73	20.54
0.85	16.36	17.20	17.49	22.70
0.8	16.36	16.13	17.38	23.06

Table III. % Distortion Factor for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	0.4655	0.3662	0.4118	0.8441
0.95	0.2054	0.2436	0.8537	0.4987
0.9	0.2208	0.3108	0.8908	0.4544
0.85	0.1851	0.3607	0.8779	0.5344
0.8	0.2440	0.3892	0.8031	0.6605

Table IV. % V_{RMS} (Fundamental) for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	296.9	290.3	296.9	299.7
0.95	279.5	267.4	279.6	285.3
0.9	265.9	252.5	266	274.3
0.85	253.8	239.3	253.8	263.8
0.8	241.7	229.2	241.8	252.8

Table V. % Harmonic contents of output voltage of chosen inverter with $m_a=0.9$

H order	PD	POD	APOD	CO
2	0.41	0.04	3.47	0.98
3	0.67	1.78	0.66	1.91
4	0.55	0.01	0.22	1.47
5	4.28	5.94	4.27	7.57
6	0.14	0.03	1.34	1.1
7	2.18	1.28	2.16	0.22
8	0.25	0.22	3.12	0.21
9	0.18	0.2	0.16	0.37
10	0.17	0.01	0.85	0.47
11	1.02	1.6	1.01	0.72
12	0.12	0.01	1.93	0.26
13	0.46	0.39	0.48	1.01
14	0.36	0.02	1.34	0.89
15	0.53	0.41	0.51	0.89
16	0.34	0.04	0.37	0.37
17	0.54	1.02	0.56	0.17
18	1.34	0.04	0.14	0.66
19	1.98	0.95	1.98	0.34
20	0.7	0.07	0.56	0.16

It is observed from Table I that the harmonic content is found to be minimum in PDPWM strategy and maximum in COPWM strategy for chosen modulation indices. Table III shows that the variation in harmonic content of the output voltage after second order attenuation indicated by %DF is relatively less in PDPWM strategy and more in COPWM strategy. From Table IV, it is found that the COPWM strategy provide relatively higher DC bus utilization and PODPWM strategy provide relatively lower DC bus utilization. It is inferred from Table V that harmonic spectra is minimum for PODPWM

strategy of chosen nine level three phase TSMLI.

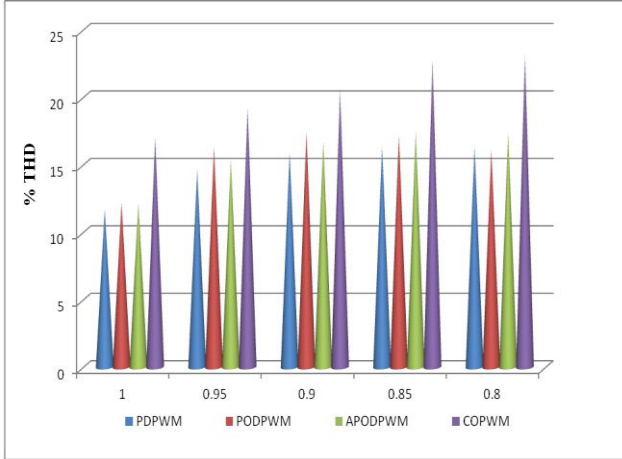


Fig.14. % THD V_s m_a (Simulation)

Of the four strategies developed, PDPWM strategy provides output with relatively minimum distortion (Table II), PDPWM strategy has low %DF (Table III), COPWM strategy provides relatively higher RMS output voltage (Table IV) and PODPWM strategy provides minimum harmonic spectra (Table V). For $m_a = 0.9$, it is observed from Figs. (7, 9, 11 and 13), the harmonic energy above 3% is present in (i) 5th and 40th orders in PDPWM, PODPWM, APODPWM and COPWM strategies. (ii) 2nd, 8th, 28th, 32nd and 38th orders present in APODPWM strategy, but 1st order present in all the strategies except PDPWM strategy. (iii) Dominant lower side band harmonic (40th order) is present in all the strategies.

5. Experimental Result

This paper also extended the experimental results of hardware work using FPGA system for chosen three phase TSMLI. The different multicarrier PWM strategies with trapezoidal reference having rectified sine carrier for TSMLI are initially developed using SIMULINK, but for further real time implementation it is carried out using SPARTAN-3 FPGA system. The nine level output voltage of the chosen TSMLI and their %THD, VRMS (fundamental) and %DF obtained for the SPARTAN-3 FPGA system based PWM strategies are analyzed and presented.

a) FPGA based implementation of PWM strategies of TSMLI

This section presents the results of experimental work performed using SPARTAN-3 FPGA system for chosen TSMLI. FPGAs usually include on-chip PWM controllers making implementation easy. The SPARTAN-3 family of FPGA is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The SPARTAN-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy

development cycles and the inherent inflexibility of conventional ASICs. SPARTAN-3 FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other non-volatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master-Parallel, Slave-Parallel, Master-Serial, Slave-Serial and Boundary Scan (JTAG). The required of gate signal generation blocks/models for the chosen nine level inverter using MCPWM strategy are developed using System Generator (Version 8.2) blocks of Xilinx software (Version 2.0). The system generator consists of logic blocks for carrier generator, reference signal generator (the reference of voltage is a sampled trapezoidal wave), frequency divider etc. and hence the PWM gating signal can be generated from the FPGA directly. Hence the real time implementation of PWM strategies for chosen inverter using FPGA only is carried out in this work. Multi-carrier PWM strategies for the chosen inverter with trapezoidal reference are developed using system generator software in Xilinx platform.

The gate signal generator model developed using system generator is compiled and converted into bits and is downloaded into FPGA for execution in real time. The nine level output voltages of the chosen TSMLI are obtained for the FPGA system based PWM strategies and the corresponding %THD, VRMS (fundamental) and %DF are presented and analyzed. The results of the experimental study are shown in the form of the oscillograms of PWM outputs and corresponding harmonic spectrum of chosen TSMLI. Experiments are performed with appropriate mf (same as in simulation studies) and for different values of m_a . The corresponding %THD and VRMS (fundamental) of output voltages and their %DF values are calculated from the FFT spectrum obtained, tabulated and analyzed. The experimental output voltages and currents as well as the corresponding voltage harmonic spectra are shown for only one sample value of $m_a = 0.9$ of nine level TSMLI topology. Fig.15 shows the entire hardware setup. Fig.15 shows the entire setup. Fig. 16 displays the connectivity diagram of downloading procedures for SPARTAN 3E. Figs. 17 – 22 display the Snapshot of downloading procedures for SPARTAN 3E. Figs.23 - 31 show the experimental output voltages and currents as well as voltage FFT of chosen TSMLI obtained using SPARTAN-3 FPGA system with PDPWM, PODPWM, APODPWM and

COPWM strategies for trapezoidal reference with rectified sine carriers. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 40V. Table VI and Fig. 31 show the comparison of %THD of output voltage with different PWM strategies for various values of modulation index obtained through experimental results. VRMS (fundamental) of output voltage for the above strategies are found for different modulation indices and are tabulated in Table VIII. Table VII provides the comparison of %DF of output voltage of different PWM strategies for various values of modulation index. The following parameter values are used for experimentation: $V_{DC} = 5V$, $R(\text{load}) = 100\Omega$, $f_c = 2000$ Hz and $f_m = 50$ Hz.

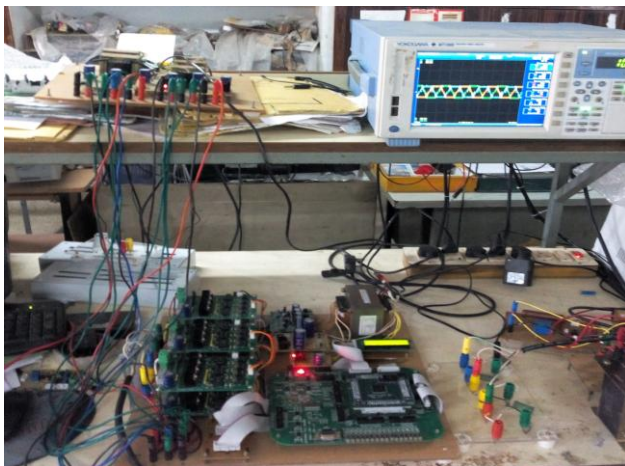


Fig. 15. Hardware setup

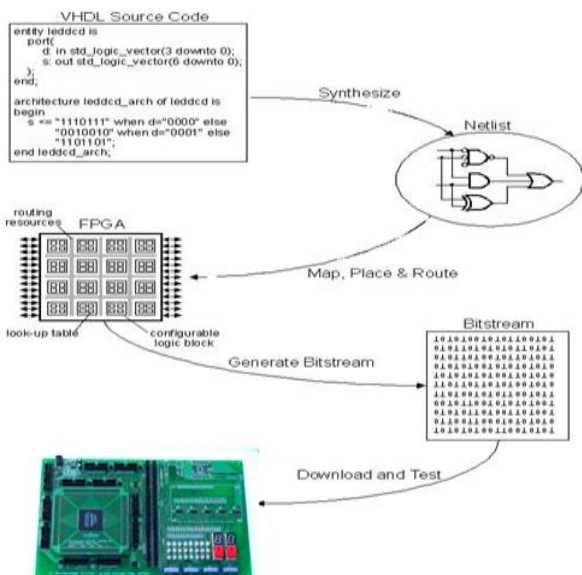


Fig. 16. Connectivity diagram of downloading procedures for SPARTAN 3E

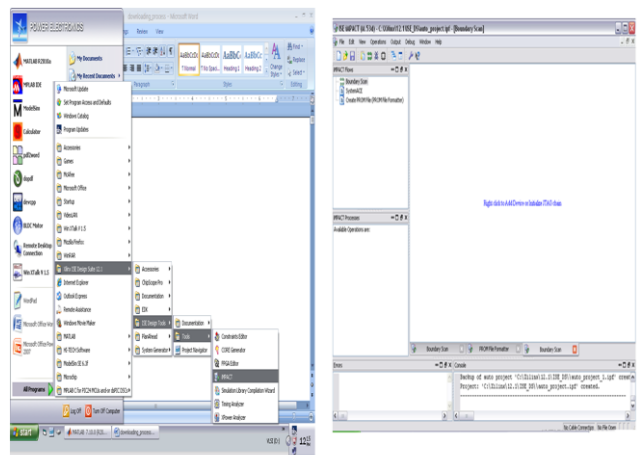


Fig. 17. Snapshot of downloading procedures for SPARTAN 3E of Step 1 and Step 2

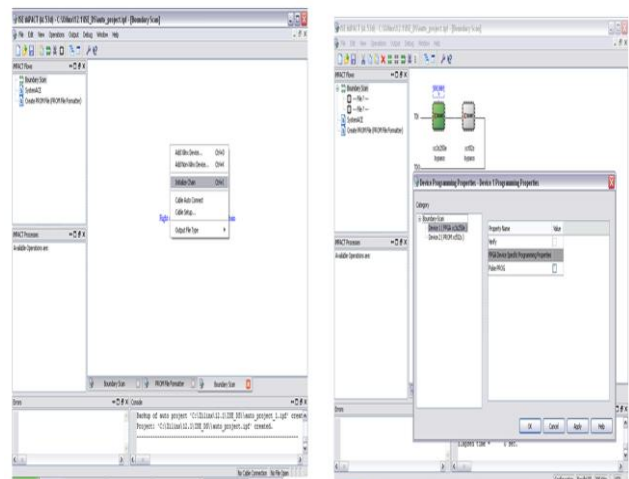


Fig. 18. Snapshot of downloading procedures for SPARTAN 3E of Step 3 and Step 4

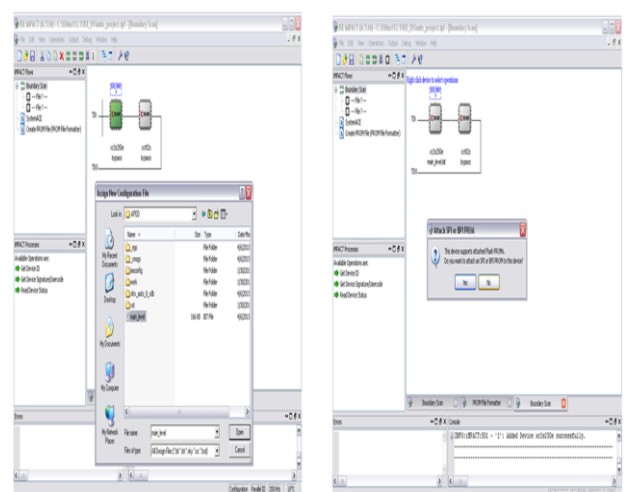


Fig. 19. Snapshot of downloading procedures for SPARTAN 3E of Step 5 and Step 6

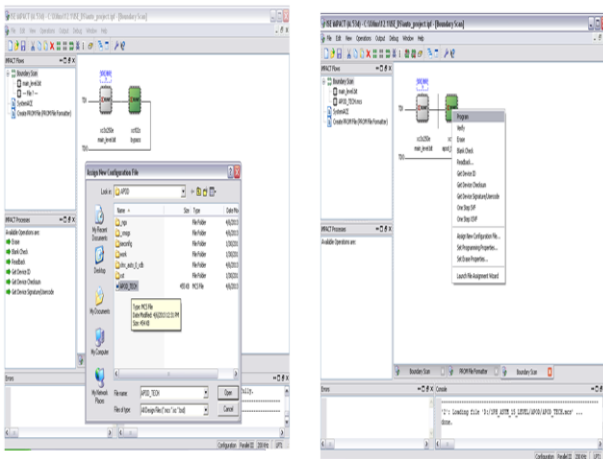


Fig. 20. Snapshot of downloading procedures for SPARTAN 3E of Step 7 and Step 8

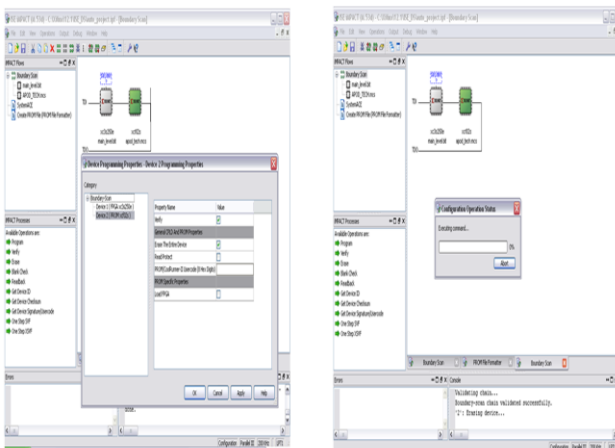


Fig. 21. Snapshot of downloading procedures for SPARTAN 3E of Step 9 and Step 10

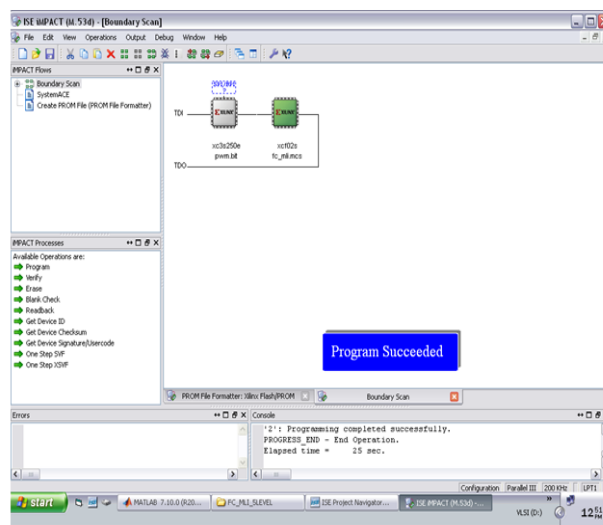


Fig. 22. Snapshot of downloading procedures for SPARTAN 3E of Step 11

b) Downloading Procedures for SPARTAN 3E

The steps involved in downloading the SPARTAN

3E are as follows:

- Step.1: ON Start menu - Open iMPACT
- Step.2: Double click boundary scan - On left side.
- Step.3: Right click boundary scan - On left side
- Step.4: It shows two devices of kit - Select OK
- Step.5: On first device - Load.bit file
- Step.6: Select No.
- Step.7: On second device - Load.mcs file
- Step.8: Right click second device-Select Program
- Step.9: It ask which devices you want to program-Select PROM-OK
- Step.10. Executing Program
- Step.11. It screen program succeeded

c) Synthesis of RTL

Synthesis is an automatic method of converting a higher level abstraction to a lower level abstraction. The synthesis tools convert Register Transfer Level (RTL) description to gate level net lists. These gate level net lists consist of interconnected gate level macro cells. These gate level net lists currently can be optimized for area, speed etc. The analyzed design is synthesized to a library of components, typically gates, latches, or flip-flops. Hierarchical designs are synthesized in bottom up fashion, that is lower level components are synthesized before higher level components. Once the design is synthesized we have a gate level net list. This gate level net list can be simulated. Delay for the individual components are available as part of the description of the component libraries. Timing accurate simulation is not possible at this point because the actual timing characteristic is determined by the physical placement of the design within the FPGA chip. However, the functional simulation that is possible at this point is quite a bit more accurate than simulation based on user specified delays. For the three phase 9-level TSMLI model explained in section, the next step is change source for as synthesis/ implementation. After run the synthesize in process window that is shown in above Figure. Then three phase 9-level TSMLI model is converted to net list file.

To convert the RTL to gates, three steps typically occur,

- i)The RTL description is translated to a un optimized Boolean description usually consisting of primitive gates such as AND and OR gates, flip-flop, and latches. This is a functionally correct but completely un optimized description.
- ii)Boolean optimization algorithms are executed on this boolean equivalent description to produce an optimized boolean equivalent description.
- iii)This optimized boolean equivalent description is mapped to actual logic gate by making use of a technology library of the target process.

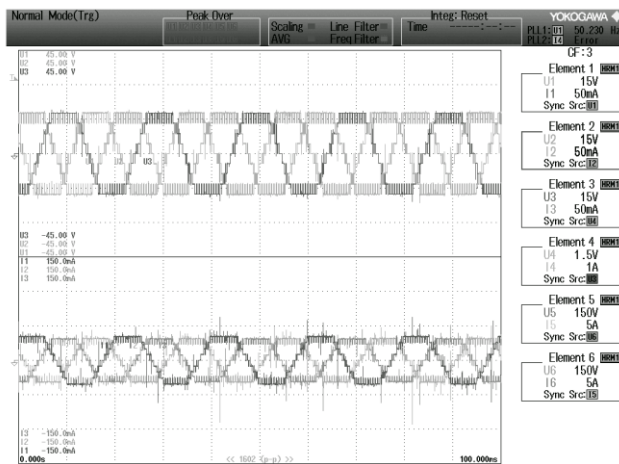


Fig. 23. Experimental output voltage and current with PDPWM strategy for rectified sine carrier

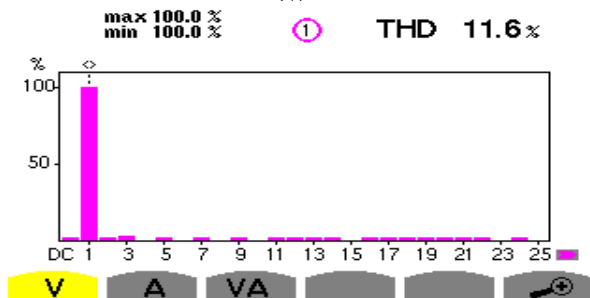


Fig.24. FFT plot for output voltage of PDPWM strategy for rectified sine carrier

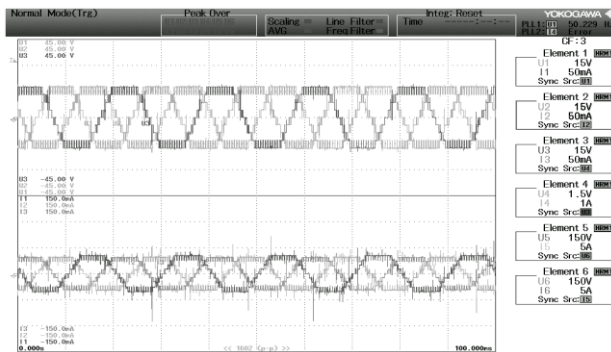


Fig.25. Experimental output voltage and current with PODPWM strategy for rectified sine carrier

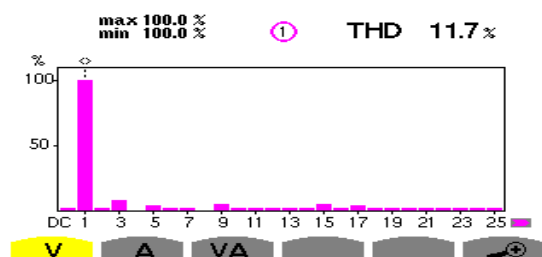


Fig.26. FFT plot for output voltage of PODPWM strategy for rectified sine carrier

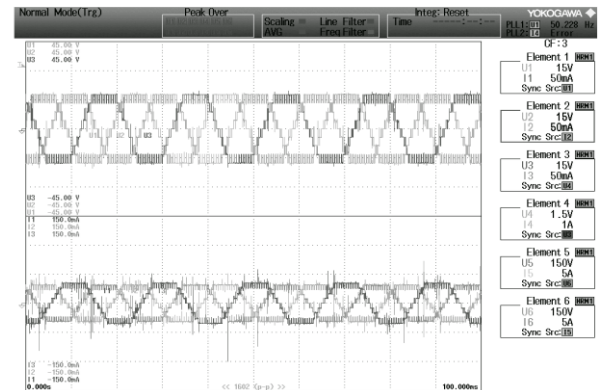


Fig.27. Experimental output voltage and current with APODPWM strategy for rectified sine carrier

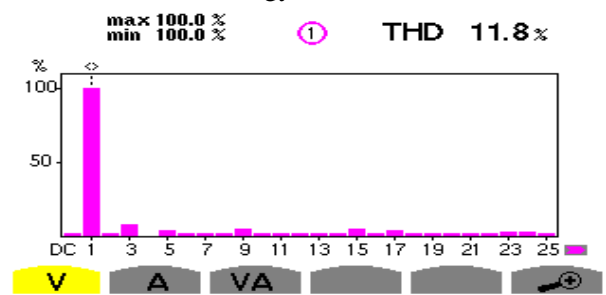


Fig.28. FFT plot for output voltage of APODPWM strategy for rectified sine carrier

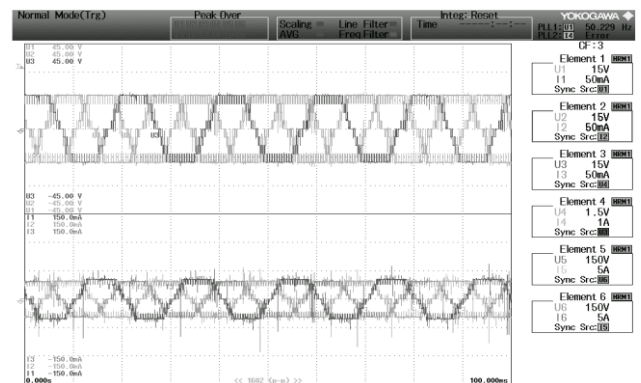


Fig.29. Experimental output voltage and current with COPWM strategy for rectified sine carrier

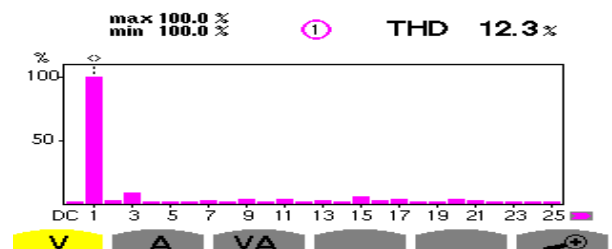


Fig.30. FFT plot for output voltage of COPWM strategy for rectified sine carrier

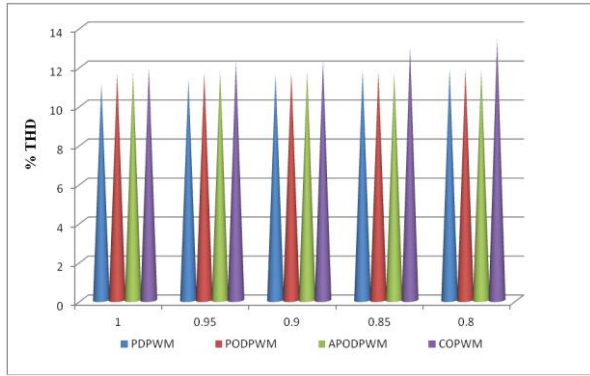


Fig.31. % THD V_s m_a (Experimental)

Table VI. %THD for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	11.15	11.65	11.71	11.95
0.95	11.35	11.68	11.79	12.29
0.9	11.60	11.70	11.80	12.30
0.85	11.79	11.76	11.72	12.98
0.8	11.88	11.85	11.86	13.42

Table VII. % Distortion Factor for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	0.116	0.119	0.121	0.128
0.95	0.118	0.120	0.123	0.129
0.9	0.120	0.122	0.125	0.130
0.85	0.125	0.128	0.128	0.132
0.8	0.126	0.129	0.129	0.134

Table VIII. % V_{RMS} (Fundamental) for Different Modulation Indices

m_a	PD	POD	APOD	CO
1	14.32	14.35	14.30	14.58
0.95	13.63	13.64	13.61	14.21
0.9	13.03	13.02	13.01	13.53
0.85	12.21	12.22	12.20	13.12
0.8	11.42	11.41	11.40	12.46

6. Conclusion

In this paper, various multicarrier PWM strategies for chosen nine level three phase Trinary cascaded DC source multilevel inverter have been developed, simulated and experimental results are presented for different modulation indices ranging from 0.8-1. Various performance factors like %THD (a measure of closeness in shape between a waveform and its fundamental component), DF, V_{RMS} of fundamental and harmonic spectra are evaluated, analyzed and presented from simulation results. It is observed that PDPWM strategy provides lower THD and relatively

lower Distortion Factor (DF) (Table II and III). The maximum DC bus utilization is achieved in COPWM strategy (Table IV). The harmonic content of the output voltage is relatively the least for PODPWM strategy (Harmonic spectra) (Table V). Chosen PWM strategies for three phase nine level TSMLI with rectified sine carrier are simulated using MATLAB - SIMULINK. From experimental results, it is observed from Table VI that the harmonic content of the output voltage is comparatively lower and also inferred from Table VII that the %DF is lowest in PDPWM strategy. From Table VIII, V_{RMS} (fundamental) output voltage of COPWM strategy is the highest, COPWM has higher V_{RMS} for rectified sine carrier. Various multi-carrier bipolar PWM strategies having trapezoidal reference with rectified sine carrier have been implemented using SPARTAN-3 FPGA and tested for different modulation indices ranging from 0.8 - 1 for three phase TSMLI. Various performance factors like %THD, V_{RMS} and %DF indicating the amount of DC bus utilization have been evaluated, analyzed and presented. The result indicate that both simulation and experimental results coincide with each other and the appropriate PWM strategies may be employed depending on the performance measure required in a particular application of Trinary DC inverter based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

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