A New Generalized Algorithm of Space Vector PWM for Multilevel Inverters

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Abstract: *This paper presents a new generalized algorithm of space vector pulse width modulation (SVPWM) for the three phases N level inverters. This algorithm is based on numerical analysis; it offers a great flexibility to optimize switching waveforms and is also adapted for digital implementation. This paper analyzes the voltage space vector distribution of the three phase inverter in (α-β) coordinates, and describes new methods for selecting the switching states and for calculating the duty cycles of adjacent vectors. Simulation and experimental results, in terms of harmonic analysis and THD responses, show the effectiveness of the generalized algorithm proposed.*

Key words: three phase multilevel inverter, space vector PWM, generic algorithm.

1. Introduction

Multilevel converters have been mainly used in high power system applications, such as static reactive power compensation and adjustable speed drives. In these applications, due to the limitations of the currently available power semiconductor technology, a multilevel concept is usually a unique alternative. They have, in general, advantages over conventional two level inverters due to: [1]-[5]:

- Their ability to handle high voltage with voltage limited devices;
- Reduced harmonic distortion in the output voltage;
- Lower electromagnetic interference and good electromagnetic compatibility;
- Minimum voltage stress on the switching devices,
- Lower dv/dt in generated voltage;
- Reduced switching losses;
- Increased efficiency;
- Reduced stress on motor bearings in drive applications.

Voltage-source multilevel-inverter topologies are based on the synthesis of a voltage waveform from several DC voltage levels typically obtained from several capacitors or DC sources [6]–[10]. As the number of levels increases, the synthesized output voltage gets more steps and produces a waveform which approaches the reference more accurately. There are several topologies of multilevel inverters, they are classified into three main categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters.

For the control of these inverters, Many PWM techniques have been proposed over the years; the most popular are those based on sinus triangular comparisons technique, hysteresis technique, Selective Harmonic Elimination Technique (SHEPWM), and Space Vector Pulse Width Modulation (SVPWM) which is the object of this work [11]–[24].

The SVPWM is generally adopted for driving multilevel inverter systems due to:

- Its flexibility to reduce the common mode and to balance the voltage of the DC link capacitors;
- Its flexibility for optimizing switching waveforms;
- It is well suited for digital implementation.

However, regardless of its advantages, the implementation of SVPWM represents a difficulty mainly due to the excessive computational requirements when applied to inverters with a higher number of levels. Consequently, several methods intended to reduce a computational time are proposed, their main contribution is on algorithms to select the three nearest vectors to the reference vector, to calculate their duty cycles and to organize the sequence of these three vectors in order to reduce the number of switching transitions and/or the harmonics content of the generated voltage.

In this paper, we propose a simple systematic method to determine the three nearest vectors to the reference vector based on region (triangle) and sector (sector) indexation. In order to identify easily the switching states associated to the region and the sector selected, space vectors matrix is organized related to the region and sector indices. With this organization, it is possible to seek the sequence of the three vectors which ensures the weakest harmonic content. Moreover, a simple method of duty cycles computation is proposed which exploits directly the projection of the reference vector to the three closest distances.

For this purpose, the paper is organized as follows, in section II, we give the general concept of SVPWM, the section III presents the generalized algorithm proposed, it describe the limiting area indexation and the process for the reference vector location. Also, the space voltage determination and their organization in matrix are given and the research method of the three closest space vectors surrounding reference vector is developed. It is also deduced, in this section, the duty cycle computation associated to these three switching states. In the Section IV, we give the simulation results for 3, 5, 7, 9 and 11 level inverter controlled with the proposed algorithm. Finally, the section V presents an experimental result of implementation of this algorithm in Dspace 1103 for the control of a NPC three level inverter.

2. Principal of SVPWM for multilevel inverters

In multilevel inverters, the number of the switching states N_a is given by:

$$N_a = N_l^{\ 3} \qquad (1)$$

Each switching states, or combination of phase leg switch produce a defined set of three phase voltages. The different voltage space vectors number, N_u, is given by:

$$N_u = 1 + 6 \sum_{i=1}^{N_l - 1} i \qquad (2)$$

The space vector representations of the output voltage for the inverters with N_l=3, 4 and 5 levels in α-β frame are shown in Fig. 2.

(a)Three levels three phases inverter

(b) Four levels three phases inverter
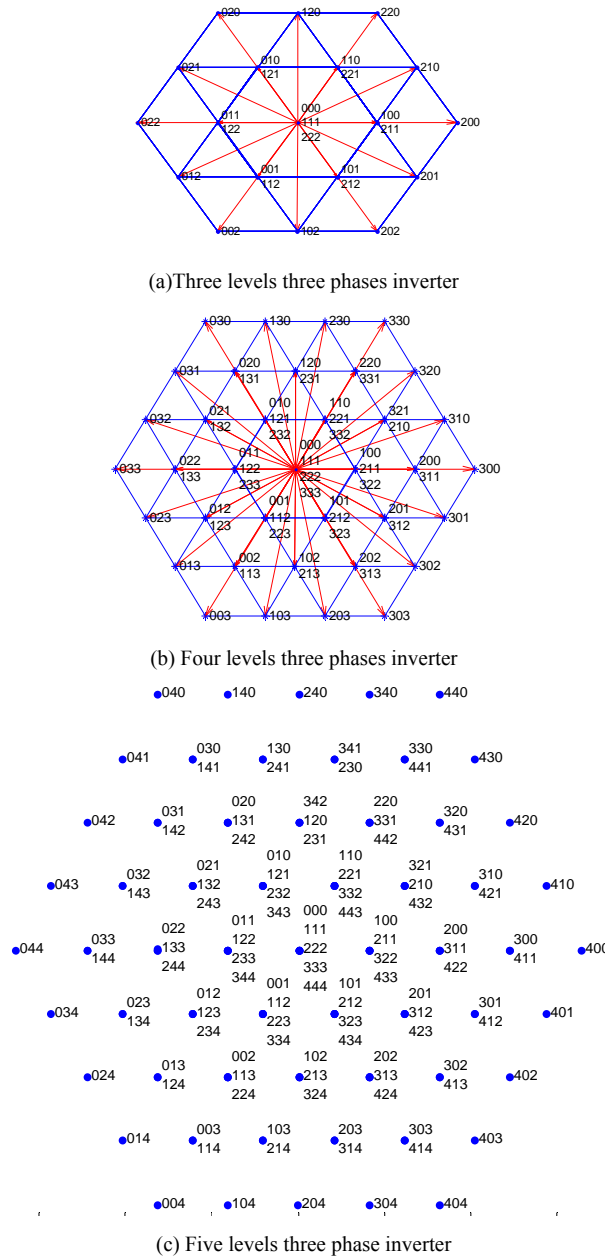

(c) Five levels three phase inverter

Fig.1. Two dimensional representation of voltage space vectors of a three phase 3 and 4 level inverters

The space vector diagram can be divided into sector and each sector can be divided into triangular regions. The division of the voltage space into triangle is illustrated in figure 1.a and figure 1.b for three and four levels inverters respectively. Where, each corner of every triangle represents a possible voltage vector of the three-phase inverter.

Similar to the SVM algorithm for two-level inverters, the reference space vector is used to select the corresponding set of three nearest adjacent voltage space vectors.

The adjacent three vectors selected can synthesize a desired reference voltage vector using averaged approximation. If the reference vector lies in the triangle connecting the tips of vectors $\vec{V_1}$, $\vec{V_2}$ and $\vec{V_3}$ (Fig. 2).
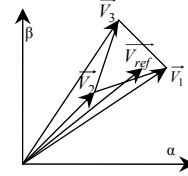

Fig.2. Generation of the reference vector by using three vectors

The average reference vector can be obtained with:

$$\overrightarrow{V_{ref}} = +d_1 \vec{V_1} + d_2 \vec{V_2} + d_3 \vec{V_3} \qquad (3)$$

Where d_1, d_2 and d_3 the duty cycles of the adjacent voltage vectors $\vec{V_1}$, $\vec{V_2}$, and $\vec{V_3}$, respectively, they must satisfy the condition:

$$d_1 + d_2 + d_3 = 1 \qquad (4)$$

3. The generalised SVPWM algorithm proposed

The multilevel SVM algorithm developed in this paper carries out three main tasks: the selection of a set of voltage space surrounding the reference vector, computation of duty cycles corresponding and the generation of an optimum sequence of the voltage states. The diagram of the proposed algorithm is presented in fig.3.
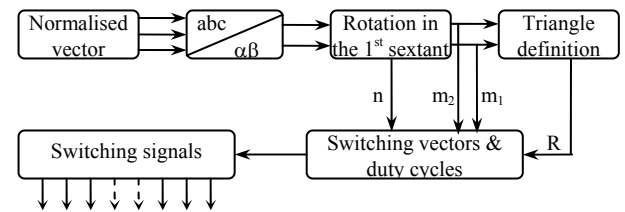

Fig. 3. Diagram of the proposed algorithm

A. Reference vector location

Process of determination of the reference voltage vector location in Cartesian coordinate system is complex. In order to overcome this complexity, hexagonal (g-h space) coordinate system is used. The location is defined in three steps:

Step 1: Sector identification.
Step 2: defining the equivalent projection components of normalized reference vector in the first sector in g-h coordinates system.
Step 3: Region definition (triangle) where the reference vector lies.

B.1. Equivalent components in the 1st sector

The projection of normalized reference vector V_{rn} in the first sector is illustrated in Figure 4, the result of projection is determined as follow:

$$V_g = V_{rn}\left(\cos\left(\theta_{ref}\right) - \frac{\sin(\theta_{ref})}{tg(\pi/3)}\right) \qquad (5)$$

$$V_h = V_{rn}\left(\frac{\sin(\theta_{ref})}{\cos(\pi/6)}\right)$$
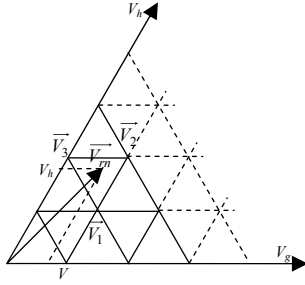

Fig. 4. Reference space vectors projection in the hexagonal coordinates system for sector-I.

The components m_1 and m_2 of the equivalent vector in the first sector can be directly found, by the values V_g, V_h, in the sector where the reference vector lies. These relationships are illustrated in table 1:

TABLE 1: EQUIVALENT COMPONENTS IN THE FIRST SECTOR

gh components	Sector	Equivalent components
$V_g\geq0$ & $V_h\geq0$	1	$m_1=V_g; m_2=V_h;$
$V_g<0$ & $V_h\geq0$ & $(V_g+V_h)\geq0$	2	$m_1=-V_g; m_2=V_g+V_h;$
$V_g<0$ & $V_h\geq0$ & $(V_g+V_h)<0$	3	$m_1=V_h;$ $m_2=-V_g-V_h;$
$V_g<0$ & $V_h<0$	4	$m_1=-V_h; m_2=-V_g;$
$V_g\geq0$ & $V_h<0$ & $(V_g+V_h)<0$	5	$m_1=-V_g-V_h; m_2=V_g;$
$V_g\geq0$ & $V_h<0$ & $(V_g+V_h)\geq0$	6	$m_1=V_g+V_h;$ $m_2=-V_h;$

B.2. Region definition

In this paper, a simple technique is presented to determine the triangle in which the desired vector is located. In first step, a region number synthesis is required.

The total number of region in one sector is the sum of sequence with the first term is 1 and general term defining as:

$$\begin{cases} U_n = U_{n-1} + 2 \\ U_0 = 1 \end{cases} \qquad (6)$$

The total number of region for N_l levels is

$$N_r = \sum_{n=0}^{n=(N_l-1)} U_n \qquad (7)$$

One sector is divided on layer, the number of layer increase with the number of level, one layer represent another extern hexagon when the level increase. Consequently, the number of region in one layer is defined by the relation:

$$N_{rl} = 2C - 3 \qquad (8)$$

C is the number of layer and it corresponds on number of level if the last layer is considered. Their domain of variation is from 2 to N_l.

The indices of regions in one sector are defined as:
- the indices is identical to region indices in last layer $C=N_l$,
- the region indices is defined by addition with the indices of region in the highest order hexagon, it can be formulated by:

$$R = R + \sum_{n=C+1}^{N_l} (2n-3) \qquad (9)$$

For identification of the region where the reference vector lies, the indexation of region in one layer is divided into odd and even number. Figure 5 show how the regions is numerated.
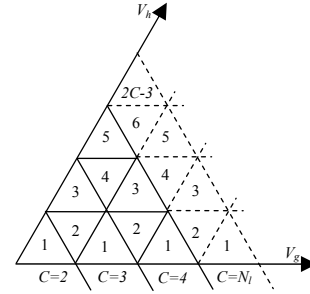

Fig. 5. Region indexes in sector I.

The criteria for defining the region indexes are summarized in the table 2:

TABLE 2: REGION DEFINITION

Region in layer	Conditions for : $2\leq C\leq N_l$ & $1\leq k\leq N_l-1$	Region
odd	$(C-(k+1))<m_1\leq(C-k)$ $(k-1)<m_2\leq k$ $m_1+m_2\leq(C-1)$	$2k+1$
even	$(C-(k+2))<m_1\leq(C-(k+1))$ $(k-1)<m_2\leq k$ $m_1+m_2>(C-2)$	$2k$

C. Space vectors matrix organization

The sets of space vector with a zero argument value are ordered in increasing magnitude; the number of these sets is equal to level number of the inverter. The rest of sets are ordered in decreasing magnitude and increasing argument, these sets are numbered from (N+1) to (2N-1) the number of total sets of space vectors.

D. Nearest vectors definition and Switching Sequence Arrangement

D.1.Vector sequence selection

The order of applied nearest vectors is function of the number of region in sector (even or odd). The order is showed by the row in the figure 6.
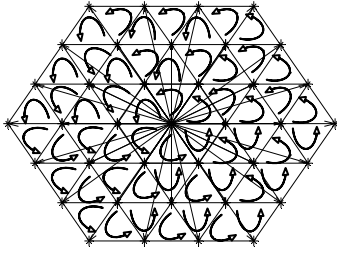
Fig. 6. Three vectors sequence arrangement

D.2. Algorithm for optimal sequence switching

It was remarked, the voltage space are represented by multiple redundant voltage states. There are several options to determine the switching sequence. Switching sequence can be arranged according to certain optimal objective, for example, minimum switching loss or minimum total harmonic distortion (THD). In this paper, in order to achieve low number of switches for a given space voltage V_{ref}, all relevant switching states are arranged to form the switching sequences.

This algorithm is based on choice in redundant vectors of the next adjacent vector in sequence the suitable for minimum number of switch (one transition switch).

After the location of the reference vector by a region index, as shown in Figure 3. The three nearest inverter space voltage for all regions can be determined by applying the following algorithm:

Step1: Define the nearest vectors for region 1 in the outer hexagon with respect of sequence arrangement as:

$V_1(1,:,C)=S(1,:,C);$
$V_2(1,:,C)=S(1,:,N_l+k+1);$
$V_3(1,:,C)=S(1,:,C-1);$

With: $k=0$, $C=N_l$, S is the states matrix.

Step 2: decrease C for N_l to 3 and increase the sector number for 1 to 6.
If C is even increase k with : $k=k+(C-2)/2$.
If C is odd increase k with : $k=k+(C-1)/2$.

Step 3: define the nearest vectors for all regions with respect of the criteria shown in the tables (3, 4, 5 and 6)

TABLE 3: FIRST VECTOR $V_1(R,:,C)$ DEFINITION

C	*		*
R_{ls}	Odd		even
R_l	1	Other	*
$V_1(R,:,C)$	S(i,:,C)	V_1(R-1,:,C)	V_2(R-1,:,C)

TABLE 4.A: SECOND VECTOR $V_2(R,:,C)$ DEFINITION

C	*	Odd			even		
R_{ls}	odd	Odd			odd		
R_l	NRC	<(NRC-1)/2	(NRC-1)/2	other	NRC	≤(NRC-2)/2	other
$V_2(R,:,C)$	S(i,:,C)	S(i,:,N_l+k+i_1)	S(i,:,N_l+k+i_1);	S(i,:,N_l+k+j_1)	S(i,:,C)	S(i,:,N_l+k+i_6)	S(i,:,N_l+k+j_6)

TABLE 4.B: SECOND VECTOR $V_2(R,:,C)$ DEFINITION

C	*	odd		even		
R_{ls}	even	even		even		
R_l	NRC-1	<=(NRC-1)/2	other	<(NRC-1)/2	(NRC-1)/2	other
$V_2(R,:,C)$	S(i,:,C-1)	S(i,:,N_l+k+(C-1)/2+i_4)	S(i,:,N_l+k+(C-1)/2+j_4)	S(i,:,N_l+k+(C-2)/2+i_5)	S(i,:,N_l+k+(C-2)/2+i_5)	S(i,:,Nl+k+(C-2)/2+j_5)

TABLE 5: THIRD VECTOR $V_3(R,:,C)$ DEFINITION

C	*	*	*	odd		even		
R_{ls}	Odd		even	even		even		
R_l	1	other	2	≤(NRC+1)/2	other	<(NRC+3)/2	(NRC+3)/2	other
$V_3(R,:,C)$	S(i,:,C-1);	V_2(R-1,:,C);	S(i,:,C-1)	S(i,:,N_l+k+i_2)	S(i,:,N_l+k+j_2)	S(i,:,N_l+k+i_3)	S(i,:,N_l+k+i_3)	S(i,:,N_l+k+j_3)

With:

TABLE 6: INITIAL PARAMETERS DEFINITION

increased variables	Decreased variables
i_1=1For the sector n=1;	j_1=(C-1)/2;
i_1=0 For the others sectors;	j_2=(C-1)/2+(C-3)/2+1;
i_2=(C-1)/2;	j_3=(C-2)/2;
i_3=0;	j_4=(C-3)/2+1;
i_4=0;	j_5=(C-2)/2;
i_5=0;	j_6=(C-2)/2+1;
i_6=0;	

R is the region number in the total space.
R_l is the region number in one layer for total space.
R_{ls} is the region number in one layer and one sector.
NRC is the number of regions in the layer C for one sector.

E. sequence organization

A Sequence organisation is similar to the case of a two-level inverter; the order of the elements in the sequence is reversed in the next half of the modulation period.

4. Simulation results

The proposed algorithm is implemented using Matlab program. An examples to indicate the simplicity of the algorithm for any number of levels is shown in figure 11, it represents the line-to-line voltage and its spectrum for a 3, 5, 7, 9, and 11 levels inverters with a modulation index of 0.95. Simulate higher levels of SVM Will be with the same simplicity.

A deeper analysis of the resulting PWM voltage harmonics spectrum shows that the low order harmonics remain relatively weak and the increasing of the level number has an effect on the reduction of the harmonics content.
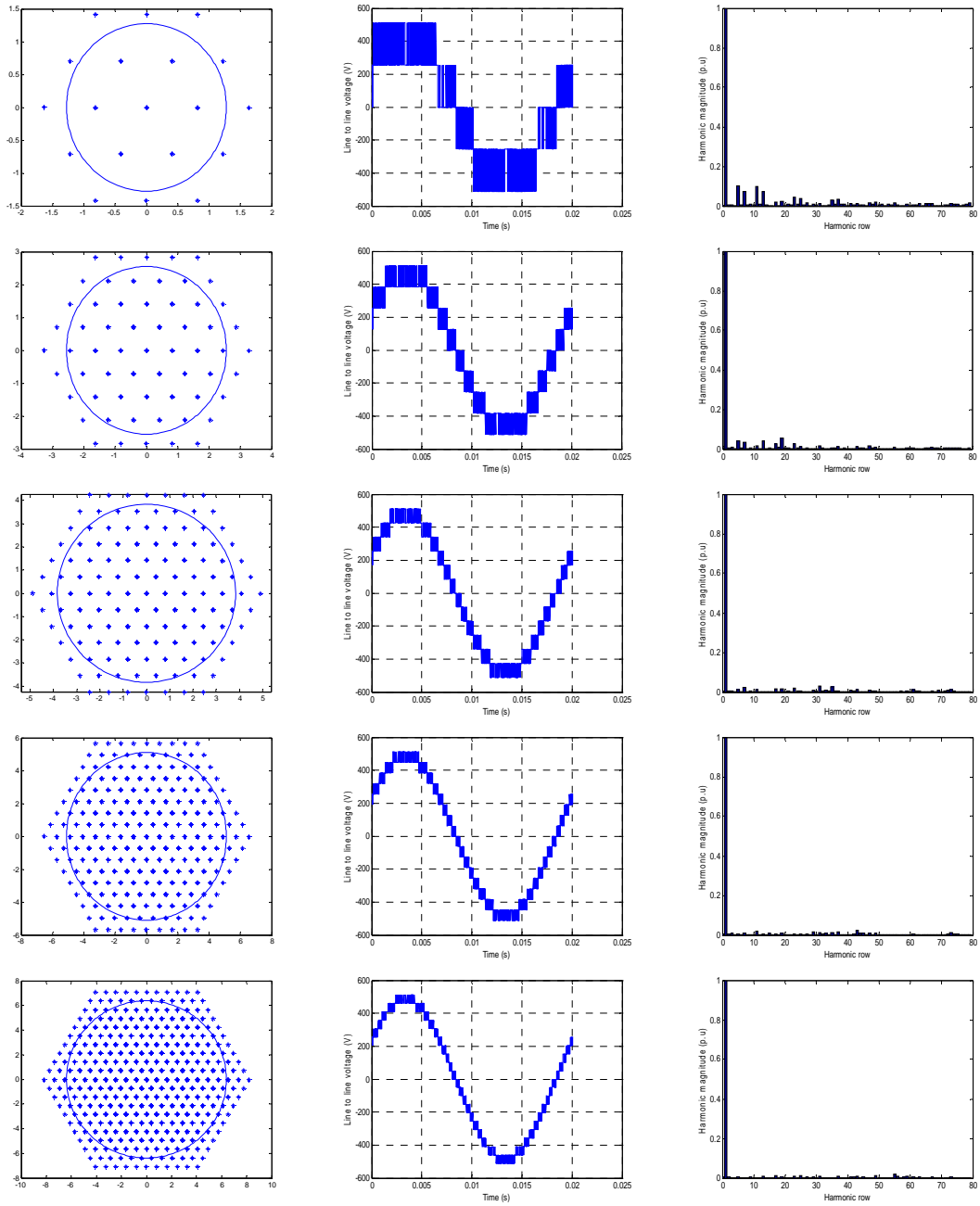
Figure. 7. Line to line voltage and their spectrum with modulation index r=0.95, for different levels N_l=3, 5, 7 , 9 and 11.

The performances of the output voltage are represented by the variation of the THD and the Weighted THD according to the modulation index r for several levels (Figure 8).
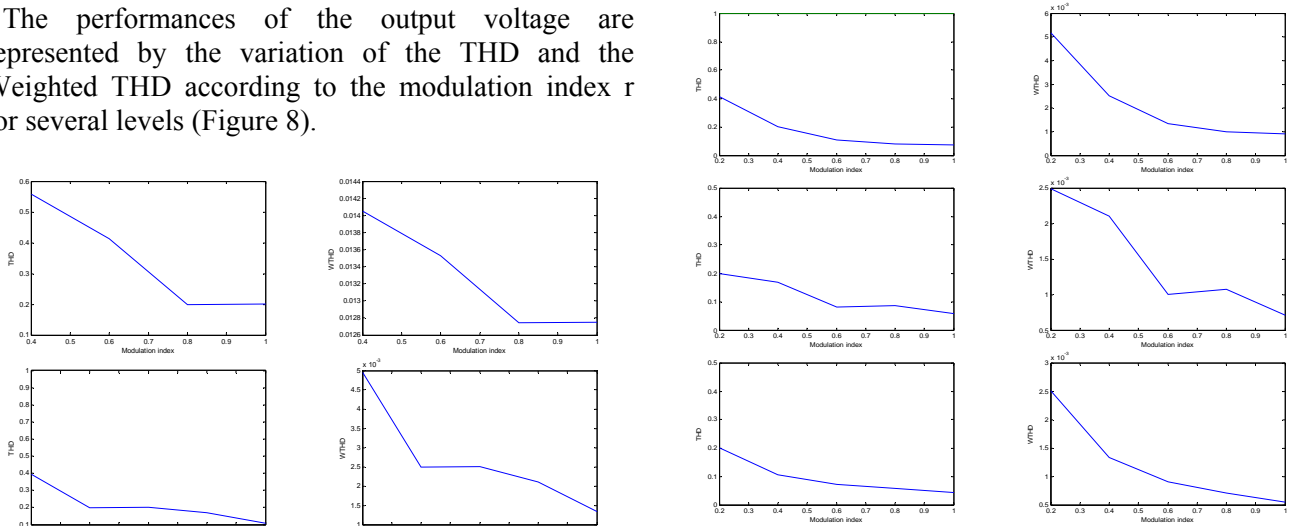

Figure 8. Values of THD and WTHD according to the index modulation for different levels N_l=3, 5, 7 , 9 and 11.

A comparison of these performances according to N_l shows that there is a significant reduction in the THD and WTHD for N_l passing from 3 to 5 and 7 to 9. For N_l=5, 7 and N_l=9, 11, the inverter performances are almost identical.

5. Experimental results

This algorithm is implemented in DSpace 1103 and tested for a NPC three level inverter. The test bench used to valdate the proposed strategie is illustrated in the figure 9.

Fig.9. The experimental setup.

The simple voltage of three phase resistive load is shown in figure 10. It shows the effectiveness of the proposed algorithm.
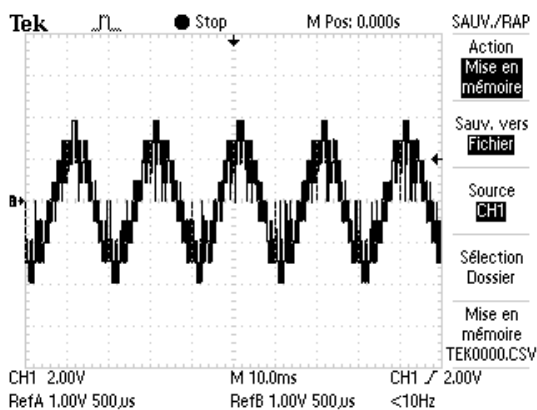

Fig.10. simple voltage of resistive load fed with NPC three level inverter controlled with SVPWM strategy proposed.

6. Conclusion

This paper has presented a new generalized algorithm for generating a SVM for N level inverters. This algorithm allows a reduction in switching numbers with fewer harmonics by an optimal utilisation of redundant vectors and classification of adjacent vectors. It has the flexibility of being adapted for a required application in order to achieve less delayed response time.

To confirm the validity of the proposed algorithm, various simulation tests were performed for 3, 5, 7, 9 and 11 levels inverters and experimental test for a NPC three level inverter. The results confirm that the proposed algorithm is effective.

References

[1] Grain P. Adam, Stephen J. Finney, Ahmed M. Massoud, and Barry W. Williams , "Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode", IEEE Trans. on Ind. Electron., vol. 55, no. 8, august 2008.

[2] Óscar López, et al, "Comparison of the FPGA Implementation of Two Multilevel Space Vector PWM Algorithms", IEEE Trans. on Ind. Electron., vol. 55, no. 4, april 2008.

[3] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. Kothari, "A review of three-phase improved power quality AC-DC converters" , IEEE Trans. Ind. Electron., vol. 51, no. 3, pp. 641–660, Jun. 2004.

[4] A. Yazdani and R. Iravani, "A neutral-point clamped converter system for direct-drive variable-speed wind power unit," *IEEE Trans. Energy Convers.*, vol. 21, no. 2, pp. 596–607, Jun. 2006.

[5] E. Benyoucef, A. Meroufel S. Barkat, « Three-Level Direct Torque Control Based on Space Vector Modulation with Balancing Strategy of Double Star Synchronous Machine », Journal of Electrical Engineering , Vol. 14, ed. 3, pp. 146 - 154, 2014.

[6] Sérgio Daher, and al, "Multilevel Inverter Topologies for Stand-Alone PV Systems", IEEE Trans. on Ind. Electron., vol. 55, no. 7, July 2008

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[8] J. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[9] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[9] H. Chekireb and E. M. Berkouk, "Generalised algorithm of novel space vector modulation for N-level three-phase voltage source inverter", Euro. Trans. Electr. Power, 2008.

[10] C.R.Balamurugan, S.Sivasankari, S.P.Natarajan , « Multilevel inverter topologies using flip flops » , Journal of Electrical Engineering , Vol. 14, ed. 4, pp. 280 - 285, 2014.

[11] S. Tuncer, and Y. Tatar, "A new approach for selecting the switching states of SVPWM algorithm in multilevel inverter", Euro. Trans. Electr. Power, 2007

[12] Óscar López, et al, "Multilevel Multiphase Space Vector PWM Algorithm", IEEE Trans. on Ind. Electron., vol. 55, no. 5, May 2008.

[13] A.K. Gupta, A. M. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two level space vector PWM," IEEE Trans. Ind. Electron., vol. 53, pp. 1631–1639, 2006.

[14] J. Pou, P. Rodriguez, D. Boroyevich, R. Pindado, L. Candella, "Efficient space vector modulation algorithm for multilevel converter with low switching frequencies in the devices", Proc of conf IEEE, Power Electron., Spec, pp. 2521–2526, 2005.

[15] R. L. Josephine, Padmabeaula, A. Dhayal Raj, R. L. Helen Catherine, « PWM control for hybrid clamped multilevel inverters » , Journal of Electrical Engineering , Vol. 13, ed. 4, pp. 99 - 107, 2013.

[16] C. Govindaraju K. Baskaran, « Multiphase multilevel hybrid carrier based space vector pwm algorithm », , Journal of Electrical Engineering , Vol. 11, ed. 4, pp. 1 - 10, 2011.

[17] Yi Deng, Koon Hoo Teo, Chunjie Duan, T.G. Habetler, R.G. Harley, "A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters", ", IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5204 - 5217, 2014.

[18] T. Duran, J. Pereda, "Novel continous space vector modulation in cascaded multilevel converters", IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, pp. 1629 - 1635, 2014.

[19] I. Ahmed, V.B. Borghate, "Simplified space vector modulation technique for seven-level cascaded H-bridge inverter", IET Power Electronics, vol. 7, no. 3, pp. 604 - 613, 2014.

[20] J. Amini, "An Effortless Space-Vector-Based Modulation for N -level Flying Capacitor Multilevel Inverter With Capacitor Voltage Balancing Capability", IEEE Transactions on Power Electronics, vol. 29, no. 11, pp. 6188 - 6195, 2014.

[21] Y. Kumsuwan, W. Srirattanawichaikul, "space vector modulation strategy for three-level operation based on dual two-level voltage source inverters", International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), pp. 3417 – 3424, 2014.

[22] C. Sarath, A. Antony, « Implementation of SVM to improve the performance of a nine level inverter with reduced number of switches", IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES), pp. 1-5, 2015.

[23] K. Tian, J. Wang, B. Wu, D. Xu, Z. Cheng, N.R. Zargari, "A New Space Vector Modulation Technique for the Reduction of Common-Mode Voltages in both Magnitude and Third-Order Component", IEEE Transactions on Power Electronics, 2015.

[24] V. Vekhande, N. Kothari, B.G. Fernandes, « Switching State Vector Selection Strategies for Paralleled Multilevel Current-Fed Inverter Under Unequal DC-Link Currents Condition", IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 1998 - 2009, 2015.