Evaluation of FPGA based speed control of Induction Motor

B.Hariram[1] Dr.N.S.Marimuthu[2]

Abstract – *This paper proposes a fully digitized hardware design scheme of a Space Vector Pulse Width Modulation (SVPWM) based V/f control, which is verified and implemented on a single chip Field Programmable Gate Array (FPGA), for the speed control of three phase induction motor. This is also implemented in Digital Signal Processor (DSP) as FPGA and DSP are the good compromise between the advantage of the flexibility of a programming solution and the efficiency of a specific architecture with a high integration density. These characteristics are quite appropriate for controller design. The comparison of the experimental results especially, Execution time and maximum circuit delay from the DSP and FPGA based implementation respectively, provides guideline on the superiority of FPGA based solution of Industrial Drives in general.*

Keywords*: FPGA, SVPWM, DSP, V/f control*

I. Introduction

Because of advances in solid state power devices and microprocessors, variable speed AC Induction motors powered by switching power converters are becoming more and more popular. Switching power converters offer an easy way to regulate both the frequency and magnitude of the voltage and current applied to a motor. As a result much higher efficiency and performance can be achieved by these motor drives with less generated noises. The most common
principle of this kind is the constant *V/f* principle which requires that the magnitude and frequency of the voltage applied to the stator of a motor maintain a constant ratio[1]. Up to now, its theories and algorithms have been well developed and applied more and more widely with the progress of Power Electronics.

Compared with Sinusoidal PWM (SPWM), which is another useful modulation strategy, the linear range of the SVPWM is 15% higher than the SPWM; furthermore, the SVPWM can continuously change from linear to over modulation and six-step mode with a superior utility factor of the DC bus voltage [2]-[3]. Speed performance of new components and flexibility inherent of all programmable solutions, give today many opportunities in the field of digital implementation for control systems. This is especially true with software solutions as microprocessor or Digital Signal Processor (DSP) [4]. However, specific hardware technology such as Field Programmable Gate Array (FPGA) can also be considered as an appropriate solution in order to boost the performance of controllers. Last twenty five years were outstanding by the revolution of technological possibilities in the field of digital electronics and this is much within the context of programmable solutions (Microcontroller, DSP, etc.,) than of digital hardware solutions (CPLD/FPGA/ASIC). Indeed, these generic components combine low cost development, thanks to their re-programmability, use of convenient software tools and more and more significant integration density [5]-[7]. FPGA technology is now considered by an increasing number of designers in various fields of application such as telecommunication [8], video [9], signal processing [10], embedded control systems [11], and electrical control systems[12]. This is because an FPGA-based implementation of controllers can efficiently answer current and future challenges of this field.

This paper is organized as follows: Section II discusses the theory of Space Vector Modulation and *V/f* control of Induction Motor. Section III and IV describes the SVPWM based *V/f* controller implementation in FPGA and DSP respectively. In section V the experimental results are discussed and section VI concludes with future proposals.

II. SVPWM AND Constant V/ f Control

II.1. Space Vector Pulse Width Modulation

In the mid 1980's Space Vector Pulse Width Modulation was proposed, which was claimed to offer significant advantages over natural and regular sampled PWM in terms of performance, ease of implementation and maximum transfer ratio [3], [4]. The principle of SVPWM is based on the fact that there are only eight possible switch combinations for a three phase inverter. The basic inverter switch states are shown in Figure 1. Two of these states (SV0 and SV7) correspond to short circuit while the other six can be considered to form stationary vectors in the d-q plane as shown in Figure 2. The magnitude of each of the six active vectors corresponding to the maximum possible phase voltage is

$$V_m = \frac{2}{3} V_{dc} \quad (1)$$

Having identified the stationary vectors, at any point in time, an arbitrary target output voltage vector can then be made up by the summation (“averaging”) of the adjacent space vectors within one switching period. Target vectors in the other five segments of the hexagon are clearly obtained in a similar manner. The geometric summation shown in Figure 2 can then be expressed mathematically as,

$$T_{sv1}V_m + T_{sv2}V_m(\cos\frac{\Pi}{3} + j\sin\frac{\Pi}{3}) = \frac{\Delta T}{2}V_o(\cos\theta_o + j\sin\theta_o) \quad (2)$$

for each switching period ΔT.

Equating real and imaginary components yield the solution,

$$T_{sv1} = \frac{V_o}{V_m}\frac{\sin(\frac{\Pi}{3} - \theta_o)}{\sin\frac{\Pi}{3}}\frac{\Delta T}{2}(\text{activetimeforsv1}) \quad (3)$$

$$T_{sv2} = \frac{V_o}{V_m}\frac{\sin\theta_o}{\sin\frac{\Pi}{3}}\frac{\Delta T}{2}(\text{active time for sv2}) \quad (4)$$

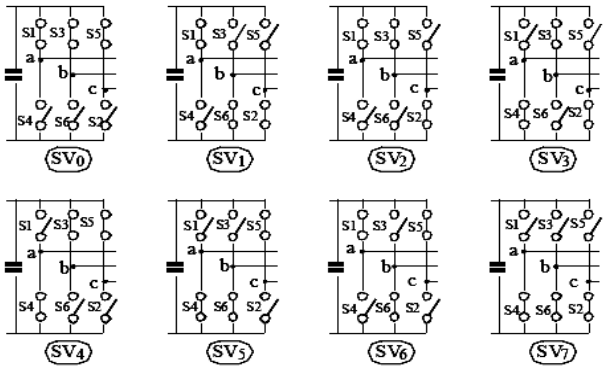

Fig. 1. Eight possible switch combinations for a three phase VSI

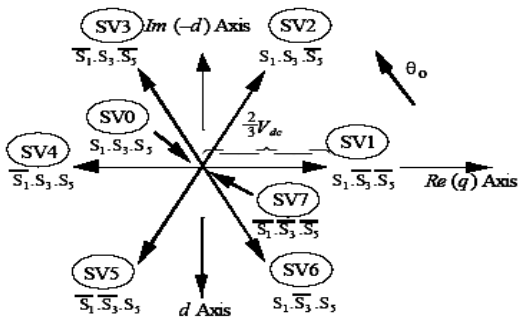

Fig. 2. Space Vector representation

Since $0 \le T_{sv1}, T_{sv2} \le \Delta T/2$, the maximum possible magnitude for V_o is V_m, which can occur at $\theta = 0$ or $\pi/3$. From simple geometry, the limiting case for the constraint $T_{sv1} + T_{sv2} \le \Delta T/2$ occurs at $\theta 0 = \pi/6$ which means,

$$\frac{T_{sv1} + T_{sv2}}{\frac{\Delta T}{2}} = \frac{V_o}{V_m}\frac{2\sin\frac{\pi}{6}}{\sin\frac{\pi}{3}} \le 1 \quad (5)$$

and this relationship constrains the maximum possible magnitude of V_o to

$$V_o = V_m\sin(\frac{\pi}{3}) = \frac{1}{\sqrt{3}}V_{bus} \quad (6)$$

where Vbus is the D.C link voltage. Since Vo is the magnitude of the output phase voltage, the maximum possible line to line output voltage using SVM must equal

$$V_{o(L-L)} = \sqrt{3}V_o = V_{bus} \quad (7)$$

This result represents an increase of 1.1547 compared to regular sampled PWM. It can be noted that SVM is an intrinsically a regular sampled process, since in essence it matches the sum of two space vector volt–second averages over a half carrier period to a sampled target volt–second average [2].

II.2. Constant V/f Induction Motor Drives

The operation of induction machines in constant Volts per Hertz (*V/f*) mode was conceptualized in late fifties and early sixties but were limited in their low speed range. Today constant V/f drives are built using PWM-IGBT-based inverters. And the speed range has widened to include very low speeds although operation very near zero speed (less than 1 Hz) remains as a challenge mainly due to inverter non-linearities at low output voltages. Ideally, by keeping a constant V/f ratio for all frequencies the nominal torque-speed curve of the induction motor can be reproduced at any frequency. Specifically if stator resistance is neglected and keeping a constant slip frequency the steady state behavior of the induction machine can be characterized as impedance proportional to frequency[13].

$$\overline{V} \approx j\omega\overline{\Lambda} \quad (8.a)$$

$$V \approx \omega\Lambda \quad (8.b)$$

where $\overline{V}$ and $\overline{\Lambda}$ are the phasors of stator voltage and stator flux, and V and Λ are their magnitude, respectively[13]. Thus, we get

$$\Lambda \approx \frac{V}{\omega} = \frac{1}{2\pi}\frac{V}{f} \quad (9)$$

Therefore, if the *V/f* ratio is kept constant the stator flux, stator current and hence torque will be constant at any frequency. This feature suggests that to control the torque one needs to simply apply the correct ratio of *V/f* to stator windings.

Since the stator flux is maintained constant, independent of the change in supply frequency, the torque developed depends on the slip speed only. So by regulating the slip speed, the torque and speed of an AC Induction motor can be controlled with the constant *V/f* principle[13].

This simple, straight forward approach, however, does not work well in reality due to several factors, the most important ones being

1) Effect of supply voltage variations
2) Influence of stator resistance
3) Non-ideal torque/speed characteristic (effects of slip)
4) Non-linearities introduced by the PWM inverter.

Low frequency operation is the particularly difficult to achieve since these effects are most important at low voltages. Also, the non-linearities within the inverter, if not adequately compensated, yield highly distorted output voltages that, in turn, produce pulsating torques leading to vibrations and increased acoustic noise. For the above mentioned facts SVPWM is reported to give a better solution [1],[13].

III. Implementation of SVPWM based V/f controller using FPGA

III.1. Design Methodology

For very complex designs, modular conception is generally used to reduce design cycle. This methodology is based on hierarchy and regularity concepts. Hierarchy is used to divide a large or complex design into sub-parts called modules that are more manageable. Regularity is aimed to maximize the reuse of already designed modules.

This implementation contains 8 modules in FPGA namely

1. Speed Variation controlled by push button input
2. Calculation of modulation index and step value (Δalpha)
3. Clock divider
4. Calculation of ON periods *Ta, Tb, To*
5. Calculation of number of 100 Mhz pulses for ON time pulse duration for six SCRs.
6. PWM pattern for IGBT 1 and IGBT 4
7. PWM pattern for IGBT 2 and IGBT 5
8. PWM pattern for IGBT 3 and IGBT 6

Fig. 3 shows a sample flowchart used for the development to calculate the ON periods Ta, Tb, To as per the following relationship

$$\begin{bmatrix} T_a \\ T_b \end{bmatrix} = \frac{\sqrt{3}}{\pi} m T_s \begin{bmatrix} \sin(k\pi/3) & -\cos(k\pi/3) \\ -\sin((k-1)\pi/3) & \cos((k-1)\pi/3) \end{bmatrix} \begin{bmatrix} \cos\alpha \\ \sin\alpha \end{bmatrix} \quad (10)$$

$$T_0 = \frac{T_s}{2} - (T_a + T_b)$$

where $f_S = 1/T_S$ = 10 kHz clock input, α = angle of the reference vector in the corresponding sector and m = modulation index.

Different combinations of *Ta, Tb* and *To/2* decide the no of 100 MHz clock pulses for ON period. ON Period Time calculation for each phase varies for every sector and it is calculated as per the details in Table I.

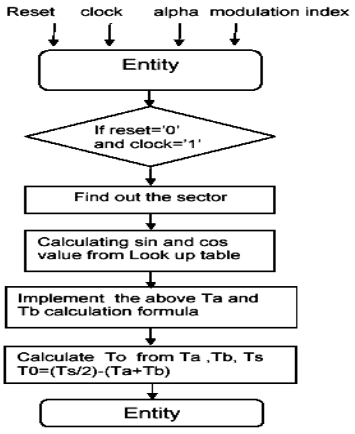

FIG.3. FLOWCHART – CALCULATION OF ON PERIODS

TABLE I
TIME CALCULATION FOR EVERY SECTOR IN EACH PHASE

Ph.	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
Ph A	Ta+Tb+To/2	Tb+To/2	To/2	To/2	Tb+To/2	Ta+Tb+To/2
Ph B	Tb+To/2	Ta+Tb+To/2	Ta+Tb+To/2	Tb+To/2	To/2	To/2
Ph C	To/2	To/2	Tb+To/2	Ta+Tb+To/2	Ta+Tb+To/2	Tb+To/2

In a similar manner every module was coded in VHSIC(Very High Speed Integrated Circuit) Hardware Description Language (VHDL) algorithmically, tested for its functionality and then integrated to give a complete system for open loop *V/f* control of three phase Induction Motor. Figures 4.(a) and 4.(b) depicts the complete schematic which is finally implemented. The modules in both the diagrams are numbered with reference to the eight modules listed above. In Fig. 4.(a) the input ports 'a' and 'b' are assigned to increase the speed and ports 'c' and 'd' are for decreasing the speed using pushbuttons. Every single press of the push button increases/decreases 10 rpm from the current speed and the speed variation achieved is from 300 rpm to 1490 rpm.

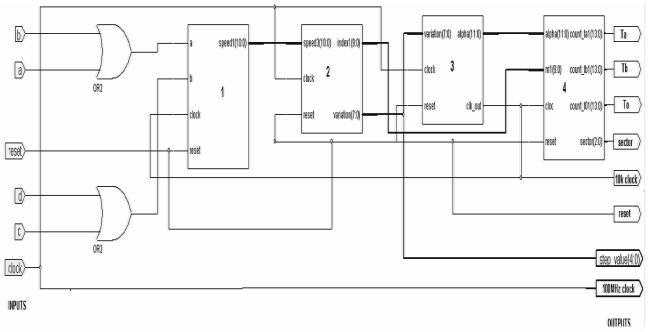

Fig. 4.(a) Implementation Schematic – Part I

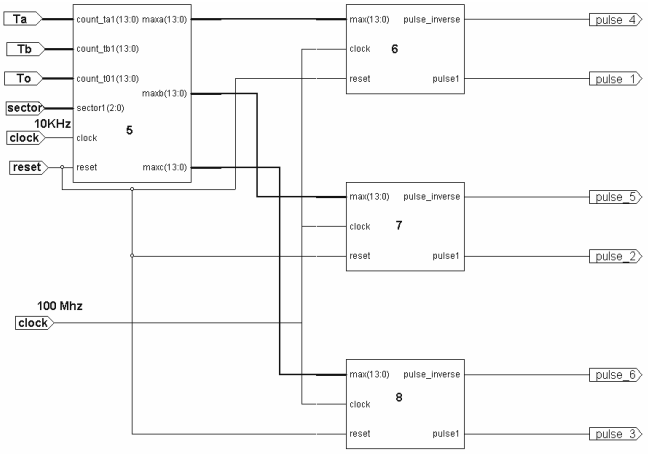

Fig. 4.(b) Implementation Schematic – Part II

Fig. 5 shows the simulation results for the realization of SVPWM based *V/f* controller when the reference vector in sector 1.

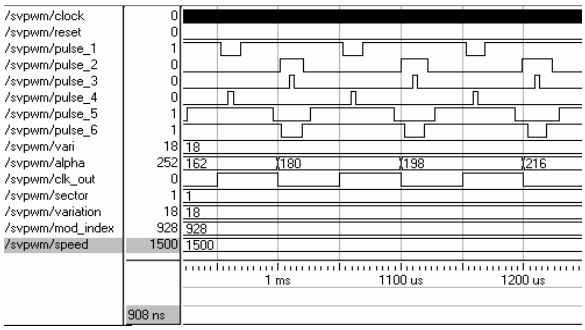

Fig. 5. The simulation output for sector 1 of SVPWM

III.2. Experimental set up

Xilinx project navigator tool is used for downloading the design into the Spartan III XS3S400PQ208-4 FPGA device. SPARTAN device is fixed in a universal development board that contains a 4X4 matrix switches. Two of these switches are set to increase and decrease in speed. Intelligent Power Module (IPM) is used to drive the induction motor. The SVPWM patterns generated using FPGA as per the speed setting from the user drives the IGBTs of IPM module to maintain the necessary *V/f* ratio. The waveforms and other results are given in section V.

IV. Implementation of SVPWM based V/f controller using TMS320F2407 DSP

The TMS320C2xxx series of DSPs has been designed specifically for signal processing and motor control applications. Its hardware is optimized for numeric computation and has the necessary processing capabilities to meet the bandwidth requirements of high performance systems. Through its internally hardwired logic the DSP can execute most functions in a single clock cycle.

Code Composer Studio software which integrates all host and target tools in a unified environment is used for the code development. It also simplifies DSP system configuration and application design to help designers get started faster than ever before.

IV.1. HARDWARE IMPLEMENTATION

SVPWM implementation depends on the application like

1. To control the speed of induction motor using constant *V/f* technique modulation index is used as the reference parameter.
2. Vector controlled induction motor drive uses the stationary reference frame quantities V_α, V_β as reference parameters.

The following are the steps to be followed for the implementation of the first method using TMS320F24XX DSP having SVPWM generation hardware.

1. Initialize various Registers.
2. Create a look up table for sine theta
3. Calculate the time values ta, tb, t0.
4. Find the Duty cycle for each pair of transistor based on sector.
5. Update the PWM.

C code for the algorithm is compiled in Code Composer Studio and the ascii output file is converted to downloadable hex format using debugger and then downloaded to TMS320F2407 DSP kit. The six PWM patterns generated from the DSP are made to drive the IGBTs in the IPM module for constant *V/f* speed control of three phase induction motor. The same approach (e.g., assigning two push buttons for the increase/decrease of speed in steps of 10 rpm) as followed for FPGA based implementation is followed here for the comparative analysis.

V. Experimental Results

Before realizing the FPGA and DSP based open loop *V/f* control of three phase induction motor the PWM patterns generated using both the technologies were tested using a Prototype PWM Testing unit

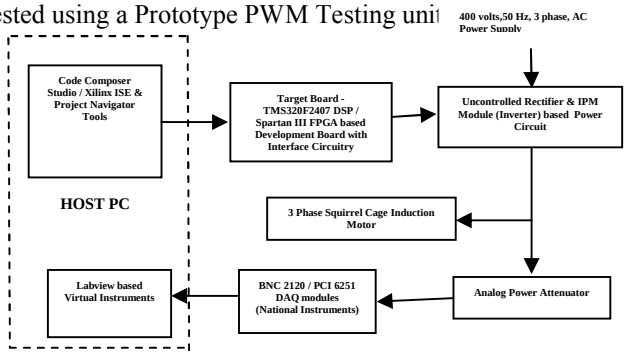

Fig. 6.a. Experimental setup

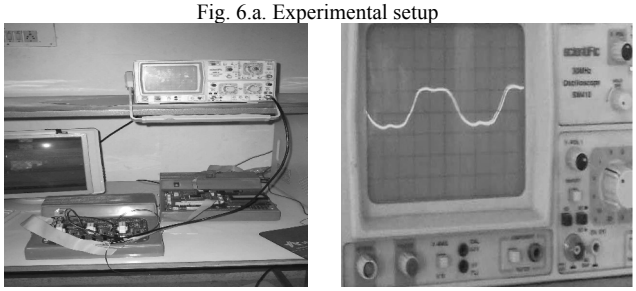

Fig. 6.b. Sample Photos of the Experimental setup

The output waveforms are captured and analyzed using National Instrument's data acquisition system. Figure 6 shows the setup used for the experiment and Figure 7 shows a sample SVPWM pattern out of the six patterns generated. It is observed the patterns generated using both the technologies are almost same.

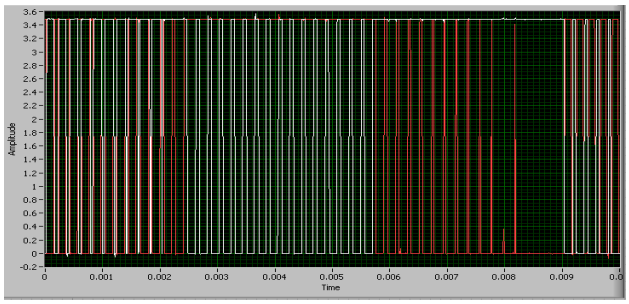

Fig. 7. SVPWM pattern – for switches in one arm

The following results are for a switching frequency of 10 kHz and other specifications are as can be seen in Table II.

TABLE II
SPECIFICATIONS OF THE HARDWARE SETUP USED

Motor rating

Phase	3 ph
Rated Voltage	415 volt
Rated current	9.5 Amps
Power	3 HP
Rated speed	1500 rpm

Intelligent Power Module Specification

IGBTs	8
Rated Voltage	1200 volt
Rated current	25 Amps

PWM Testing unit Rating

Transistors	6
Rated Voltage	5 volt
Rated current	.25 Amps

Since the SVPWM patterns generated are similar, the Phase and Line Voltage waveforms observed in both the ways of implementation and hence the Harmonic contents are also similar. Only sample waveforms are shown in Figures 8 and 9. Figure 10 shows a sample power spectrum of line voltage at 1490 rpm. The machine is run at different speeds from 300 rpm to 1490 rpm in steps of 10 rpm and at certain speeds the Harmonic Content is noted to verify the conformity of the algorithm in both ways of implementation. Table III shows the Harmonic content at three different speeds.

Compilation Report – FPGA based implemenation

Selected Device : 3s400pq208-4
Top Level Output File Name : svpwm
Optimization Goal : Speed
Number of Slices: 1438 out of 3584 40%
No. of Slice Flip Flops: 221 out of 7168 3%
No. of 4 input LUTs: 2082 out of 7168 29%
Number of bonded IOBs: 17 out of 141 12%
Number of MULT18X18s: 6 out of 16 37%
NUMBER OF GCLKS 2 OUT OF 8 25%
Maximum cicuit delay time : 9.342ns
(5.960ns logic, 3.382ns route)
(63.8% logic, 36.2% route)
Total equivalent gate counts for design: 44,770

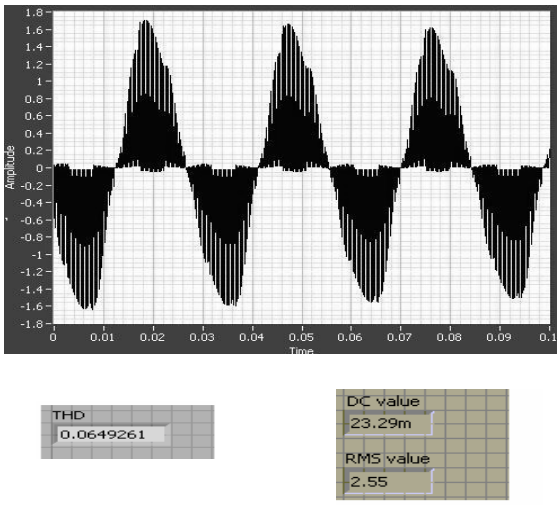

Fig. 8. Phase_A Voltage at 1490 rpm

Output summary – DSP based implementation

Selected Device : TMS320F2407
Total no.of Instrution cycles: 167
% of CPU loading: 20.07 @ 40 MHz clock
Total Execution time: 417.5ns

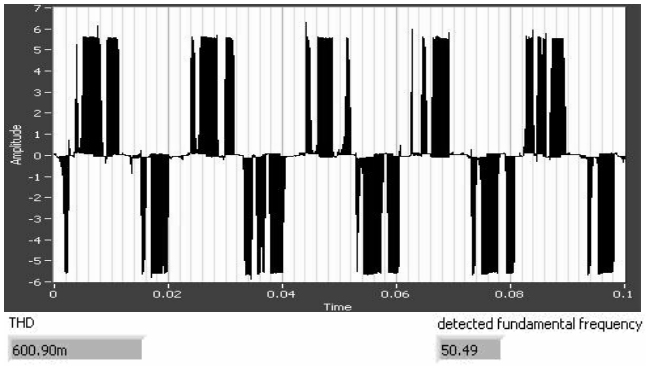

Fig. 9. Line to Line Voltage – 1490 rpm

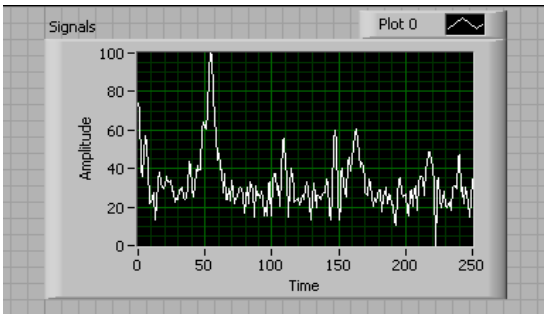

Fig. 10.Power Spectrum - Line to Line Voltage at 1490 rpm

Though there is not much difference in the final outcome of the algorithm this attempt is made to throw light on the advantages and superiority of FPGA based solution for Industrial Drives.

TABLE III
HARMONIC CONTENT OF THE LINE TO LINE VOLTAGE

SPEED (rpm)	FUNDAMENTAL		THIRD HARMONIC		FIFTH HARMONIC	
	Freq. (Hz)	amplitude (dB)	Freq. (Hz)	amplitude (dB)	Freq. (Hz)	amplitude (dB)
500	16.13	62	48.39	48	80.65	30
1000	33.15	95	99.45	55	160.75	60
1490	50	100	150	60	250	47

Speed and size are the parameters under consideration. From the results listed above the total execution time taken by DSP is obviously higher than the circuit delay of the FPGA based implementation and percentage of CPU loading of DSP warns the space requirement. This is because of the inherent parallelism present in the FPGA. Other advantages like rapid prototyping, dynamic reconfiguration, high density integration and availability of Intellectual Property (IP) cores facilitates computationally intensive high performance Industrial Drives to be realized at ease.

VI. Conclusion

This paper presents the implementation of SVPWM based open loop constant *V/f* control of three phase induction motor using TMS320F2407 DSP and 3s400pq208-4–SPARTAN III FPGA individually. The algorithm was successfully implemented using both ways. As the entire digital controller fits into a single FPGA device and since the algorithm was implemented in terms of modules, the results prompts to two specific conclusions. Firstly, all specific modules needed for High Performance drives can be coded in any HDL and kept as a library of reusable IP cores. As per necessity, modules can be chosen and interconnected to implement the desired algorithm. Secondly, the comparison of the results from FPGA with the existing solution namely DSP based implementation in terms of size(memory) and execution time confirms the possibility of proposing any complicated algorithm and their realization on a System on a Chip (SoC) with fastest execution time, less space and less time to market.

This work was carried out to assess the possibility of complete digital realization of SVPWM based *V/f* control algorithm in open loop and has become successful. Realization of Digital antiwindup-PI controller, Clarke's Transformation, Parks Transformation and Flux model have been realized as individual modules and are being integrated by the authors for implementation of a closed loop vector control. Further this can be implemented in FPGA based Embedded System Development kits where part of the modules will be realized as custom logic and rest to be implemented in the soft core processor to get the advantages both the solutions.

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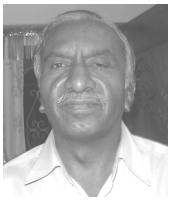

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