Design of Low Power and Area Efficient CSD-VHCSE FIR Filter using UAS based CSLA-AS

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Abstract:

Digital Filters are the significant component required in most DSP (digital signal processing) applications. This proposed work plays a significant role in low power consumption and reduction in area. Several researchers studied and investigated about reducing the switching activity of the adder blocks and their approaches do not provide better accuracy. To obtain high throughput, as well as low power and area consumption, an improved architecture for efficient Unified Adder/Subtractor (UAS) based Carry SeLect Adder(CSLA) Adder/Subtractor implementation of the digital signal processing parts are preferable. This method performs simultaneous calculation of sum and difference of two operands with less area and low power. This Unified Adder/Subtractor reduces the power consumption of the circuit with at least one order of magnitude compared to a flexible implementation using digital signal processors. The proposed technique helps in reducing the area and power consumption for different orders of filter by 58.5% and 64.9% respectively. The experimental results of Finite Impulse Response (FIR) in the range of 10 -100 taps and the coefficients of 8, 12 and 16 shows the improvement results when compared to the canonical signed digit based vertical and horizontal common sub-expression elimination (VHCSE) algorithm. The simulation results are obtained with the help of Cadence RC tool in TSMC 180 nm technology.

Keywords : UAS - Unified Adder/Subtractor, Finite Impulse Response (FIR), multiple constant multiplication (MCM), optimization method, Canonical Signed Digit (CSD)

1. Introduction

Due to the requirements on high data rates in many communication systems, the corresponding subsystems and circuits must have a high throughput as well. Since significant parts of such communication systems are customer products that are produced in large quantities and are sold at low prices, efficient, fast, and reliable design methods as well as low cost circuit implementations are required [17]. The possibility of integrating an entire system or parts of a system, on a single chip also requires subsystems with low power consumption. For such integrated systems, where analog and digital circuits may be implemented on the same chip, the heat dissipation and the cooling of the chip becomes a problem [18]. Low power consumption is an important design limitation. Finite Impulse Response (FIR) is extensively applicable in Digital Signal Processing (DSP) as a result constancy and linear-phase property [16]. Nowadays, low power consumption and less area are the significant parameter for the manufacture of DSP systems. Several resource minimization and power reduction techniques have been proposed by the researchers and are implemented on designing FIR filters are studied. Jiatao et al. studied various ways to MCM minimization by benchmark FIR filters.

In this paper, Common Sub-expression Elimination algorithm is proposed to search for the dual common expressions and map into unified adder/ subtractor (UAS) units [1]. This method concludes that it provides 20.4% of area efficient and 12% of power efficient. For low complexity FIR filter design addition aware quantization technique is used Oscar et al., [9].Constant shift method and programmable shift method are applied for low complexity design by using Common Sub-expression Elimination [12]

Solomon and Nirmal explored on the design of ESPFFIR filter based on Multiple Constant Multiplier (MCM) which functions according to Common Sub-expression elimination and modified Carry SeLect Adder (CSLA) is used for area consumption and power consumption. The achieved reduction using the modified CSLA approach is 20% for power and 15% for area than the Carry Save Adder (CSA)[2]. For resource reduction trouble in scheduling scheme bit level optimization has been applied for an efficient area and power reduction for MCM design(Yu et al., 2014)[11]. Indranil et al. proposed an approach for the design of FIR filter to reduce area and power consumption for FIR filter design. This technique uses reconfigurable multiple constant multiplier based on canonical signed digit (CSD) Vertical and Horizontal common sub expression elimination algorithm (VHCSE). This method provides the improvement of area and power reduction of 57.5% and 61.9% respectively [3]. Jiajia et al. proposed the new logic formation design to reduce the area and power consumption. In this paper, a different method is used for reducing the number of adders and subtractors. This method effectively reduces the area and power by synthesizing the filter coefficients based on Genetic Algorithm which solves the integer programming problem to increase the cost savings of Tap Delay and Accumulate. The simulation results showed the less area and power consumptions in this approach are 26.8 % and 27.5% respectively [4]. Tsao and Choi. presented the symmetric convolution techniques which is used to minimize the number of multiplier in even and odd length parallel FIR filter in with additional adders in the preprocessing and post processing module[5], [6].Hatai et al. presented a novel VHBCSE technique that removes CS by using 2-bit BCSE vertically and also performed horizontally in order to reduce switching activities of multiplier adder block [7]. To minimize the area non-uniform coefficient quantization using truncated multipliers [8]. To allow efficient trade off, a low power reconfigurable method is used [10].

To improve the reduction in area and power consumption for the design of Finite Impulse Response (FIR) digital filter, the proposed system makes use of Unified Adder/ Subtractor. This technique improves the area-power efficiency by reducing the number of coefficient multiplier block for different order of filter.

The main contribution of this paper is as follows;

- Multiple Constant Multiplication hardware was design with the help of Unified Adder/ Subtractor based on CSLA Adder/Subtractor (AS).
- Significant amount of gate count reduced for the filter design while applying UAS
- Multiple Constant Multiplication (MCM) architecture based on UAS method is efficient for reducing the power consumption considerably by minimizing the average switching activities of the adder blocks used in Multiple Constant Multiplication.
- The proposed Unified Adder/Subtractor (UAS) based CSLA-AS logical element makes use of smaller number of resources for simultaneous calculation of sum and difference of two operands with a reduced amount of area and power.

The organization of the paper is as follows: Section I describes the introductory part of the proposed framework and the investigations of several researches papers, section II clarifies the proposed framework, section III states the obtained simulation results and their discussion and section IV concludes the paper.

2. Proposed Method

2.1. Problem statement

Generally, the power and area consumption are the major trouble of Multiple Constant Multiplication design which increases

the filter length linearly. The graph based CSD algorithms required to run on a highly well-organized stage for a period of few hours in order to obtain optimized filter hardware. The use of number of adders for adding the partial products maximize the switching activities that increases the power for the implementation of coefficient multiplier block. Reducing the area and power for MCM is one of the challenging tasks carried out by the designer so far. There are several techniques proposed by the researchers to reduce area and power for the filter design. But it does not provide better improvement like FIR filter synthesis technique used by the proposed system.

2.2. Overview

The proposed method is based on Unified Adder/ Subtractor CSLA-AS as shown in Figure.1. For coefficient multiplier unit the Unified Adder/ Subtractor technique is used which is applicable for the FIR filter designer in order to reduce the adder cells and the dynamic power. Two stages involved for the filter design are mentioned below:

(i) Non-Zero Term (NZT) reduction on the basis of canonical signed digit

The signed binary representation to the CSD representation has been done by binary to canonical signed digit convertor block which reduces the number of non-zero terms available in the coefficient up to 50 percentages (Ram kumar &Kittor, 2012)[13]. However it makes efficient results than the binary format when applying UAS method.

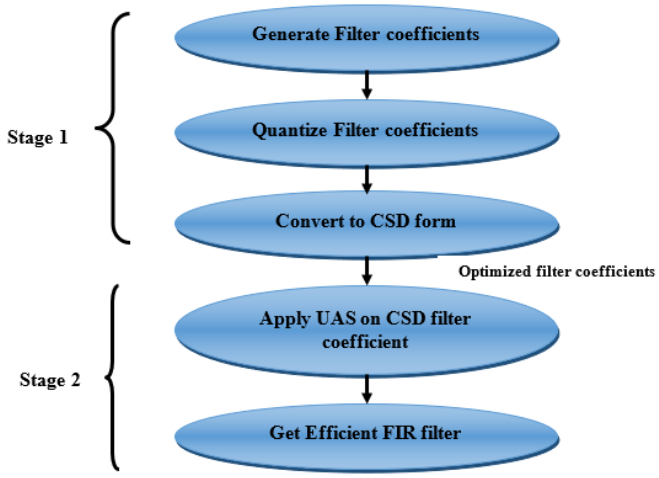

Fig.1 Reconfigurable coefficient multiplier dataflow

(ii) Unified Adder/Subtractor (UAS)

The proposed coefficient multiplier hardware architecture is designed with Unified Adder/ Subtractor based CSLA-AS considering 16-bit.The architecture of the UAS based CSLA-AS constant multiplier is shown in Figure.2

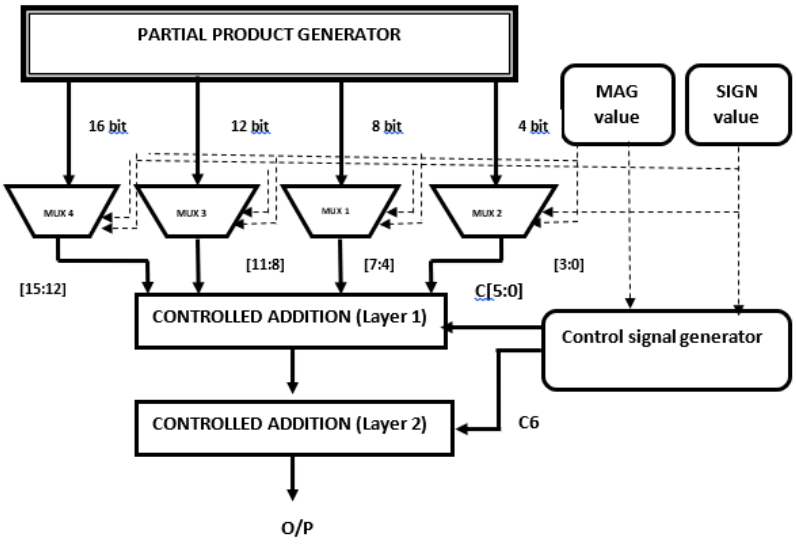

Fig.2 Proposed Unified Adder/ Subtractor architecture design

In the proposed architecture UAS was designed to design a 16-bit UAS based CSLA-AS. The UAS CSLA consist of UAS-1 and UAS-2 with carry in (Ci), borrow in (Bi) which is equal to 'zero' and 'one', at last the sum, difference and carry out (Co), borrow out (Bo) are chosen based on the actual carry and borrow input using the multiplexer unit. The 16-bit constant multiplier architecture was designed with the help of UAS CSLA unit. When the 16-bit UAS based CSLA used as a unified adder/subtractor instead of separate adder/subtractors unit like CSD based VHCSE adder UAS reduce the number of logical gate used for in the design. As a result of this the proposed UAS based CSLA-AS require low area and power consumption (Meher&Park,2014)[15]. The less consumption area and power of Canonical Signed Digit (CSD) based Vertical Horizontal Common Sub-Expression Elimination (VHCSE) was compared with modified UAS CSLA-AS. The novel UAS based CSLA adder consume 15% less area and power compared with CSD based VHCSE Adder/Subtractor. The Multiple Constant Multiplier (MCM) was design by using UAS based CSLA-AS to reduce area and power consumption. In the proposed method the UAS based CSLA-AS is applicable for MCM design.

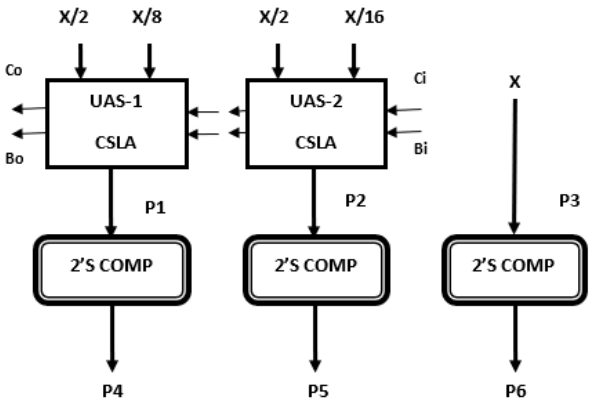

Fig.3 Partial Product Generator Block

In the proposed architecture the adders and subtractors are replaced by UAS CSLA which performs the functions very faster when compared to the existing adder. The unified operators available in the Multiple Constant Multiplication are replaced by UAS CLSA-AS to reduce the consumption of area and power of MCM used in the FIR filters (Chen et al,2015)[14]. Shift and ADD based method is the most significant one for the constant multiplier architecture which functions based on UAS because of its gate count reduction. By using UAS instead of adder/subtractor the number of gates has been reduced. Moreover the partial products (P1-P3) can be generated based on the AS shifted version of input variable 'X'. The partial products (P4-P6) which is considered as negative partial products has been generated by taking the two's complement of the real products (P1-P3) as shown in Figure.3.

3. Simulation Results and Discussion

In this section, the obtained result for Constant Multiplication architecture is discussed. UAS applied on CSLA-AS to reduce the consumption of area and power based on the design. So far researches have not implemented UAS based CSLA on MCM design. Henceforth a novel technique, UAS based CSLA is applied on the constant multiplier architecture which provide 15% of reduction than the CSD based VHCSE. This helps in decreasing the gate count implemented on the MCM system to design FIR filter.

3.1. Implementation Environment

The coefficients for different FIR filter description for the proposed MCM system is implemented with the help of Cadence RC tool in TSMC 180 nm technology. The algorithm was coded using Verilog HDL and synthesize in the xilinx ISE 9.2i synthesis tool.

3.2. Experimental Results

The following steps show the results obtained by giving the UAS instead of Adder/Subtractor. UAS based CSLA-AS techniques are applied on the constant multiplier design to minimize the area and power consumption. The various resultant parameters used for the filter design are given in Table.1. In this table the proposed method is compared with different filter length for various designs of different length.

Table. 1: Comparison result of various parameters for filter design

Design	Filter length	Target device	Slice Register	Slice LUT	MSP (ns)
DA-based [15]	16-tap	XC5VSX95T	1120	755	2.27
Serial Multiplier based [19]	8-tap	XC4VFX100	196	379	2.71
VHBSCE based [7]	20-tap	XC4VFX100	320	583	8.05
Proposed	16-tap	XC4VFX100	152	329	7.98

Slice LUT: Slice Look Up Table, MSP : Maximum Sampling Period

The results depicted in Table.1 shows that the Slice register and Slice LUT for the proposed design are 152 and 329 respectively on XC4VFX100 FPGA device which achieves less maximum sampling period than those of the Finite Impulse Response designed previously based on DA-based FIR filter design [15] and Serial Multiplier[19].

The proposed coefficient multiplier using UAS based CSLA-AS has been applied in various FIR filter wherever all the filters consists of different pair of coefficients for various requirements. The length of the coefficient compared is 8-bit, 12- bit and 16-bit respectively. Therefore, the advantages of the UAS based CSLA in comparison with those of CSD based VHCSE and EDBNS are mentioned in Table.2, 3 and 4. The result depicted in Table.2 shows that the required gate count for FIR filters of 10 different length.

Table.2: Comparison of proposed 8-bit coefficient UAS based CSLA-AS gate count with CSD based VHCSE [3]and EDBNS [14]

Filter length N	CSD based VHCSE [3]	EDBNS [14]	Proposed UAS based CSLA-AS	Imp % [3]	Imp % [14]
10	1209	2402	1001	17.2	58.3
20	2295	4774	1891	17.6	60.4
30	3348	7129	2762	17.5	61.3
40	4444	9490	3671	17.4	61.3
50	5605	11853	4635	17.3	60.9
60	6708	14208	5561	17.1	60.9
70	8077	16573	6696	17.1	59.6
80	9239	18932	7668	17.0	59.5
90	10371	21280	8618	16.9	59.5
100	11516	23653	9616	16.5	59.3

According to the proposed coefficient multiplier architecture using UAS based CSLA-AS technique used in FIR filter design using 8-bit coefficient which compares the improvement power consumption for EDBNS [14] and CSD based

VHCSE [3] Table.2 reveals that the proposed design achieves better result than the existing methods.

Table.3: Comparison of proposed 12-bit coefficient UAS based CSLA-AS gate count with CSD based VHCSE [3]and EDBNS [14]

Filter length N	CSD based VHCSE [3]	EDBNS [14]	Proposed UAS based CSLA-AS	Imp % [3]	Imp % [14]
10	1912	3556	1589	16.9	55.3
20	3661	6833	3053	16.6	55.3
30	5577	10083	4651	16.	53.9
40	7400	13358	6186	16.4	53.8
50	9476	16642	7950	16.1	52.2
60	11369	19900	9550	16.0	52
70	13240	23160	11122	16.0	52
80	15131	26459	12740	15.8	51.9
90	17480	29710	14736	15.7	50.4
100	19520	32975	16475	15.6	50.0

For simple comparison between the proposed architecture and the earlier designs the Table. 3 demonstrate the result for 12-bit coefficients for efficient FIR filter synthesis and 7-linear phase band pass filters used are mentioned. The less power consumed for the design has been evaluated regarding the input clock frequency of range 50 MHz.

Table.4: Comparison of proposed 16-bit coefficient UAS based CSLA-AS gate count with CSD based VHCSE [3]and EDBNS [14]

Filter length N	CSD based VHCSE [3]	EDBNS [14]	Proposed UAS based CSLA-AS	Imp % [3]	Imp % [14]
10	2830	4640	2389	15.6	48.5
20	5544	9112	4690	15.4	48.5
30	8361	13596	7065	15.5	48.0
40	11402	18095	9680	15.1	46.5
50	14172	22569	12046	15.0	46.6
60	17486	27055	14898	14.8	44.9
70	20447	31533	17462	14.6	44.6
80	23378	36020	19988	14.5	44.5
90	26266	40502	22483	14.4	44.5
100	29265	45000	25080	14.3	44.3

RTL SCHEMATIC OF PROPOSED DESIGN

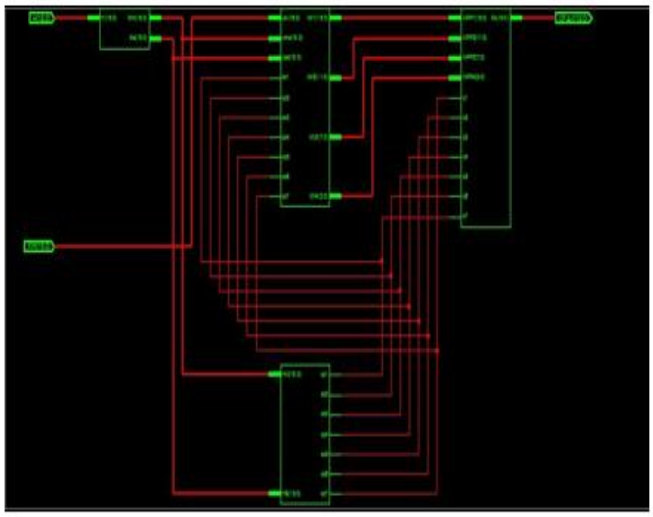

Fig.4 Output for UAS based CSLA

Figure.4 shows the output for Unified Adder/ Subtractor based CSLA.After observation of simulation waveforms, synthesis is done for the calculation of area and power comparison of adder architectures are made in terms of area and power are listed in Table.5.

Table. 5: Comparison of different adders

Adder	Coefficient bits	Area(μm^2)	Power (mW)
SQRT CSLA [13]	16-bit	2272	527.25
Modified SQRT CSLA[13]	16-bit	1929	471.84
UAS CSLA	16-bit	845	409.17

From the above table it is clear that area and power is less in UAS based CSLA is compared with SQRT CSLA [13] adder and Modified SQRT CSLA[13] architectures. The proposed UAS based CSLA achieves the area and power for 16-bit coefficient bits are 845(μm^2) and 409.17 (mW) respectively which is less than the earlier design of SQRT CSLA and Modified SQRT CSLA for an efficient FIR filter design. Figure.5 shows the performance analysis of proposed UAS based CSLA-AS design area and power with existing techniques

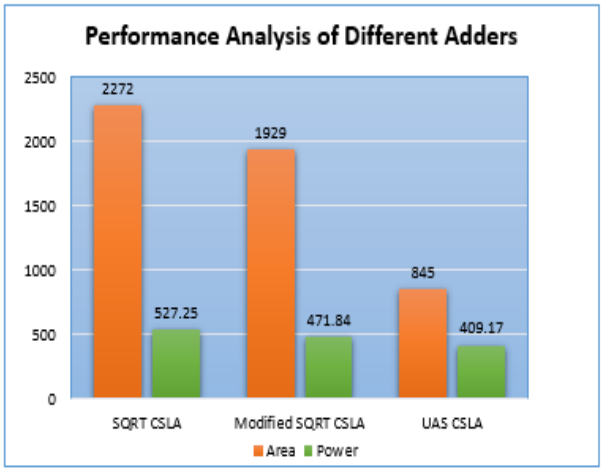

Fig.5 Performance measures of different adders

4. CONCLUSION

Area and Power reduction in FIR filter has been much researched in recent years, due to the significance of multiplication and addition in Digital Signal Processing system. In this research, various adders are analyzed on the basis of area and dynamic power dissipation. According to the analysis of different adders, the FIR filter is designed by using Unified Adder/Subtractor based CSLA adder for area and power consumption also improving their performance than the CSD based VHCSE FIR filter. The UAS based CSLA-AS FIR filter consumes 15% reduction of both area and power than the earlier design method. The less area and power consumption results are shown by using Cadence RC tool and synthesized in the Xilinx using ISE 9.2i simulator.

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