LIMITS OF DC BUS BEHAVIOR ON PHOTOVOLTAIC SYSTEMS IN DISTRIBUTED ARCHITECTURE

H. ALLOUACHE A. ZEGAOUI*
LGEER Laboratory, UHB University, Algeria
BP151, Hay Essalam, Chlef, Algeria. hallouach@gmail.com, abd.zegaoui@gmail.com *Corresponding author.

G. BACHIR
USTO University, Oran, Algeria
ghalem.bachir@yahoo.fr
A. DJAHBAR A. DELLALI
LGEER Laboratory, UHB University, Algeria
BP151, Hay Essalam, Chlef, Algeria. a_djahbar@yahoo.fr, abdelkader2006elt@hotmail.fr.

M. AILLERIE
Université de Lorraine, LMOPS, EA 4423, 57070 Metz, France.
Centrale Supélec, LMOPS, 57070 Metz, France. michel.aillerie@supelec.fr.

Abstract: *This study focuses on a photovoltaic (PV) chain constituted by a photovoltaic (PV) generator, a boost converter and a load. The principal target is to study a distributed photovoltaic (PV) architecture feeding a direct current bus. To do this we will outline a new vision concerning the influence of environmental variables, solar irradiance and temperature on the position of the maximum power point. Thereafter we analyzed the influence of load variation on the behavior of the boost converter and we deduced the limits of the imposed load on the converter. Thus, the displacement of the maximum power point due to the influence of the simultaneous variation of the duty cycle and load on the parameters of the photovoltaic chain components is discussed by an original way.*

Key words: *Distributed photovoltaic architecture, direct current bus, Boost converter, photovoltaic module, maximum power point tracking, duty cycle, optimum power point, load limits for the boost.*

1. Introduction

The integration of renewable energy sources and especially the photovoltaic (PV) generators into the power networks and for supplying autonomous users continues to increase. The photovoltaic (PV) power harvesting has greatly contributed to solve problems of the increasing demand of energy and global warming [1-2]. In order to supply a high voltage direct current (HVDC) bus with a voltage range between 100 V and 1 kV from photovoltaic generator (PVG) and power electronic interface as boost converter is needed [3-4]. A Step-Up DC-DC converter has two important roles: first to meet the voltage demand of the used high voltage direct current (HVDC) bus and second to track the maximum power point in order to transfer the maximum power available in the photovoltaic generator (PVG) [5-6]. Maximum power point tracking algorithms are used to elaborate the signal control of the boost power switch in order to reach the photovoltaic generator maximum power point (MPP) under considered environmental conditions [7-12]. Several Step-Up converter have been proposed in the literature for impedance adapting and interfacing between the photovoltaic source and the load. In [13-15], a switched capacitor technique is chosen for high gain conversion systems. To generate from photovoltaic sources a high step-up voltage, coupled inductor converter are widely discussed in [16-21]. The tapped inductor boost is developed for several application in [22-25]. In this article, we will give a new approach to the study of a photovoltaic system consisting of a chain: photovoltaic generator, boost converter and a load. The target is to build through simulation new characteristics of optimal current, optimal voltage and optimal power depending on the irradiation changes. The continuous conduction-operating mode (CCM) of the boost is explicitly discussed and the optimum duty cycle for reaching the actual maximum power point (MPP) is evaluated. The load limits (maximum and minimum) that the designed boost can powered without suffering are depicted. Thus, with a basic perturb and observe maximum power point tracking (MPPT) algorithm inserted in the system, a novel set of characteristics are developed according to the duty cycle variations.

2. Considerations on the photovoltaic generator

In this paper, we apply the one-diode physical model to the marketed photovoltaic panel ESM80S-125 in which we integrate parameters giving by data manufacturer. Simulated results under Matlab software are shown in Figure 1 and Figure 2. One can found the influence of the irradiation G and temperature T on each parameters such as optimal photovoltaic generator (PVG) current, optimal photovoltaic generator (PVG) voltage, optimal photovoltaic generator (PVG) resistor and its optimal

power.

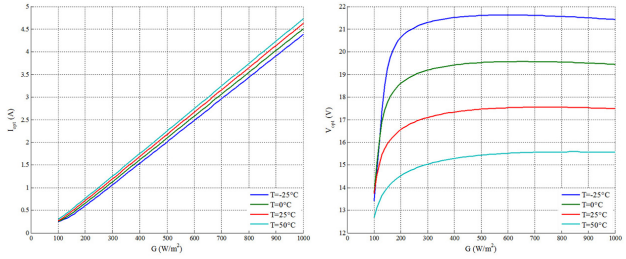

Fig1. Influence of both solar irradiation and temperature on the optimal current of the ESM80S-125 module and on its optimal voltage.

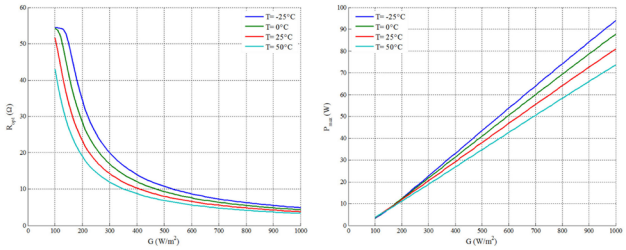

Fig. 2. Influence of both solar irradiation and temperature on the optimal resistance of the ESM80S-125 module and on its optimal power.

From the characteristics obtained in Figure 1 and Figure 2, we have developing a simple routine programmed under Matlab software, which can give the corresponding values at maximum power point (MPP) of the considered photovoltaic generator (PVG): the optimal current Iopt, the optimal Vopt, the maximum power Pmax and the optimal resistance Ropt.

We did a sort on the power vector thing that allows us to determine position of the maximum power point (MPP). Positions of the optimal current and the optimal voltage are deduced from the corresponding vectors. By analyzing these results, it appears that:

- For irradiation levels less than 100 W/m², this marketed photovoltaic generator (PVG) produces nothing.
- The Iopt current has sensitive variation due to the illumination: a variation of the illumination of 100 W/m2 causes a variation in the same direction of Iopt current of 10.58%.
- It is also clear from Figure 2, for illumination less than 200 W/m² and a given fixed temperature, the Vopt voltage varies with the illumination can even see straight and slightly decreases with temperature increase. For example, for a fixed irradiance of 1000 W/m2 and an ambient temperature of 25°C, when the temperature varies up or down 25°C, the Vopt voltage varies what about 10%. These results also show that at a fixed temperature, the Vopt voltage varies relatively little with any variation of the illumination beyond 200 W/m² and this variation can be constant.
- The maximum power Pmax has a sensitive variation according to the irradiation changes: when irradiation falls by 100 W/m², the Pmax power decreases by 10.4%. By cons, this maximum power slightly decreases with temperature especially for high illumination levels. Increasing temperature of 25°C around ambient temperature and for a fixed illumination of 1000 W/m² the Pmax power decreases by 9.0395%.
- The Ropt resistance of the studied photovoltaic generator (PVG) is very sensitive to the illumination, in particular low levels. At ambient temperature and around an illuminance of 300 W/m² (800 W/m²) when the illumination increases with 100 W/m², Ropt resistance value decreases by 28.0099% (11. 954% respectively). On the other hand, the temperature has a very little influence on this resistance. For an irradiance of 1000 W/m² and about room temperature: if the temperature increases by 25°C, the Ropt resistance decreases by 12.9686%.

In the ESM80S-125 module, the optimum resistance to its terminals must varies from 54.3812 Ω to 3.2898 Ω in order to exploit the photovoltaic generator (PVG) in optimum conditions. This corresponds to virtually any application, since the load always imposes the operating point within insertion of an adapting stage of impedance between photovoltaic generator (PVG) and the load.

3. Modelling of the boost converter associated to the photovoltaic generator (PVG) in the continuous conduction operating mode

We focus now on the details of the continuous conduction-operating mode of the boost converter. It is then necessary to size the converter components in order to avoid its discontinuous and critical operating modes that interrupted the return of the energy stored in the inductor.

Consider Figure 3, a photovoltaic system where the photovoltaic generator is suitable for resistive load Rch using a DC-DC Boost converter. The rigorous calculation of the boost elements: the inductance (L) and capacities (Ce, Cs) enables mitigation of the current ripples and minimizes the rate of the input voltage and the output ripple of the boost [7-8]. The RL schematically resistance in series with the inductor L, represents the internal resistance of the coil, it depends on the winding conductor and the number of turns. The output voltage adjustment is made by varying the duty cycle, which can be varied by acting on the conduction time, Tp, of the switch.

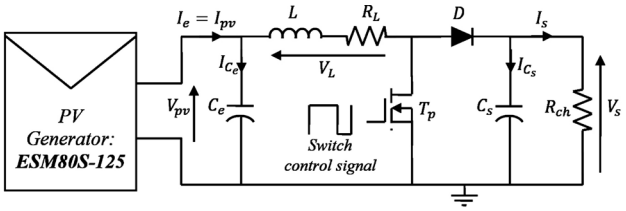

Fig. 3. The studied system; boost connected to the PV module and supplied a resistor load connected to the photovoltaic DC bus.

In what follows, we focus on the details of the continuous conduction-operating mode of the boost converter. It is then necessary to size for its components in order to operate only in this mode and to avoid the return of the energy stored in the inductor.

3.1 Continuous conduction mode (CCM)

When the current in the inductor Boost does not have time to cancel, we say that the Boost operates in continuous conduction mode (CCM). For this operating mode and considering the presence of the capacitors Ce and Cs, Figure 4 represents the shapes of the control signal of the power switch, the output voltage Vs, the current through the inductance IL, the current through the drain of the transistor ID and the voltage across the inductance VL.

The condition that the average voltage provided at the inductance terminals is zero in the steady state imposes the input voltage as an average voltage across the power switch [6]. Therefore:

$$V_{ch} = V_s = Y \times V_e \quad (1)$$

Where: $Y = \frac{1}{1-\alpha}$ and $0 \leq \propto \leq 1$ is the duty cycle of the switch control signal. Equation 1 shows that the converter is a boost. Since Y is constant for a fixed value of $\propto$ then in this case the conduction mode is continuous.

Assuming that the power exchanged between the photovoltaic generator (PVG) and the load is maintained, we can write:

$$V_{pv} \times I_{pv} = V_s \times I_s \quad (2)$$

Combining Equation 1 and Equation 2, one can establish relationship between currents on input and output terminals of the boost:

$$I_s = (1-\alpha) \times I_{pv} \quad (3)$$

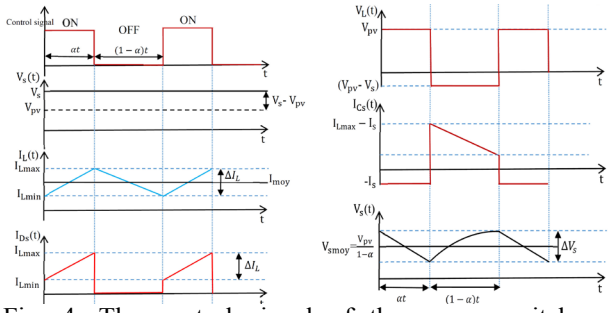

Fig. 4. The control signal of the power switch and waveforms of different instantaneous electrical quantities in the Boost operating in CCM in the presence of the capacitors Ce and Cs.

3.2. Ripple at the output

The presence of Cs capacitor to the boost output for filtering reduces the undulations in the output voltage. During ON time of the switch ($0 < t < \alpha T$) we can write:

$$V_L = V_{pv} = L\frac{dI_L}{dt} = L\frac{\Delta I_L}{\alpha T} \quad (4)$$

The expression of the current ripple ΔIL in the inductor is then:

$$\Delta I_L = \alpha \frac{V_{pv}}{L.f} \quad (5)$$

With $f = \frac{1}{T}$ is the switching frequency.

Figure 4 shows the current forms through the inductor IL, the diode ID, the output capacitor Cs and the boost output voltage Vs. The voltage ripple is derived from the following equation linking the output voltage Vs to the current through the capacitor Cs:

$$V_s = \frac{1}{C_s}\int I_{cs}\, dt + V_{s_0} = \frac{1}{C_s}\int (I_D - I_s)dt + V_{s_0} \quad (6)$$

Where: ID the diode current, Ics current through the capacitor Cs and Vs0 is the initial value of the output voltage.

When the diode is blocked (ID = 0 and the switch is in OFF state), the Cs capacitor is discharged through the load Rch. As the switching frequency of the control signal is high, the discharge time of the capacitor is faster. So the current through this capacitor Ics (or the output current Is) is practically constant.

Thus, Equation 6 becomes:

$$V_s(t) = \frac{1}{C_s}\int (-I_s)\, dt + V_{s_0} \quad (7)$$

By integration, we have:

$$V_s(t) = -\frac{I_s}{C_s}t + V_{s_0} \quad (8)$$

Since the change in the output voltage Vs is linear, we can deduce the expression of the ripple voltage ΔV_s in the form:

$$\Delta V_s = \left|V_s(t = \alpha T) - V_{s_0}\right| = \frac{I_s}{C_s}\alpha T = \frac{I_s}{C_s}.\frac{\alpha}{f} \quad (9)$$

We note that the output voltage, Equation 6, is linear when the transistor is in OFF state (ID is null) and parabolic when the transistor is in the ON state, see Figure 4. It therefore appears a ripple of the output voltage around the average voltage given by Equation 1. Then, we can deduce the value of the output capacitor Cs for a fixed ripple rate:

$$C_s > \frac{I_s}{\Delta V_s f}\alpha \quad (10)$$

Equation 10 can be written in a different way:

$$C_s > \frac{V_s}{\Delta V_s f R}\alpha \quad (11)$$

3.3. Ripple at the input

The inductor current is constituted of two

superposed currents: DC component ILmoy equal to the input current Ipv from photovoltaic panel and an alternating current ILalt that is a triangular signal in fact:

$$I_L = I_{Lmoy} + I_{Lalt} = I_{pv} + I_{Lalt} \quad (12)$$

In theory, the analysis of the ripple at the input side is assumed that the current delivered by the power generator is almost constant (for a fixed current of the generator).

On the other hand, in our case, this assumption is quite rigorous as the photovoltaic generator is not linear. The current Ipv can undergo ripples following the fluctuations of the voltage of the photovoltaic generator Vpv. The undulations current Ipv depend on the ripple factor of the Vpv voltage and can be minimized if we make a good sizing of the C_e capacitor. As part of our simulations, the current flowing in the Ce capacitor is given by:

$$I_{ce} = I_{pv} - I_L \quad (13)$$

Taking into account Equation 12, we can write:

$$I_{ce} = -I_{Lalt} \quad (14)$$

In Figure 5 we have presented the current waveforms in the inductor and from equation 13, we deduce the shape of the current in the capacitor Ce. The equation relating the voltage and the current in the capacitor Ce is given by:

$$V_{pv} = \frac{1}{C_e}\int I_{ce}\,dt + V_{pv_0} = -\frac{1}{C_e}\int I_{Lalt}\,dt + V_{pv_0} \quad (15)$$

With V_{pv0} is the input voltage at a given time (initial value).

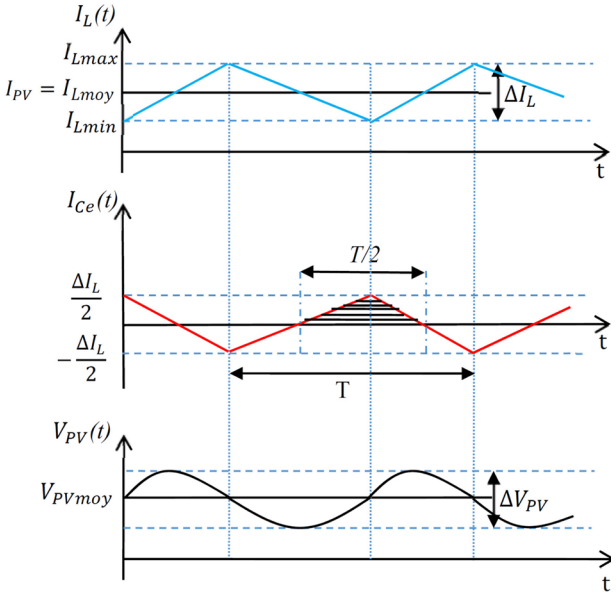

Fig. 5. Current shapes, in the inductor, in the input capacitor Ce and the ripple input voltage Vpv.

By integrating of Equation 15 over a half period (see the Figure 5), we can evaluate the ripple ΔV_{pv} of the input voltage. This integral is equal to the hatched area of the triangle as shown in figure 5 [11]:

$$\Delta V_{pv} = \frac{1}{C_e}\left(\frac{1}{2}\cdot\frac{T}{2}\cdot\frac{\Delta I_L}{2}\right) \quad (16)$$

According to equation 5, the expression of the ripple of the input voltage can be written in the form:

$$\Delta V_{pv} = \frac{\alpha V_{pv}}{8\cdot L\cdot C_e\cdot f^2} \quad (17)$$

Which leads to the relationship that determines the sizing of the boost input capacitance:

$$C_e > \frac{\alpha}{8\cdot L\cdot f^2}\cdot\frac{1}{\frac{\Delta V_{pv}}{V_{pv}}} \quad (18)$$

The inductance sizing play a very important role in the normal operating of the boost. The current in the storage phase of the energy in the inductor is the same current flowing through the MOSFET. A low inductance value can increase the current in the inductance and so the current in the MOSFET before the closing of this transistor, while a significant inductance value tends to increase the response speed of the boost against the variations of the duty cycle. This situation disturbs the maximum power point tracking (MPPT) circuit and increases the voltage undulations, thus of the power and produce a low output voltage.

For our application, the inductance L of the boost circuit is calculated for a duty ratio of 91.25% and an average switching frequency of 10 kHz with a maximum current of 7 A (30% of maximum current of the MOSFET). This inductance must be performed as high-frequency inductor with a ferrite core, and the lowest possible resistance made with a stranded wire so that the performance is better. The internal resistor of the inductance RL is neglected. Calculations conduct us to have:

$L > \frac{X_0 V_{pv}}{f I_{Smin}}$, $X_0 = 0.125$, $V_{pv} = 17.6\,V$, $I_{Smin} = 0.320\,A$

$L > \frac{0.125\times17.6}{10\times10^3\times0.320} \approx 700\,\mu H$, (most unfavorable case).

For input and output capacities, their values are based on the desired ripple voltage of 1%. The estimation of these two capacitors according to the previous equations for elements sizing is:

$$C_e > \frac{0.9125}{8\times700\times10^{-6}\times(10000)^2}\cdot\frac{1}{0.01} \approx 170\,\mu F$$

$$C_s > \frac{4.55}{0.01\times200\times10000}\times 0.9125 \approx 220\,\mu F$$

$\alpha = \alpha_{max} = 91.25\%$ the maximum duty cycle,
$I_S = I_{Smax} = 4.55\,A$ (most unfavorable case).

4. Impedance adaptation condition

In Continuous conduction operating mode (CCM) and from Equations 1 and 2, we can deduce Rpv the apparent resistance in the output terminals of the photovoltaic generator (PVG) as function of the duty cycle α and Rch the load resistance as follow:

$$R_{pv} = \frac{V_{pv}}{I_{pv}} = (1-\alpha)^2 R_{ch} \quad (19)$$

Which leads to:

$$R_{ch} = \frac{R_{pv}}{(1-\alpha)^2} \quad (20)$$

And

$$\alpha = 1 - \sqrt{\frac{R_{pv}}{R_{ch}}} \quad (21)$$

Since the duty cycle α is always lower than 1 (α <1) and relating to Equation 21, one can conclude that the converter (Figure 3) plays the role of a boost if the load resistor Rch fulfills the following condition:

$$R_{ch} > R_{pv} \quad (22)$$

When the illumination varies from 100 to 1000 W/m² at a fixed temperature of 25°C, the optimum resistance Rpv of the marketed ESM80S-125 photovoltaic generator (PVG) varies from 51.5590 Ω to 3.78 Ω. Therefore, the Rch load resistor must be greater than 51.559 Ω (3.78 Ω) for the same illumination level variations.

According to Equations 21 and 22, we can deduce that the impedance adaptation between the photovoltaic generator and the load will be achieved by changing the value of the duty cycle α.

Under optimal conditions and for a given load Rch, the resistance to the photovoltaic generator output terminals (Rpv = Ropt) and the duty cycle (α = αopt) must obey to the following equation:

$$\alpha_{opt} = 1 - \sqrt{\frac{R_{opt}}{R_{ch}}} \quad (23)$$

5. Variation range of load and limits of the boost and the tracking

The position of the maximum power point moves according to the resistance value of the load. Figures 6, 7 and 8 present the simulation results of the influence of the duty cycle and the load variation on the maximum power point position (MPP). Figure 6 shows clearly that the maximum power point (MPP) position moves in the same direction with the increase of the load resistance. This is valid to what the tracking algorithm automatically changes the value of the duty cycle.

As indicated in Figure 7 and Figure 8 and according to the use of a very small or a very substantial load, the maximum power point (MPP) can move outside the range of variation of the duty cycle [10% to 90%]. In such situation, the boost converter will be unable to bring the input voltage to the desired value by the maximum power point tracking (MPPT) algorithm.

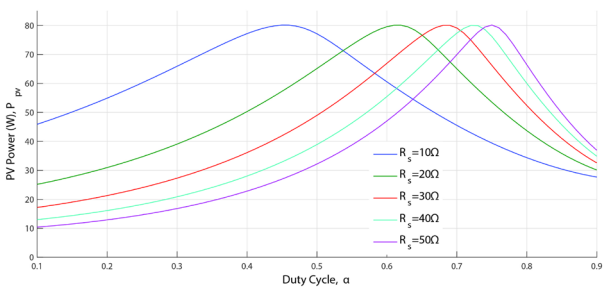

Fig. 6. MPP displacement as function of duty cycle and according to the load change at a fixed irradiation of 1000 W/m².

The maximum admissible load estimation must be made when the solar module has a minimum output impedance. This impedance corresponds to a maximum input power so to maximum irradiation of 1000 W/m2 and for a maximum current 4.55 A (see the photovoltaic generator datasheet). This current provides a voltage of 17.6 V for maximum power of 80 W. Under these conditions, the boost converter must use a maximum duty cycle (90%) to bring this impedance to the maximum impedance of the load. The current and the output voltage when the boost operates at such a duty cycle are equal to:

$$I_s = (1 - \alpha_{max}) \times I_{opt_{1000W/m^2}} = (1 - 0.9120) \times 4.55 = 0.4004A$$

$$V_s = \left(\frac{1}{1 - \alpha_{max}}\right) \times V_{opt_{1000W/m^2}} = \left(\frac{1}{1 - 0.9120}\right) \times 17.6 = 200V$$

This couple of current-voltage corresponds to a maximum impedance $R_{s_{max}}$ equal to:

$$R_{s_{max}} = \frac{200\ (V)}{0{\cdot}4004\ (A)} = 499.5005\ \Omega$$

Similarly, the minimum load must be calculated when the photovoltaic generator has a maximum load impedance (minimum current), so a minimal irradiation level (100 W/m2) which corresponds to a current value of 0.2663 A (one tenth of the maximum current). Therefore, from Figure 1 and Figure 2, and for a power of 3.6552 W this current gives an operating voltage 13.7283 V. To adapt this impedance with the minimum load, the boost converter must use a minimum duty cycle (10%), which corresponds in the ideal case to the following output voltage and current:

$$I_s = (1 - \alpha_{min}) \times I_{opt_{100W/m^2}} = (1 - 0.1) \times 0.2663 = 0.2397\ A$$

$$V_s = \left(\frac{1}{1-\alpha_{min}}\right) \times V_{opt_{100W/m^2}} = \left(\frac{1}{1-0.1}\right) \times 13.7283 = 15.2537\ V$$

With this couple of current-voltage results, the minimum impedance is equal to:

$$R_{min} = \frac{15.2537}{0.2397} = 63.6366\ \Omega$$

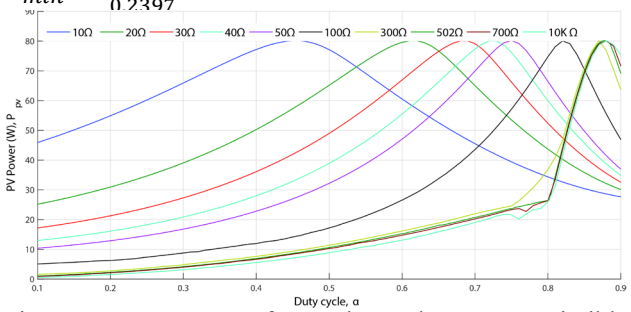

Fig. 7. No movement of MPP beyond upper permissible load limit at a fixed irradiation of 1000 W/m².

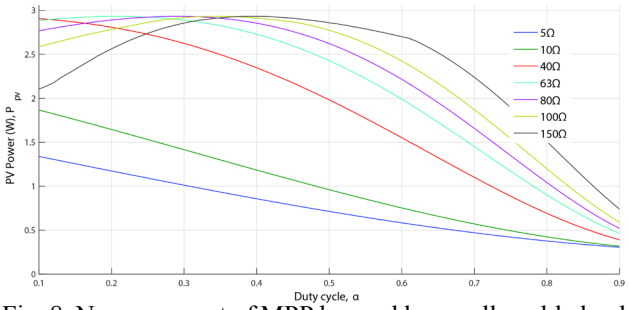

Fig. 8. No movement of MPP beyond lower allowable load limit at irradiation of 100 W/m².

Figure 6 and Figure7 approve the limits of the load impedance values that the boost can support without influencing the maximum power point by the variation of the duty cycle. It is quite clear in Figure 7 that the variation in the load beyond the upper permissible load value of 502 Ω, all photovoltaic power-α characteristics variation remain unchangeable. Also, Figure 7, too lower loads permissible value of 63 Ω we note the occurrence of the same phenomenon.

Conclusion

In this paper, we presented new analytical methods for studying photovoltaic generators. We graphically presented the evolution of the current, voltage and power of the optimum power point (MPP) based on both variation of two variables: the solar irradiation and the temperature. The same procedure is done for the resistance of the photovoltaic module at optimum power point (MPP) parameters. After modeling the boost in the continuous-operating mode, we presented a simple method for calculating the duty cycle to achieve the optimum operating point. In the studied system, we have also demonstrated that the boost converter has upper and down load limits that should be respected. Therefore, in case of a photovoltaic generator feeding a high voltage direct current bus via a boost converter, as demonstrated in this paper, load variation limits should be considered.

References

1. Razykov T M, Ferekides C S, Morel D, Stefanakos E, Ullal H S, Upadhyaya H M. Solar photovoltaic electricity: current status and future prospects.Solar Energy 2011;85,(8): 1580-1608.
2. Bratcu A, Munteanu I, Bacha S, Picault D, Raison B. Cascaded DC–DC converter photovoltaic systems: power optimization issues. IEEE Trans. Ind. Electron. 2010; 58(2) : 403-411.
3. Carrasco J M, Franquelo L G, Bialasiewicz J T, Galvan E, Guisado R C P, Prats M A M, Leon J I, Moreno-Alfonso N. Power electronic systems for the grid integration of renewable energy sources: a survey. IEEE Trans. Ind. Electron. 2006;53 (4): 1002–1016.
4. Kim H S, Kim J H, Min B D, Yoo D W, Kim H J. A highly efficient PV system using a series connection of DC-DC converter output with a photovoltaic panel. Renew. Energy, 2009;34 (11): 2432–2436.
5. Sahoo M, Kumar KS. High gain step up DC-DC converter for DC micro-grid application. IEEE International conference on Information and Automation for Sustainability,22-24 Dec. 2014; Colombo:IEEE.pp.1-5.
6. Farahat M A, Metwally H M B, Abd-Elfatah M A. Optimal choice and design of different topologies of DC–DC converter used in PV systems, at different climatic conditions in Egypt. Renewable Energy, 2012 ;43 : 393-402.
7. Zegaoui A, Aillerie M, Petit P, Sawicki J P, Charles J P, Belarbi A W. Dynamic behaviour of PV generator trackers under irradiation and temperature changes. Solar Energy, 2011; 85(11) : 2953-2964.
8. Bae H S , Park J H , Cho B H, Yu G J. New MPPT control strategy for two-stage grid-connected photovoltaic power conditioning system. J. Power Electron. 2007;7 (2):174-180.
9. Enslin J H R, Wolf M S, Snyman D B, Swiegers W. Integrated photovoltaic maximum power point tracking converter. IEEE Trans. Indust. Electron. 1997;44 (6): 769–773.
10. Esram T, Chapman P L. Comparison of photovoltaic array maximum power point tracking techniques. IEEE Trans. Energy Conver. 2007;22 (2): 439–449.
11. Jain S, Agarwal V. Comparison of the performance of maximum power point tracking schemes applied to single-stage grid-connected photovoltaic systems. IEEE Trans. Electron. Power Appl.2007; 1 (5): 753–762.
12. Liu F, Kang Y, Zhang Y, Duan S. Comparison of P&O and hill climbing MPPT methods for grid-connected PV converter. In: IEEE Conference on Industrial Electronics and Applications,3-5 June 2008;Singapore,IEEE. pp. 804–807.
13. Qian W, Cao D, Cintron-Rivera J G, Gebben M, Wey D, Peng F Z. A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count, IEEE Trans. Ind. Electron. 2012; 48 (4) :1397–1406.
14. Chung H, Mok Y K. Development of a switched-capacitor DC/DC boost converter with continuous input current waveform, IEEE Trans. Circuit Syst. I, 1999; 46(6) :756–759.
15. Gandmkar A, Seok J-J.Inductive-boost switched-capacitor DC/DC converter for maximum power point tracking photovoltaic systems. IEEE Energy Conversion Congress and Exposition (ECCE), 14-18 Sept. 2014;Pittsburgh,PA,IEEE.pp. 5296 – 5303.
16. Wai R J , Lin C Y, Duan R Y, Chang Y R. High-efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage, IEEE Trans. Ind. Electron. 2008;55 (10): 3702–3714.
17. Luo F L. Six self-lift DC–DC converters, voltage lift technique, IEEE Trans. Ind.Electron. 2001; 48 (6): 1268–1272.
18. Luo F L, Ye H. Advanced DC/DC Converters, CRC Press, Boca Raton, Florida, USA, 2004.
19. Nouri T, Babaei E, Hossein S. A generalized ultra step-up DC–DC converter for high voltage applications with design considerations, Electr. Power Syst. Res. ,2013,(105): 71–84.
20. Hwu K I, Yau Y T. Inductor-coupled KY boost converter, Electron. Lett. 2010;46(24): 1624–1626.
21. Hu X, Gong C. A high voltage gain DC–DC converter integrating coupled-inductor and diode–capacitor

techniques, IEEE Trans. Power Electron.2014; 29 (2): 789–800.
22. Shi Z H, Cheng K W E, Ho S L. Static performance and parasitic analysis of tapped-inductor converters, IET Power Electron. 2014; 7 (2) :366–375.
23. Grant D A, Darroman Y, Suter J. Synthesis of tapped-inductor switched-mode converters, IEEE Trans. Power Electron. 2007; 22:1964–1969.
24. Grant D A, Darroman Y. Extending the tapped-inductor DC-to-DC converter family, Electron. Lett. 2001; 37:145–146.
25. Cheng K W E. Tapped inductor for switched-mode power converters, Int.Conf. on Power Electronics Systems and Applications, 12-14 Nov 2006,Hong kong:pp.14-20.