IMPLEMENTATION OF DELTA PWM FOR AC–AC CONVERTERS USING FPGA

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Abstract – *Variable frequency AC to AC converters can be used to control the speed and the torque of AC motors, in aerospace and airline industries. In renewable energy systems, frequency converters are an essential component of doubly fed induction generators (DFIGs) as used in modern multi-megawatt class wind turbines. This paper presents an FPGA based variable frequency AC to AC converter which can step up as well step down the base frequency of 50 Hz. The output of the converter is improved by use of delta modulation techniques, which is flexible and effective in reducing the harmonic content to greater extent. The modulation technique is implemented on FPGA, which relieves the controller from the time consuming computational task of PWM signal generation, by implementing the method of trigger pulse generation in FPGA using Hardware Description Language VHDL in Xilinx. The trigger circuit is tested qualitatively by observing various waveforms on oscilloscope. The operation of proposed system has been found satisfactory.*

Keywords: FPGA; Delta PWM; VHDL; digital controllers; AC–AC converters

1. Introduction

Frequency changers are an expanding field of power conversion technology. These systems have been largely supplanted by static frequency changers using power semiconductor devices. Traditionally, AC–AC converters employ thyristors to regulate AC–AC power, i.e., phase-controlled AC–AC converters. This is largely due to cost, reliability, and larger power handling capability of thyristor switches. Such AC-AC converters, however, have slow response speed and need large input–output filters to reduce low-order harmonics. The use of self-commutated switches with PWM control can significantly improve the performance of AC-AC converter [1]. The output of the converter is however rich in harmonics. The conventional filter cannot be used for reduction of harmonics because the output frequency is varying and using tuned filter for each harmonic is not feasible. Hence the solution lies in the use of modulation techniques which are flexible and effective in reducing the output harmonic content to greater extent [2]. Various modulation techniques employed to improve the quality of load voltage are sinusoidal PWM [3], space vector PWM [4] and delta modulation [5-7]. In this paper delta, modulation technique has been applied for a generalized frequency converter because this modulation provides constant volts per hertz control for preset frequency range of operation and smooth transition to constant voltage mode of operation. The modulation technique is implemented in field programming gate array (FPGA), using hardware description language VHDL to generate the trigger signals for the proposed converter. FPGA are programmable semiconductor devices [8-9] that are based around a matrix of configurable logic block (CLBs) connected via programmable interconnects as opposed to ASICs where the device is custom built for a particular design [10-12].

2. Power Circuit

Fig.1 shows the circuit of the proposed variable frequency converter. It consists of two converters a positive converter PC and a negative converter NC connected in anti parallel. MOSFETs 1 and 2 form positive converter whereas MOSFETs 3 and 4 form negative converter, NC. The output of this converter will have a frequency either $f_o = f_i \times N_r$ or $f_o = fi/N_r$. Here N_r is an integer and f_i is the source frequency. There is a definite firing sequence

for a given value of N_r to generate the variable frequency output f_o. Figure 2 and Fig. 3 show the ideal waveform for an output frequency of $2f_i$ and $f_i/2$ respectively. A detailed study has been made in [13] to generate the trigger pulses for the cyclo-converter operation. Trigger requirements are obtained for single-phase centre tapped transformer configuration. The study has been extended here for a generalized frequency converter using FPGA.

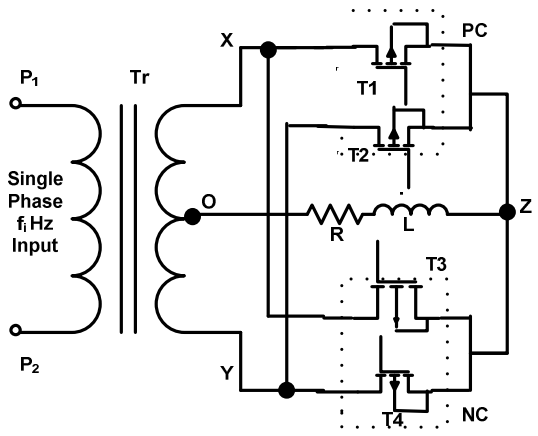

Fig. 1 The Power circuit of Frequency Converter.

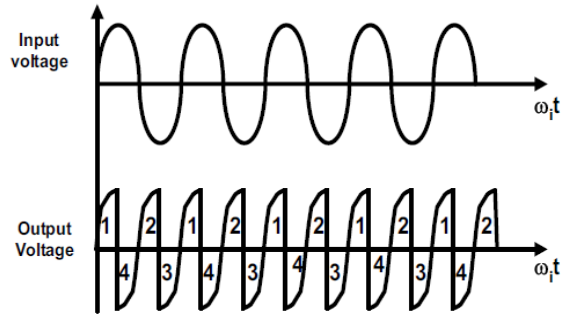

Fig. 2 Idealized waveform of converter for $f_o = 2 f_i$

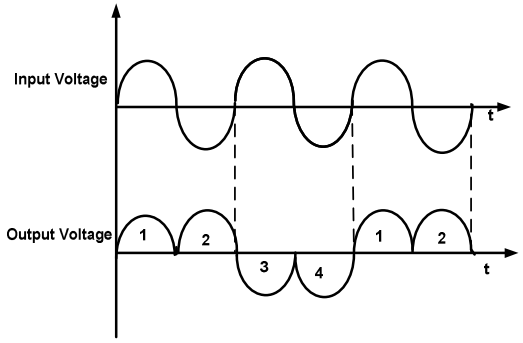

Fig. 3 Idealized waveform of converter for $f_o = f_i / 2$.

3. Principle of Trigger Pulse Generation

In order to optimize the harmonics and to improve the output of the converter, gate pulses to different MOSFETs are modulated using delta modulation technique. The basic principle of delta modulation is illustrated in Fig. 4. It utilizes a sine reference wave V_R and a delta shaped carrier wave V_F. The carrier wave V_F is allowed to oscillate within a defined window extending equally above and below the reference wave V_R. Fig. 5 shows the flow chart to generate the required delta modulated trigger pulses for the converter. The generation of different pulses required for delta modulated trigger signals are described in the following subsection:

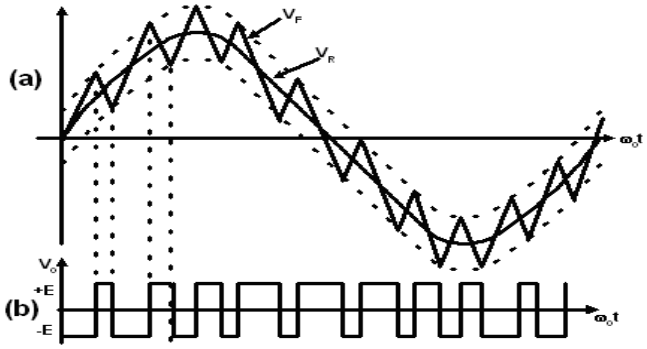

Fig. 4 Delta modulation technique.
(a) Reference signal and carrier signal V_f.
(b) Delta modulated switching function V_r.

A Carrier wave and Reference wave generation

The principle of delta PWM is implemented on FPGA using Xilinx. In the proposed work a 7 bit up/down counter is used that generates a 'M' shape sine wave carrier signal V_F. In order to have the sampled sinusoidal reference signal, data representing magnitude of the sinusoidal needs to be calculated first by using equation (1):

$$V_{ref} = \frac{(2^n - 1)}{10}\left(\sin(2r \times f_r\{2k+1\})\frac{1}{f_c}\right) \qquad (1)$$

Where 'k' is the carrier pulse position, 'n' the bit size of up-down counter, 'f_c' the clock frequency and 'f_r' is the reference frequency. The counter

digitally increments the counter value from 0 to 127 and then subsequently decrements it back to 0 over a period of time. Good accuracy requires high bit number. The digitized reference signal is compared with the sampled delta wave at high repetition rates to obtain the required time resolution.

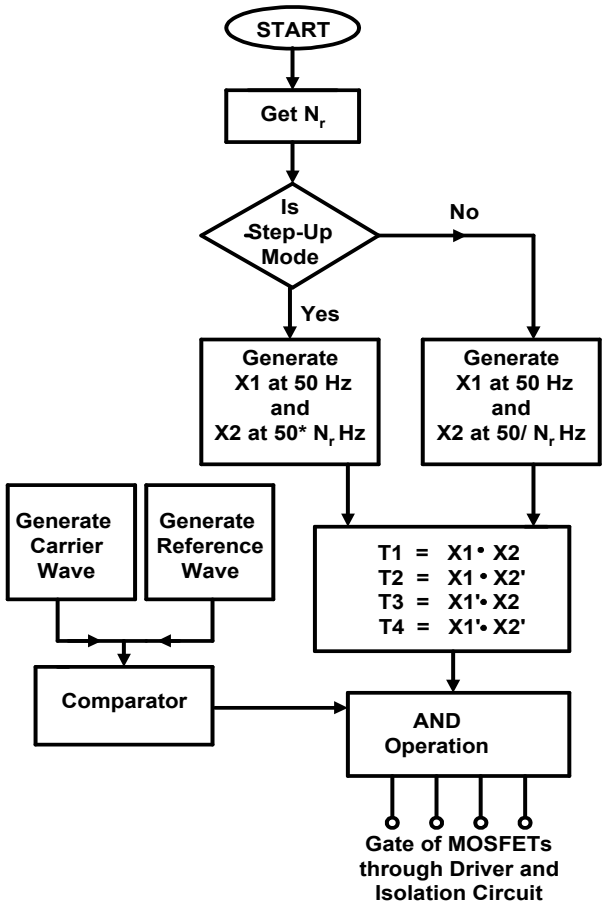

Fig. 5 Flow chart to generate the required delta modulated trigger pulses

B. Basic Pulse signal Generation

Two pulses X_1 (50 Hz) and X_2 (50* N_r) or X_2 (50/ N_r) need to be generated by control algorithm to generate the required switching pulses. The principle for generation of the desired frequency pulses is to divide the main clock of the FPGA by counting the number of clocks at which output wave is required. To get the desired clock pulse from the input clock of 50 MHz , it is required to calculate the on time and off time of the timer which are counted by equation (1). After counting these numbers of clock, counter will be set as one and after that output pulse is reset. Then again counting those clocks the output wave is set thus, giving the desired frequency output. Clock frequency of signal can be calculated by equation 2)

$$f_{out} = \frac{f_{clk}}{2(2^n - 1)} \qquad (2)$$

Where f_{out} = Desired output frequency
f_{clk} = Main clock of FPGA.
n = Number of clocks to be counted

C FPGA Implementation of Gating signal

Fig 6 shows the scheme for generation of gating signal on FPGA. Initially all the logical gating signals for a particular value of N_r are generated by VHDL programming in Xilinx ISE 9.2i software. Then AND operation of different pulses will result the required trigger signals for the four MOSFETs. These signals after modulating with delta modulating signal, generated earlier, are fed to the power circuit through isolation and driver circuit.

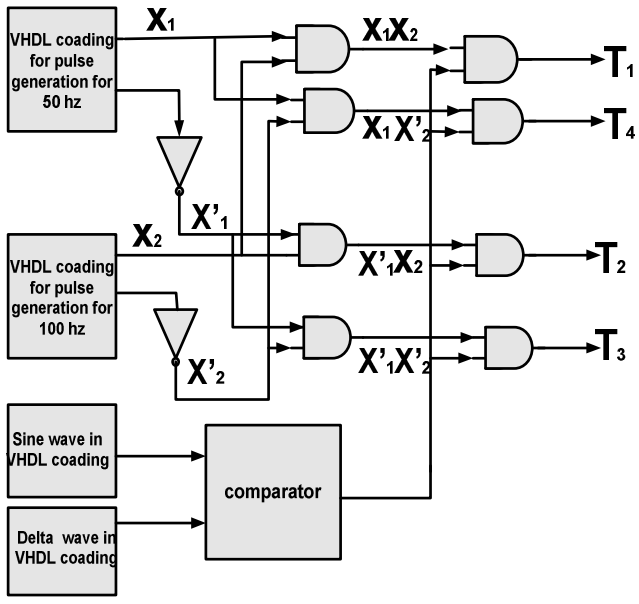

Fig. 6 Output gate pulses after logical operation.

4. Experimental Results

The trigger circuit has been tested qualitatively by observing various pulses on DSO. Fig. 7 shows the synchronized signal X1 of 50 Hz with signal X2 of output frequency 150 Hz (N_r = 3) signal for step-up converter. The signal X1 and X2 at 10 Hz for step-down converter are shown in Fig. 8.

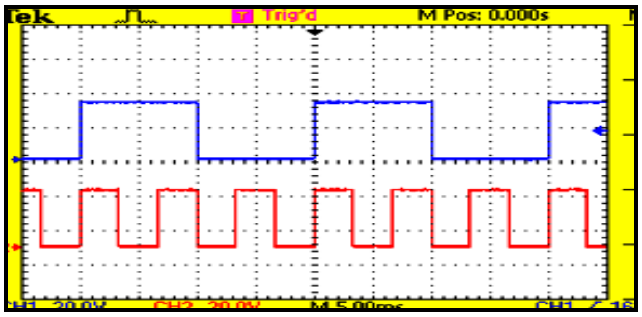

Fig. 7 Synchronization of X1 (upper trace) at 50 Hz and X2 at 150 Hz (lower trace)

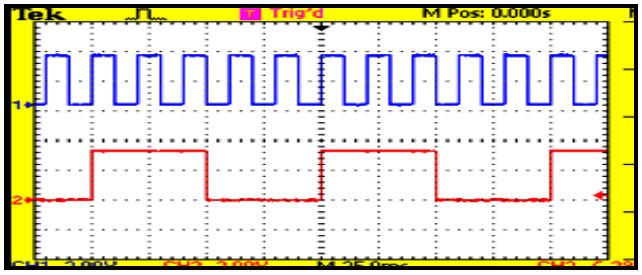

Fig. 8 Synchronization of X1 (upper trace) at 50 Hz and X2 (lower trace) at 10 Hz

Figures 9 and Fig. 10 show the desired four gating signals T_1, T_2, T_3 and T_4 without using delta modulation, generated in Xilinx chip XC4005XL.

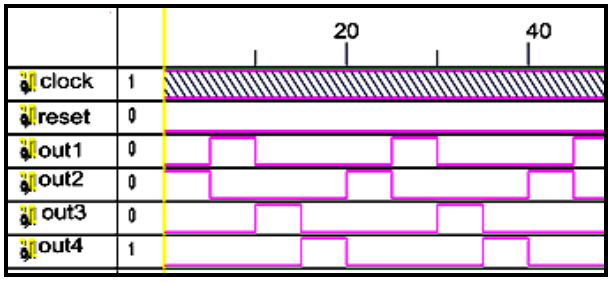

Fig. 9 Triggering pulse at f_o=100 Hz without delta modulation in text-bench.

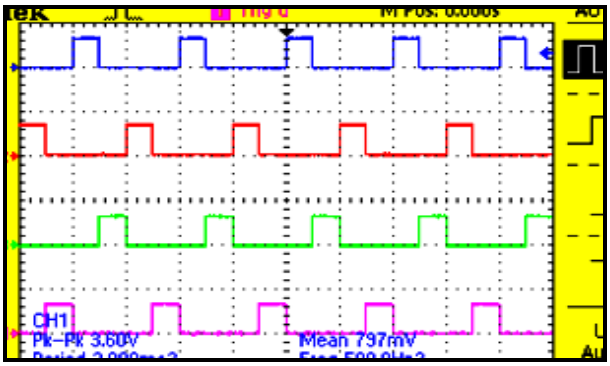

Fig. 10 Triggering pulse at f_o = 100 Hz without delta modulation on DSO

Delta PWM is shown in Fig 11 in text-bench while Fig. 12 shows the delta modulated pulse on DSO. Fig 13 and Fig. 14 show the desired four gating signals T_1, T_2, T_3 & T_4 in text-bench and then on DSO.

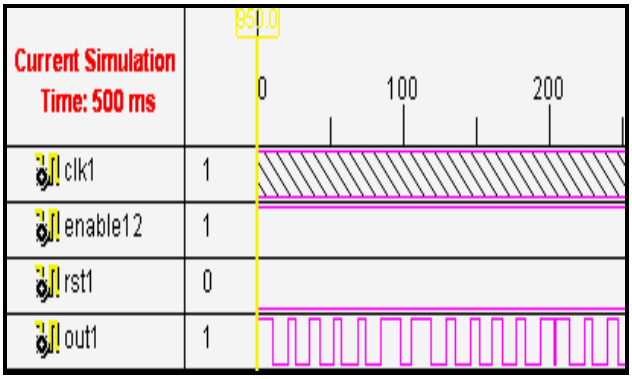

Fig. 11 Generation of delta PWM pulse in text-bench.

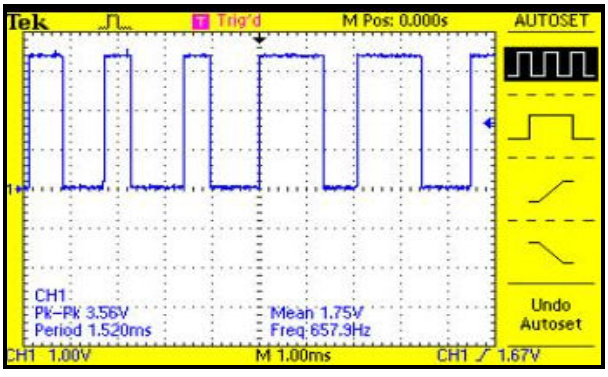

Fig. 12 Delta PWM pulse

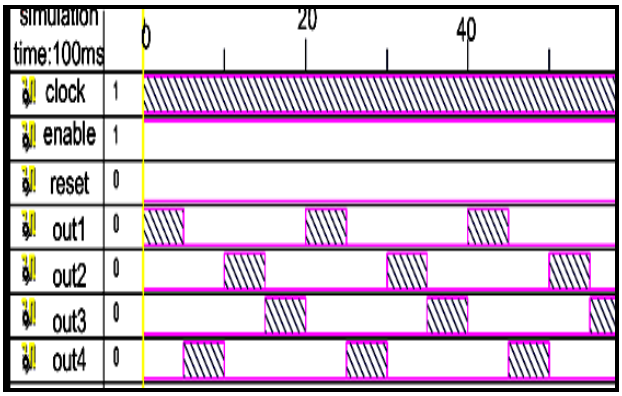

Fig. 13 Delta Modulated trigger signals in text-bench.

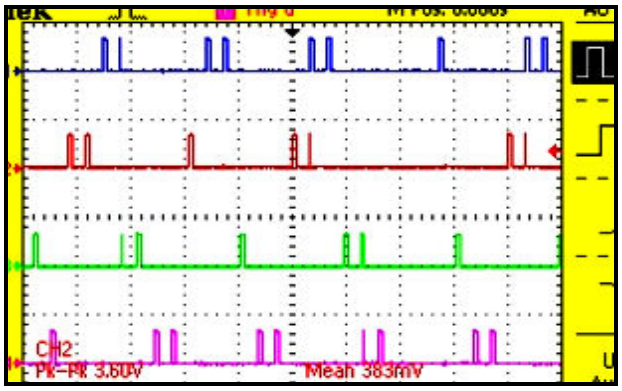

Fig. 14 Delta Modulated trigger signals for f_o = 100 Hz and f_c = 1 kHz.

Finally, Fig. 15 and Fig. 16 show the output voltages for the output frequency of 250 Hz and 10 Hz respectively with a carrier frequency of 2 kHz with RL load.

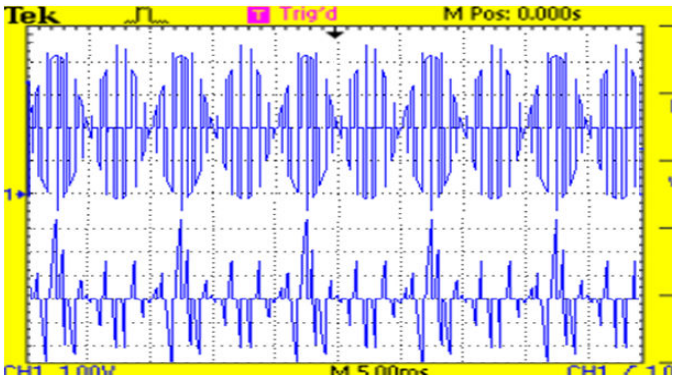

Fig. 15 Output voltage of Frequency Converter in step-up mode at f_o= 250 Hz.

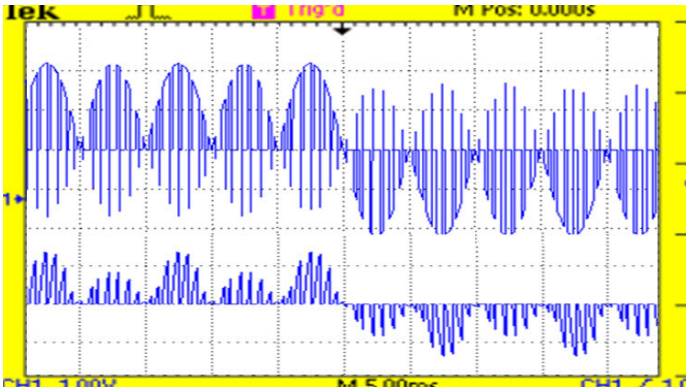

Fig. 16 Output voltage of Frequency Converter in step-down mode at f_o= 10 Hz.

Some regular spikes are observed in the voltage waveform because of the presence of the inductance in the load. It is observed that the spikes are more persistent in case of low output frequency. Thus the output voltage becomes slightly distorted. This makes the load current unsymmetrical, and increase the harmonic contents. The fundamental value of load current lags the fundamental value of load voltage because of inductive load. Although, the converter has been tested in the output frequency range of 1 Hz to 850 Hz but it can work for other frequencies also by taking high bit up-down counter.

5. Conclusions

A frequency converter has been proposed using XILINX 9.2i Web Pack software to generate the trigger pulses required for delta PWM technique. Trigger controller has been designed in Xilinx VHDL software and which is dumped in spartan 3e kit. By using the input pin of spartan kit, switching pulses are applied to the power circuit of the converter for obtaining the required output voltage waveforms. Xilinx 9.2i FPGA based controller enables to make easy, fast and flexible design implementation, reconfigurability, immune to noise, power saving options, less external passive components and less sensitive to temperature variation in comparison to analog controller .

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