DESIGN AND PERFORMANCE ANALYSIS OF TG - CMOS FULL ADDER FOR DIGITAL APPLICATIONS

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Abstract: *In this paper, a hybrid Transmission Gate - CMOS logic (TG-CMOS) single bit full adder is proposed. This proposed full adder replaces the six transistor XNOR in the existing adder with two transistors XNOR and also the carry generation path is modified for better power with good voltage swing. The proposed logic is designed as single bit full adder and implemented with a 16 bit ripple carry adder. The design and simulation are done through cadence virtuoso tool with 180nm, 90nm and 45nm technologies. The performance parameters of the proposed design is compared with the existing adder designs. The Performance analysis of the proposed system shows that it consumed less power and operates in high speed. Also the extended version of proposed full adder ie., 16 bit ripple carry adder works effectively.*

Key words: *Hybrid, Cadence, RCA,PDP, High Speed, CMOS*

1. Introduction

Increasing the usage of portable battery devices claims an efficient power, area and speed circuits. Full adder is a sole module in major electronic circuits. Since more researches were gone through this arithmetic blocks [1], [2].

Full adders were analyzed using various logic techniques in past research and evaluated its own merits and demerits [3]-[11]. Other improvised design is Mirror adder [4]. It almost had the same transistor count and power consumption but the maximum propagation delay.

It was a simple design compared to CMOS logic. Other part complementary pass transistor logic gives efficient voltage swing with 32 transistors [5], [6]. But this logic is not a good option for low power applications. Due to the high switching activity, high transistor count, overloading of the inputs and static inverters are the drawback of this technique. Voltage degradation is the important disadvantage of CPL which is analyzed using TGA with only 20 transistors in full adder design [7], [8].

In Static CMOS [3], Dynamic CMOS [4], CPL Logic [5], [6], TGA [7], [8] the various logic designs were analyzed. To improve the performance of the adder hybrid logic was used [9]. Delay and high power consumption are the other demerits of CPL logic. Then research has been focused on hybrid logic styles to improvise the performance of the adder. Vesterbacka [10] proposed 14 T Full adder design. In same Zhang et al [11] presented a hybrid pass and static CMOS logic (HSPC). Partha Bhattacharya et al [26] adders are giving promising performance.

2. TG-CMOS Full Adder design

Fig. 1. shows the TG-CMOS full adder design. The TG-CMOS Full Adder design is to reduce the power consumption and area of the full adder circuit

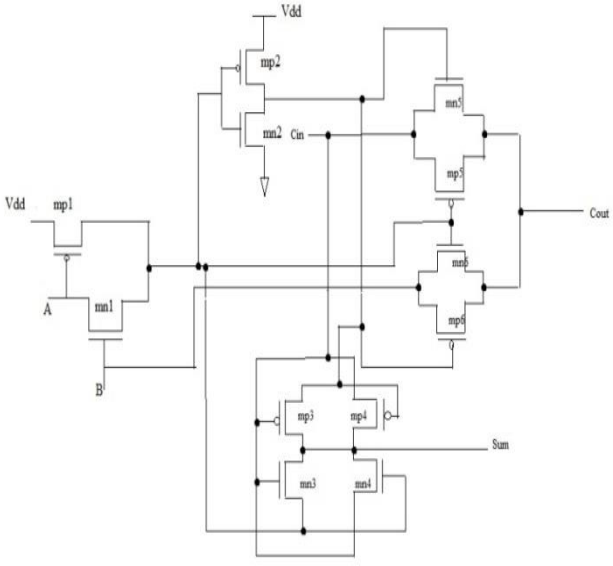

Fig. 1. TG-CMOS Full Adder Design

In full adder circuit, XNOR circuit. XNOR is a very important module in every full adder design but it consumes the large amount of power. Different types of XNOR/XOR circuit designs were executed and the results were compared reported in [7] and [12] – [14].

The existing adder design consist of two XNOR module with six transistors each and the carry propagation module. In this paper the six transistor XNOR is replaced with two transistors design for better power with good voltage swing. The output carry signal is implemented by the transistors M_{p5}, M_{p6}, M_{n5}, and Mn_6.

3. Performance Analysis of the TG-CMOS Full Adder

The performance of the TG-CMOS full adder has been simulated using180nm, 90nm and 45nm technology and compared with the existing design from [1] – [11] and also the special hybrid designs from [1], [2] and [19].

4. Result and Discussion

In this section the simulated and compared output results of the TG-CMOS full adder discussed.

Table I - III reflects the power, Delay and Power Delay Product of the multiple types of single bit full adder design with 180nm, 90nm and 45nm technology using cadence Virtuoso tools. The transistor count also calculated for these variety designs.

From this table we can clearly understand that our proposed design is efficient in terms of power and delay and its products also. In this table some of the design output parameter values are not able to calculate due to the different types of transistor.

Especially the 10T full adder design were all not simulated using 90nm and 180nm technology because in that design they using only NMOS Transistors so their threshold voltage were very much lower in these technologies

comparing the delay parameter this paper proposed design was good but the existing full adder design also have very good speed comparatively our proposed model.

Like wise the transistor count also good comparatively other designs. The lower transistor count is received by 10T full adder design.

The power delay product also good comparative to other designs. From this comparison table the efficiency of the proposed design is reflects.

Table I - Adders parameters comparison in 180nm with 1.8v

Design	Average Power in µW	Delay in ps	PDP in fJ
24 T	15.91	314.2	4.998
FA_ Hybrid	5.978	252.3	1.508
C-CMOS2	6.2199	292.1	1.8168
CPL	7.7198	183.97	1.4202
TGA	8.4719	293.9	2.8989
14 T	12.7217	381.7	4.8558
HSPC	6.3798	273.7	1.74615
Mirror	6.0797	281.61	1.7121
FA_DPL	19.56	226.6	4.432
FA_SR_DPL	20.78	220.65	4.585
TFA	8.2491	287.1	2.3686
Majority Based	6.3227	185.4	1.7222
10 T	14.3449	132.59	1.9020
16T_ Hybrid	4.156	224	0.932
TG-CMOS FA	2.529	212	0.537

Table II - Adders parameters comparison in 90nm with 1.2v

Design	Average Power in µW	Delay in ns	PDP in fJ
24 T	7.707	0.1406	1.0836
FA_ Hybrid	6.21	0.143	0.888
C-CMOS2	1.5799	0.1269	0.200489
CPL	1.7598	0.0791	0.1392
TGA	1.7619	0.2317	0.40823
14 T	3.3297	0.3389	1.1284
HSPC	1.56	0.2207	0.34429
Mirror	1.1507	0.1226	0.19249
FA_DPL	7.34	0.254	1.864
FA_SR_DPL	7.4	0.167	1.235
TFA	1.7363	0.3198	0.55526
Majority Based	1.5751	0.0939	0.1479
10 T	---	----	----
16T_ Hybrid	1.17664	0.0913	0.10742
TG-CMOS FA	0.4883	0.0456	0.0224

Table III - Adders parameters comparison in 45nm with 0.6v

Design	Average Power in µW	Delay in ns	PDP in fJ
24 T	3.8535	0.0703	0.2709
FA_ Hybrid	3.105	0.0715	0.0224
C-CMOS2	0.78995	0.06345	0.8524
CPL	0.8799	0.0395	0.0348
TGA	0.88095	0.11585	0.1034
14 T	1.66485	0.1694	0.2820
HSPC	0.78	0.1103	0.0860
Mirror	0.57535	0.0613	0.0354
FA_DPL	3.67	0.127	0.4671
FA_SR_DPL	3.7	0.0835	0.3089
TFA	0.86815	0.1599	0.1389
Majority Based	0.78755	0.04698	0.0369
10 T	----	----	----
16T_ Hybrid	0.58832	0.0456	0.0268
TG-CMOS FA	0.24415	0.0228	0.0149

Table IV - Adders Transistor count

Design	No of Transistors
24 T	24
FA_ Hybrid	24
C-CMOS2	28
CPL	32
TGA	20
14 T	14
HSPC	22
Mirror	28
FA_DPL	22
FA_SR_DPL	20
TFA	16
Majority Based	--
10 T	10
16T_ Hybrid	16
TG-CMOS FA	12

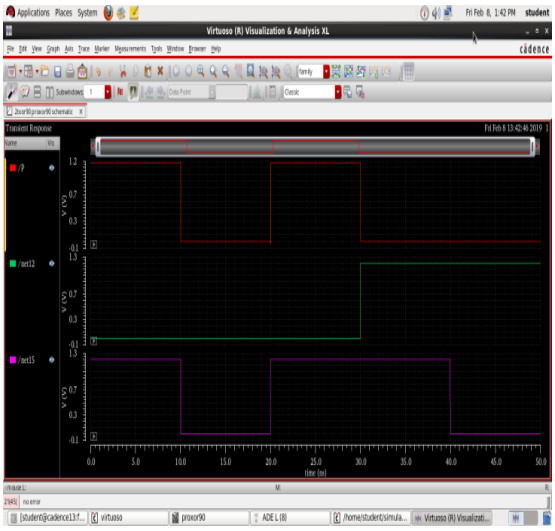

Fig. 2. 1 Simulation output of XOR Gate

The Fig 2.1 shows the output of the two input XOR Gate. This design is simulated using Cadence Virtuoso tools using 180nm, 90nm and 45nm technology. XOR gate is on when two inputs of the gate is different. It is in off condition when two of its input is same.

Fig. 2. 2 Simulation output of Full Adder

The Fig 2.2 reflects the output of the Single bit Full Adder Design. This design is simulated using Cadence Virtuoso tools using 45nm, 90nm and 180nm technology.

Single bit full adder generates carry signal when three of its input signals are maximum. it will not generate the carry signal otherwise.

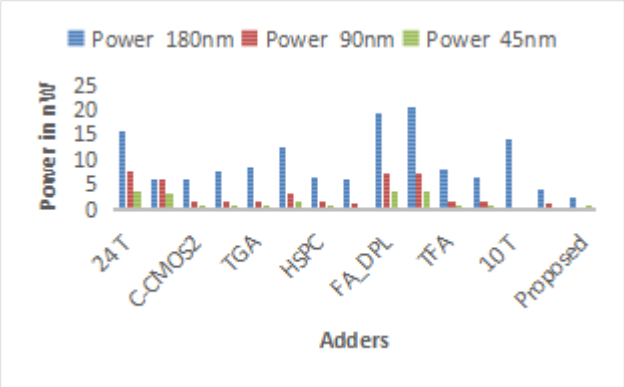

Fig. 2. 3 Power comparison of the full adder using 45nm,90nm and 180nm technology.

The above graph shows the power analysis of the full adder in different design techniques using 45nm, 90nm and 180nm technologies. From this analysis graph, clearly explains the power consumption of the proposed full adder comparatively better with the existing adder designs.

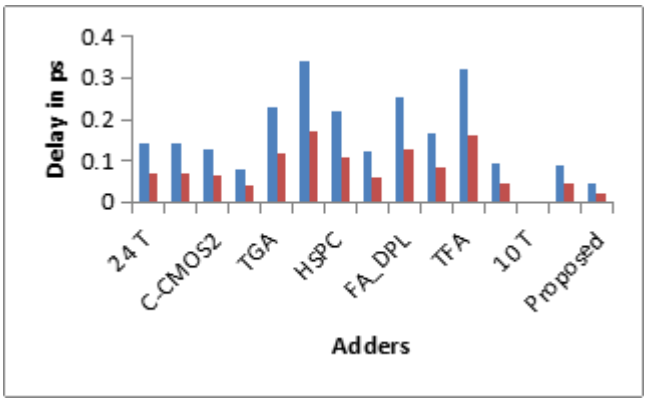

Fig. 2..4 Delay comparison of the full adder using 45nm and 90nm technology.

The above graph shows the delay analysis of the full adder in different design techniques using 45nm and 90nm technologies. From this analysis graph, shows the speed of the proposed full adder comparatively good with the existing adder designs.

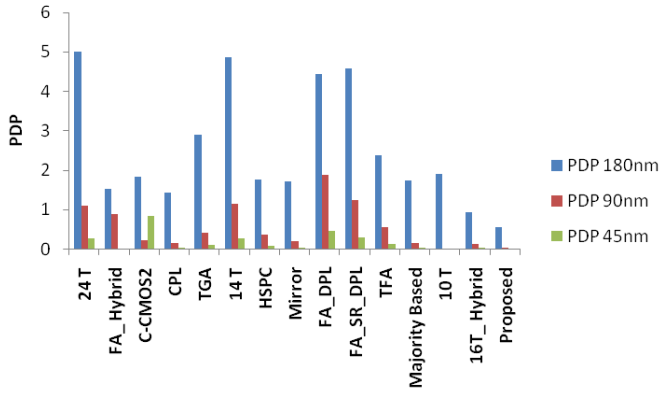

Fig. 2. 5 PDP comparison of the full adder using 45nm,90nm and 180nm technology.

The above graph shows the PDP analysis of the full adder in different design techniques using 45nm, 90nm and 180nm technologies. From this analysis graph, clears that the power Delay Product of the proposed full adder is efficient

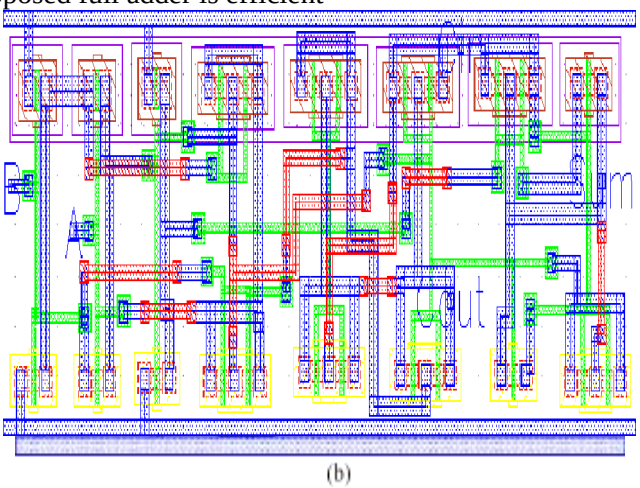

Fig. 2. 6 Layout of full adder with 180 nm and 90nm

From the analysis of Table I & Fig 2 we concluded that the area in 180nm is 68.62µm^2 and the area in 90- and 45nm are 34.31µm^2 and 17.15 µm^2 respectively. When compared with the 10T [24] full adder, the proposed design is consumed 34.5% more area. But the main objective of the proposed design is reducing the PDP.

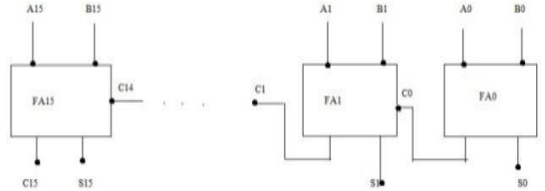

Fig. 3. 16-bit ripple carry full adder with TG-CMOS full adder

To the extension of TG-CMOS single bit full adder, 16 bit Ripple Carry Adder had been designed and simulated using 180nm, 90nm and 45nm. From that concluded that TG-CMOS full adder is working efficiently when increase the bits of an adder also.

5. Conclusion

A hybrid TG-CMOS full adder design is proposed. The logic is designed as single bit full adder and implemented with a 16 bit ripple carry adder.

The design and simulation are done through cadence virtuoso tool with 180nm, 90nm and 45nm technologies. The performance parameters such as power consumption, Delay and PDP of the proposed adder are compared with the existing adder designs.

The power consumption and the delay of proposed adder is 2.529µW, 0.324µW, 0.2441nW and 214ps, .0713ns, 0.0228ns corresponding to 180nm, 90nm and 45nm respectively.

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