MODELING AND SIMULATION OF TRANSISTOR MOSFET (HIGH-K) USING NEURAL NETWORK.

[1]Abdelkrim MOSTEFAI **[2]Smail BERRAH**
[1]Applied Materials Laboratory, University of Sidi Bel Abbes, 22000- Sidi Bel Abbes, Algeria, mostakrimo@yahoo.fr.
[2]LMER Laboratory, University of A/ Mira of Bejaia, Algeria, sm_berrah@yahoo.fr.

[3]Hamza ABID
[3]Applied Materials Laboratory, University of Sidi Bel Abbes, 22000- Sidi Bel Abbes, Algeria, abid_hamza@yahoo.fr.

Abstract: *Smart tools are increasingly used in the design, modeling and control of complex systems, in this paper; we present the results of the characterization and modeling of the electrical current-voltage of the MOSFET (HfO_2 dielectric oxide), using neural network.*

Key words: *Microelectronic, MOSFET, CMOS technology, high-k dielectric, artificial intelligence, neural network.*

1. Introduction.

The reduction of the MOS transistors dimensions is accompanied by the reduction of the gate oxide thickness. In this context, one solution is to replace SiO_2 as a gate dielectric by high-dielectric constant (high–k) materials (for example HfO_2 oxide [1,2]) to reduce leakage currents.

Assuming that the MOSFET strongly submicron is a complex electronic device, electrical and physical phenomena (degradation, the effect of miniaturization, quantum effect, ...) Nonlinear, presenting difficulties of its study and its modeling, it can be studied using statistical methods in the field of artificial intelligence.

The paper addresses a simple and fast approach to implement Artificial Neural Networks (ANN) models for the MOS transistor (HfO_2 dielectric oxide) into MATLAB.

2. Continuous model 'EKV MODEL'

The operation of a MOSFET can be separated into three different modes:

When $V_{GS} < V_T$ where V_T is the threshold voltage of the device, the transistor is turned off, and there is no conduction between drain and source ($I_D \approx 0$).

When $V_{GS} > V_T$ and $V_{DS} \leq V_{GS} - V_T$. The transistor is turned on; the current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1)$$

Or

$$I_D = k_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (2)$$

$$k_n = \frac{\mu_n \varepsilon \varepsilon_{ox}}{2t_{ox}} \frac{W}{L} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \quad (3)$$

When $V_{GS} > V_T$ and $V_{DS} \geq V_{GS} - V_T$. The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. When the device is in saturation the drain current is given by:

$$I_D = k_n(V_{GS} - V_T)^2 \quad (4)$$

When $V_{DS} = V_{GS} - V_T$

Into either Equation (2) or (4), so we get:

$$I_D = k_n {V_{DS}}^2 \quad (5)$$

The fig.1 presents the log $I_D - V_{GS}$ characteristics of a standard MOSFET.

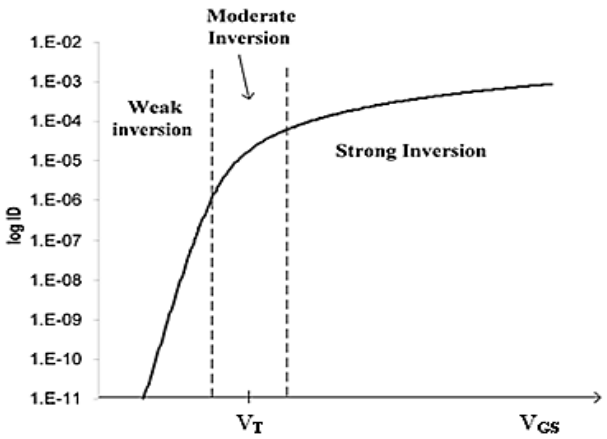

Fig.1. Discontinuity of the $I_{DS}(V_{GS})$ characteristics at $V_{GS} \cong V_T$.

In some cases, such as for the simulation of analog circuit, it is necessary to have a model which is continuous in all regime of operation (weak or strong inversion). In 1995, Enz, Krummenacher and Vittoz proposed a relatively simple MOSFET model

valid in all regions of operation: weak, moderate, and strong inversion. This has come to be known as the EKV model [3].

Their basic equation for drain current (in saturation) is given by [4,5] :

$$I_D = I_F - I_R \tag{6}$$

$$I_D = 2n\mu_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2\left[\left\{ln\left[1 + exp\left(\frac{V_P - V_S}{2KT/q}\right)\right]\right\}^2 - \left\{ln\left[1 + exp\left(\frac{V_P - V_{DS}}{2KT/q}\right)\right]\right\}^2\right] \tag{7}$$

$$V_P = \frac{(V_{GS} - V_T)}{n} \tag{8}$$

On the other hand, $V_S = 0$, $V_{DS} < V_P$ and $V_{GS} > V_T$ (*i.e.* the transistor is operating in the non-saturated regime). In that case the exponential terms are much larger than unity, and one can write:

$$I_D = 2n\mu_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2\left[\left(\frac{V_P}{\frac{2KT}{q}}\right)^2 - \left(\frac{V_P - V_{DS}}{\frac{2KT}{q}}\right)^2\right] \tag{9}$$

$$I_D = \frac{1}{2}n\mu_n C_{ox}\frac{W}{L}[2V_{DS}V_P - V_{DS}^2] \tag{10}$$

$$I_D = \frac{1}{2}n\mu_n C_{ox}\frac{W}{L}\left[2\frac{(V_{GS} - V_T)V_{DS}}{n} - V_{DS}^2\right] \tag{11}$$

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}nV_{DS}^2\right] \tag{12}$$

3. Equivalent oxide thickness.

The miniaturization of the transistors results in the decrease of the gate length. The capacitive coupling between the gate and the substrate must increase or remain constant. Therefore, to maintain these properties, the gate oxide thickness t_{ox} is reduced [6], but when the thickness decreases below a certain value [7,8], several problems arise [1-9]. To resolve this problem, one should consider replacing the gate dielectric (currently SiO_2) by a higher permittivity dielectric (for example HfO_2), one can then increase the thickness and thereby reduce the gate current, while keeping a high C_{ox}. Then introduce the notion equivalent oxide thickness (EOT):

- High-k monolayer

$$C_{SiO_2} = C_{High-k} \Leftrightarrow \frac{\varepsilon_{SiO_2}}{t_{SiO_2}} = \frac{\varepsilon_{High-k}}{t_{High-k}} \tag{13}$$

$$\Rightarrow t_{SiO_2} = EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{High-k}}\, t_{High-k} \tag{14}$$

- High-k multilayer

$$EOT = \frac{\varepsilon_{ox}}{\varepsilon_{High-k}} t_{High-k} + \frac{\varepsilon_{ox}}{\varepsilon_{SiO2}} t_{SiO2} \tag{15}$$

$$C_{tot} = \frac{\varepsilon_{ox}\varepsilon_0}{EOT} \tag{16}$$

The fig.2 presents the Comparison of leakage current density as a function of the equivalent oxide thickness between HfO_2 and SiO_2.

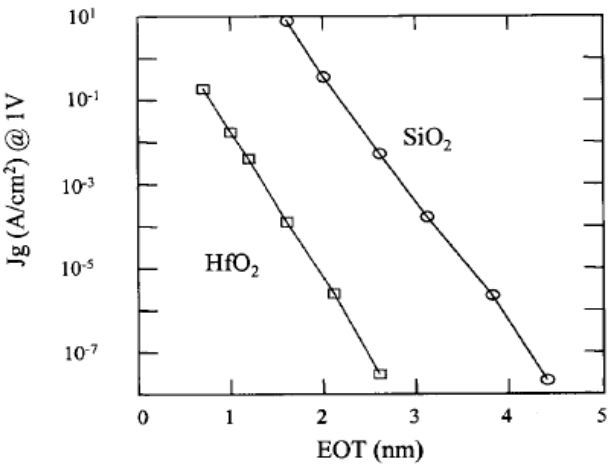

Fig.2. Comparison of leakage current density as a function of the equivalent oxide thickness between HfO_2 and SiO_2. According to Lee et al [10].

The fig.3 presents the Illustration of the integration of dielectric high-k in a MOSFET structure.

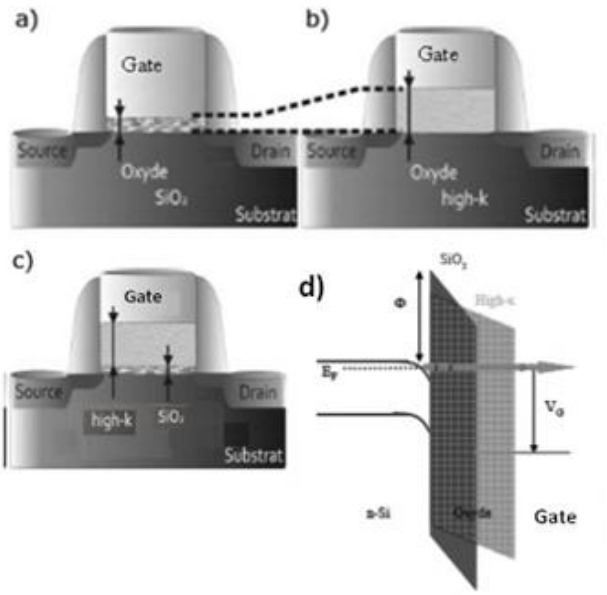

Fig.3. Illustration of the integration of dielectric high-k in a MOSFET structure, a) Reference Oxide SiO_2; b) Integration of a high-k oxide; c) Real structure; d) This difference in thickness allows limiting leakage currents by tunnel effect through the gate.

4. Neural network.

Multilayer Perceptron (MLP) is the most used neural network model. MLP utilizes a learning algorithm (backpropagation) for training the network [11], MLP are capable to separate data that are not linearly separable [12]. The MLP structure is shown in Fig. 4.

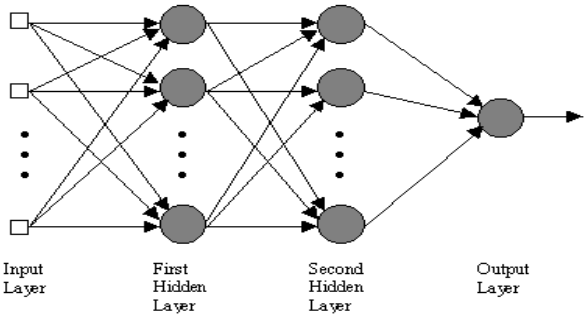

Fig.4. The neural network.

5. Neural network transistor model.

The neural network designed to connect the input vector (Vd, Vg, t_{ox} and L) for MOSFET (HfO_2 monolayer) (Fig. 5-a) and (Vd, Vg, t_{ox}, t_{SiO2} and L) for MOSFET (HfO_2/SiO_2 multilayer) (Fig. 5-b) to output vector Id. Each of these parameters is indexed by a neuron (Fig. 5). The output activation function is the linear function, for hidden layers we choose the sigmoid function (logsig). To enhance learning, we modified different parameters such as the number of neurons in the hidden layer.

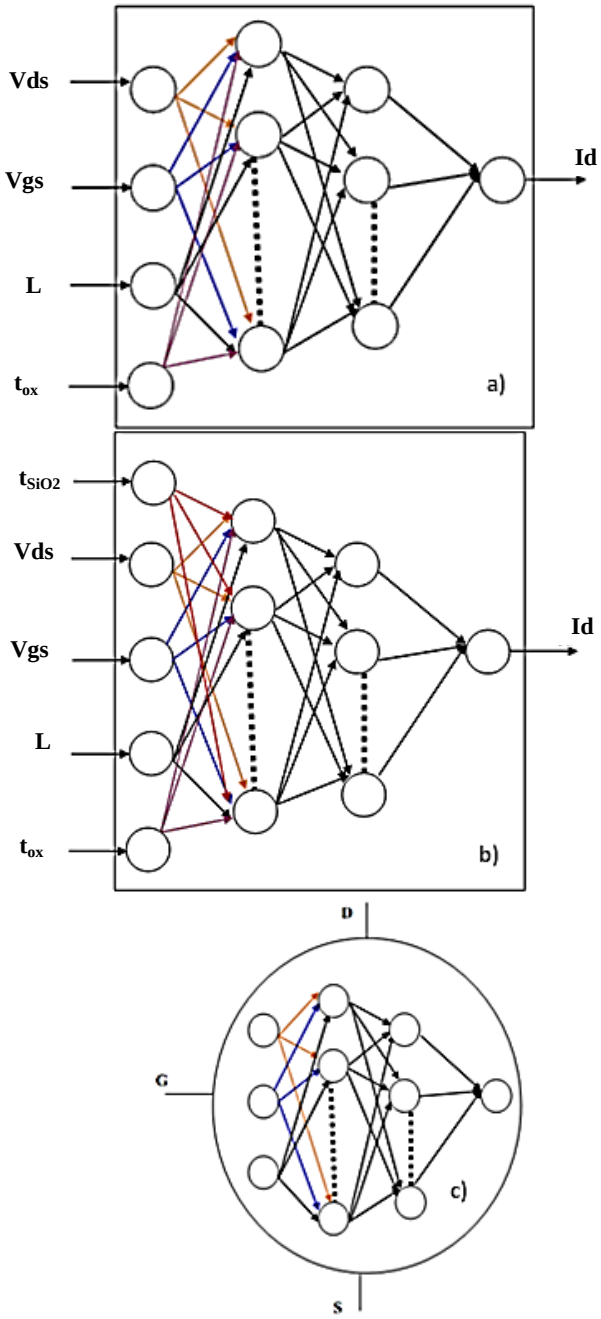

Fig.5. The neuronal model and symbol of transistor MOSFET.

Number of neuron of the first hidden layer: 10
Number of neuron of the second hidden layer: 8

Table 1 summarizes the characteristics of the network optimized of the MOSFET.

Table1

Characteristic of the network optimized.

Propriety	**Characteristic**
Structure	10-8-1 MLP
Function of activation	Logsig-Logsig-linear
Learning rule	back propagation
EQM of test	0.0001
Itération	4000

The program of learning is launched. One observes then at the same times the evolution of the error to each epoch (cycle of learning), then the function obtained by the network, the evolution of the average error of learning is shown in Fig. 6.

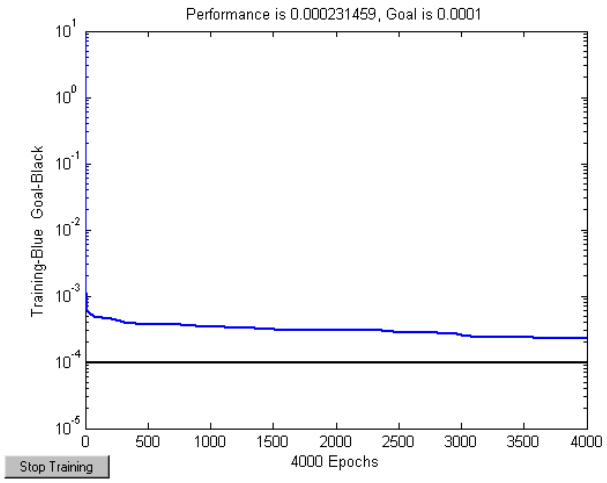

Fig.6. Evolution of the average error of learning.

6. Results and discussion.

Figures 7,8,9 and 10 show a comparison between the results predicted by the neuronal model (ANN) of different characteristics I-V (I_D-V_D and I_G-V_G) with those calculated by the analytical model for a transistor MOSFET (monolayer HfO_2) low doped with L=0.1µm, t_{ox}=14 nm (monoclinic HfO_2, EOT=3 nm) and t_{ox}=22 nm (tetragonal HfO_2, EOT=3 nm).

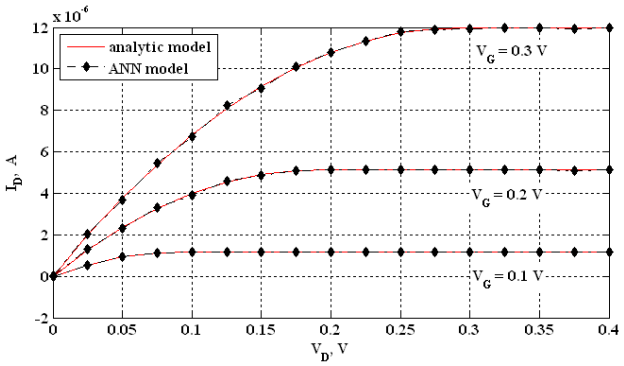

Fig.7. I_D (V_D) Characteristic of the MOSFET high-k monolayer HfO_2 (monoclinic-HfO_2 oxide).

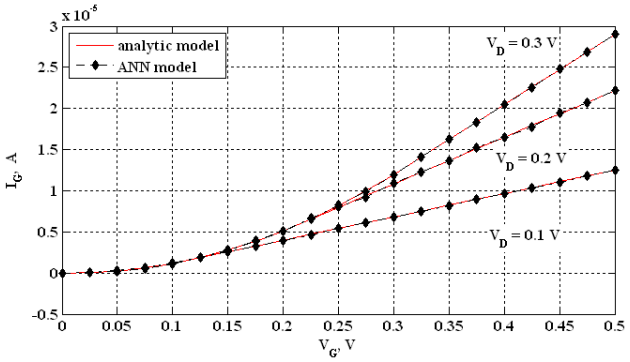

Fig.8. I_G (V_G) Characteristic of the MOSFET high-k monolayer HfO_2 (monoclinic-HfO_2 oxide).

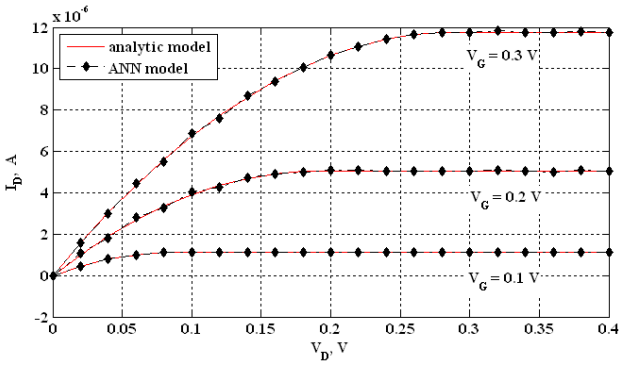

Fig.9. I_D (V_D) Characteristic of the MOSFET high-k monolayer HfO_2 (tetragonal-HfO_2 oxide).

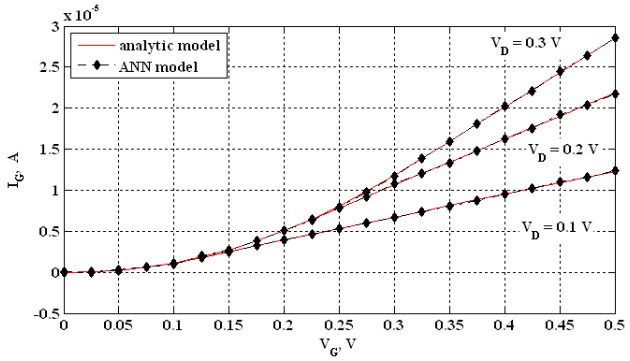

Fig.10. I_G (V_G) Characteristic of the MOSFET high-k monolayer HfO_2 (tetragonal -HfO_2 oxide).

Figures 11,12,13 and 14 show a comparison between the results predicted by the neuronal model (ANN) of different characteristics I-V (I_D-V_D and I_G-V_G) with those calculated by the analytical model for a transistor MOSFET (multilayer HfO_2/SiO_2) low doped with L=0.1 µm, t_{sio2}=1 nm, t_{ox}=9 nm (monoclinic HfO_2, EOT=3 nm) and t_{ox}=15 nm (tetragonal HfO_2, EOT=3 nm).

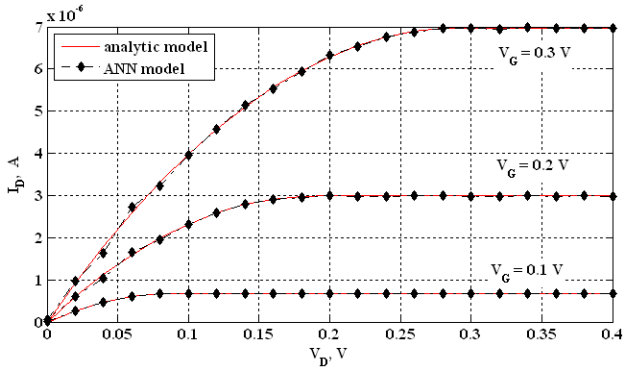

Fig.11. I_D (V_D) Characteristic of the MOSFET high-k multilayer HfO_2/SiO_2 (monoclinic-HfO_2 oxide).

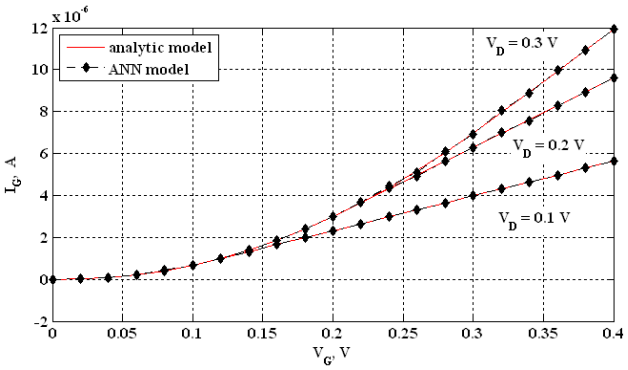

Fig.12. I_G (V_G) Characteristic of the MOSFET high-k multilayer HfO_2/SiO_2 (monoclinic-HfO_2 oxide).

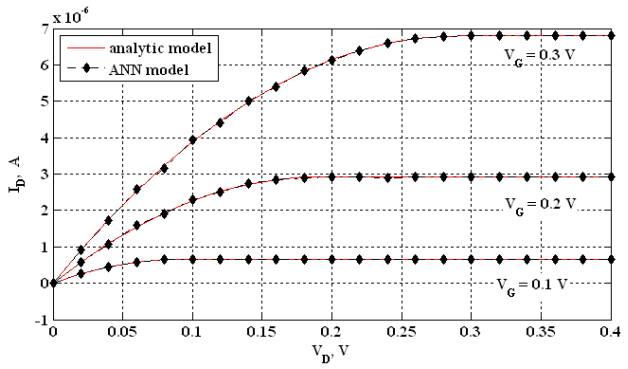

Fig.13. I_D (V_D) Characteristic of the MOSFET high-k multilayer HfO_2/SiO_2 (tetragonal-HfO_2 oxide).

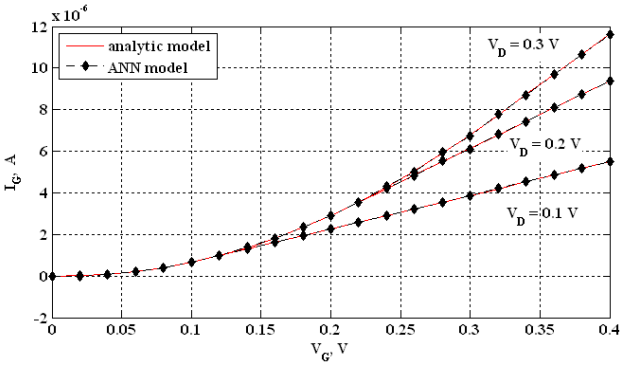

Fig.14. I_G (V_G) Characteristic of the MOSFET high-k multilayer HfO_2/SiO_2 (tetragonal-HfO_2 oxide).

I(V) characteristic of the MOSFET high-k (Fig.7, Fig.8) (monolayer HfO_2, monoclinic-HfO_2 oxide) and I(V) characteristic of the MOSFET high-k (Fig.9, Fig.10) (monolayer HfO_2, tetragonal-HfO_2 oxide) have the same results but with different thickness ($t_{monoclinic\text{-}HfO2}$ = 14 nm, $t_{tetragonal\text{-}HfO2}$ = 22 nm).

I(V) characteristic of the MOSFET high-k (Fig.11, Fig.12) (multilayer SiO_2/HfO_2, monoclinic-HfO_2 oxide) and I(V) characteristic of the MOSFET high-k (Fig.13, Fig.14) (multilayer SiO_2/HfO_2, tetragonal-HfO_2 oxide) have the same results but with different thickness ($t_{monoclinic\text{-}HfO2}$ = 9 nm, $t_{tetragonal\text{-}HfO2}$ = 15 nm).

From the results obtained (Fig.7, Fig.8, Fig.9, Fig.10, Fig.11, Fig.12, Fig.13 and Fig.14), HfO_2 is good candidate to replace SiO_2.

I(V) characteristic simulated by the analytical model is compared with the neural model. It can be observed that good agreement between the analytical and neural data was obtained by both of the models.

The differences between the results of monoclinic and tetragonal-HfO_2 is:

1- Thickness of tetragonal-HfO_2 is wider than Thickness of monoclinic-HfO_2 (The monoclinic-HfO_2 has a smaller dielectric constant than the tetragonal-HfO_2).

2- The tetragonal-HfO_2 is more stable than the monoclinic-HfO_2.

Table 2 summarizes the percentage error between analytical model and ANN model in different cases.

Table2
Percentage error between analytical model and ANN model in different cases.

Different cases of oxide	Percentage error %
monolayer HfO_2, monoclinic-HfO_2	1.37 %
monolayer HfO_2, tetragonal-HfO_2	1.2 %
multilayer SiO_2/HfO_2, monoclinic-HfO_2	2.11 %
multilayer SiO_2/HfO_2, tetragonal-HfO_2	2.24 %

Our objective here is to implement neural network programs in Matlab, using the backpropagation to identify different curves (characteristic I (V) of the MOSFET, the evolution of the average learning error of our predictor). This model can be used to simulate the MOSFET response to different parameters related to the manufacturing technology.

The great advantage of neural networks lies in their automatic learning capability, which allows solving problems without requiring writing complex rules. The results in this work, in good agreement with previous results, [13,14,15,16,17,18]. This last observation shows the applicability of the networks of artificial neurons being studied of nanometric circuits CMOS.

7. Conclusion.

This paper showed the applicability of the neuronal approach to the problem of prediction of the lifespan of the strongly submicron integrated devices. An analytical approach based on a neuronal predictor was developed in the case of transistor MOSFET has high permittivity (HfO_2). The latter enabled us to envisage the evolution of the current according to the different parameters (drain voltage, gate voltage, channel length and oxide thickness).

8. Reference.

[1] Wilk, G.D., Wallace, R.M., Anthony, J.M. "High-k gate dielectrics: current status and materials properties considerations", Journal Applied Physics, vol. 89, n°10, pp.5243-5275, 2001.

[2] Robertson, J. "High dielectric constant oxides", European Physical Journal Applied Physics, vol. 28, pp.265-291, 2004.

[3] Colinge, J.P., Colinge, C.A. "Physics of Semiconductor Devices", Springer Science - Business Media, New York, NY, USA, 2002.

[4] Enz, C.C. "The EKV model: a MOST model dedicated to low-current and low voltage analogue circuit design and simulation". In: Machado, G.A.S (Ed.). "Low-Power HF Microelectronics: A Unified Approach", Institution of Electrical Engineers and Technology, London, 1996, pp.247-300.

[5] Enz, C., Krummenacher, F., Vittoz, E.A. "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low current applications". In: Serdijn, W. (Ed.). "Low-Voltage Low-Power Analog Integrated Circuits", Springer Science-Business Media, New York, 1995, pp.83-114.

[6] Taur, Y."CMOS design near the limit of scaling", Journal of Research and Development, vol. 46, n°2, pp.213-220, 2002.

[7] Green, M.L., Sorsch, T.W., Timp, G.L., Muller, D.A., Weir, B.E., Silverman, P.J., Moccio, S.V., Kim, Y.O. "Understanding the limits of ultrathin SiO_2 and Si-O-N gate dielectrics for sub-50 nm CMOS", Microelectronics Engineering, vol.48, pp.25-30, 1999.

[8] Muller, D.A., Sorsch, T., Moccio, S., Baumann, F.H., Evans-Lutterodt, K., Timp, G. "The electronic structure at the atomic scale of ultrathin gate oxides", Nature 399, pp.758-761, 1999.

[9] Green, M.L., Gusev, E.P., Degraeve, R., Garfunkel, E.L. "Ultrathin (<4 nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits", Journal Applied Physics, vol. 90, pp.2057-2121, 2001.

[10] Lee, B.H., Kang, L., Qi, W.J. , Nieh, R., Jeon, Y., Onishi, K., Lee, J.C. "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application", Technical Digest. IEEE International Electron Devices Meeting (IEDM), pp.133-136, 1999.

[11] Rosenblatt, F. "Principles of Neurodynamics: Perceptrons and the Theory of Brain Mechanisms", Spartan Books, Washington DC, USA, 1961.

[12] Cybenko, G. "Approximation by superpositions of a sigmoidal function", Mathematics of Control Signals & Systeme, vol. 2, n°4, pp.303–314, 1989.

[13] Lindorfer, Ph., Bulucea, C. "Modeling of VLSI MOSFET characteristics using neural networks". In: Selberherr, S., Stippel, H., Strasser, E. (Ed.). "Simulation of Semiconductor Devices and Processes", vol. 5, Springer, New York, 1993, pp.33-37.

[14] Litovski, V.B., Radjenović, J.I., Mrčarica, Ž.M., Milenković, S.Lj. "MOS transistor modeling using neural network", Electronics Letters, vol. 28, n°18, pp.1766 – 1768, 1992.

[15] Hayati, M., Rezaei, A., Seifi, M. "CNT-MOSFET modeling based on artificial neural network: Application to simulation of nanoscale circuits", International Journal Solid-State Electronics, vol. 54, pp.52–57, 2010.

[16] Djeffal, F., abid, M.A., dibi, Z., Chahdi, M., Benhaya, A. "A neural approach to study the scaling capability of the undoped Double-Gate and cylindrical Gate All Around MOSFETs", Materials Science and Engineering B, vol. 147, pp.239-244, 2008, .

[17] Djeffal, F., Dibi, Z., Hafiane, M.L., Arar, D. "Design and simulation of a nanoelectronic DG MOSFET current source using artificial neural networks", Materials Science and Engineering C, vol. 27, pp.1111-1116, 2007.

[18] Avci, M., Babac, M.Y., Yildirim, T. "Neural network based MOSFET channel length and width decision method for analogue integrated circuits", International Journal of Electronics, vol. 92, n°5, pp.281–293, 2005.