

Dynamic Protection of Power Converters Associated with the Grid Using Shunt Active Filter And Thyristor Switched Capacitor for Power Quality Enhancement

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Abstract: The major problems with the high power converters connected to the grid are the increased currents harmonics introduced by switching and the poor power quality. Further, it is essential to identify and recover the system during the fault occurrence. Failure to recover the power converters from the fault will lead to jeopardy and hence is not preferred. A dynamic system is proposed for the fault isolation and the power quality improvement. The proposed system uses shunt active filter (ASF) and Thyristor Switched Capacitor (TSC) to recover the converter from the fault condition. The proposed system is designed, simulated and implemented. The simulations were made with and without faults triggered at desired intervals. The simulated results are further validated with the hardware setup. When the fault is triggered, the output voltage is disrupted by the fault, when the shunt active filter and Thyristor Switched Capacitor (TSC) are inactive. The results validate that the proposed system greatly reduces the currents harmonics and improves the power factor.

Keywords: Power quality, Power converters, Shunt active filter, Thyristor switched capacitor, currents harmonics

1. Introduction

Nowadays, grid framework experiences major issues of currents harmonics and poor power factor due to the increased use of distributed generation and power electronic converters that are being used for loading the system. The power system parameters such as current, voltage and system impedance transferred from the source at any instant play the vital role in addressing the mentioned problems and the impedance monitoring paves the way for active filter control. The calculation of impedance is used for the dynamic operation of power electronic systems connected to the grid such as sine wave rectifiers [1] and active shunt filters (ASF). The measurement of active filter's line current or voltage, at the point of common coupling, provides non-invasive estimation of power system impedance changes, though it's not appropriate enough to provide a proper value for controlling.

The minimal disturbance introduced by a minor change to the PWM method of Power Electronic Equipment (PEE) stimulates the impedance of the power system and the related voltage and current transients that are used to determine more exactly the supply side impedance. When a significant change is observed in the calculated values, the dynamic control is triggered [2].

In the existing power system network, it is evident that line voltage and line current have to be measured for the duration of 160 milli seconds (ms) before transient injection and the equal period to be maintained post-transient to obtain the required frequency resolution for impedance measurement. When Continuous Wavelet Transform (CWT) is applied, the data capturing period is substantially decreased to 5ms post-transient and the pre-transient data requirement is greatly reduced. This significant reduction happens because of the application of CWT. CWT is a method used to process the current and voltage transient for calculating the supply impedance. This method determines changes in the the supply impedance within a half cycle of the supply[3].

The new strategy for real-time impedance estimation is discussed in [4]. The significance of CWT in speeding up the time for impedance estimation is also explained in the paper. The new methodology is experimentally proved with furnished results. The estimation technique to locate faults in a given power zone is also described in this paper. Power system applications in aircraft, ships and transport systems specifically require the ability to precisely identify and locate faults in the power systems [4].

In the proposed method, Shunt active filter and Thyristor Switched Capacitors are used. Shunt active filter has the ability to compensate both current harmonics and power factor for the three-phase power system. Thyristor Switched Capacitor (TSC) is used for reactive power compensation.

2. Power system impedance measurement

The Circuit diagram of power impedance measurement is shown in the Figure.1. The impedance of the power system is obtained by analysing the voltages and currents that are measured after a disturbance is introduced into the source system. The disturbance will be introduced when two consecutive PWM cycles are controlled and the momentary disturbance will be injected into the system. To perform the above operation, PEE is designed with an active filter that is shown in Figure 2. The presence of the filter inductance produces a momentary current spike, of approximately 1m long and 20A peak, injected to PCC. Continuous Wavelet Transform is used to find the voltage and current value by [5-7].

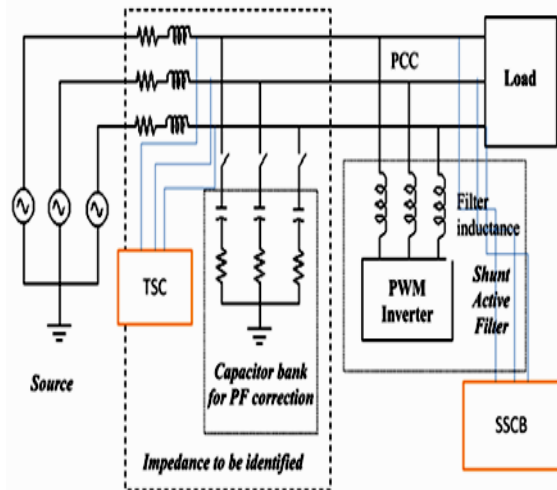


Figure.1 Circuit diagram for power impedance measurement

An interpolation routine determines the impedances at harmonic frequencies and that impedance to source under such frequencies are discarded. An active shunt can be deployed in the stand alone mode with the adequate control of the filter. For the desired frequency range, the window is adjusted in wavelet based transformation method, as opposed to fourier transform. The non stationary signal is analyzed using the signal processing tool CWT. The proposed work uses both voltage and current measurement to find the power system impedance.

3. Shunt active filter

Shunt active filter has the ability to compensate the current harmonics and improve the power factor for the three-phase power system. Moreover, it

balances the load and eliminates the current reversal fault that occurs in the neutral line. Active power filters (APF) provide the most elegant solution to the voltage quality problems.

APF produces the required currents component to cancel the harmonic current components in case of the non linear load. The existing APF systems use PWM based converters to be utilized in the low or medium voltage distribution system, with series or shunt connection. The combination of series and shunt APFs are used to compensate the harmonics. The shunt APF compensates the load current as a controllable current source and the series APF acts as a controllable voltage source. Both schemes are deployed in conjunction with PM inverters, when the DC bus has reactive elements such as a capacitor. APFs can be tuned to the required order for harmonics compensation and power quality improvement.

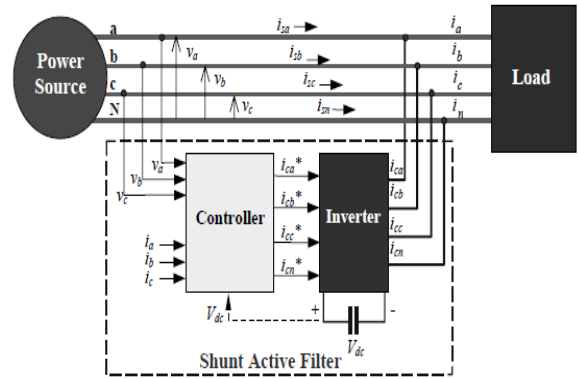


Figure.2 Shunt APF deployed in a 3 ph. power system

Figure.2 shows the circuit for shunt active filter in a three phase power system network along with the neutral line. The principle of active shunt filter is to produce harmonic current equal in magnitude but opposite in phase to those harmonics that is present in grids. Phase shift of harmonic current is 180° [8-9].

The Shunt Active Filter is added in series with the proposed system to reduce the current harmonics and improve the power factor.

4. Thyristor switched capacitor

A Thyristor Switched Capacitor (TSC) system is used to compensate the reactive power in the power systems. A power capacitor is connected in series with the bidirectional thyristor valve as shown in Figure 3. The number of TSC branches in one phase is calculated based on how much reactive power compensation is required. TSC based system

is the simple design and offers numerous advantages in many applications. The benefits include the better compensation of the reactive power and excellent harmonic filtration.

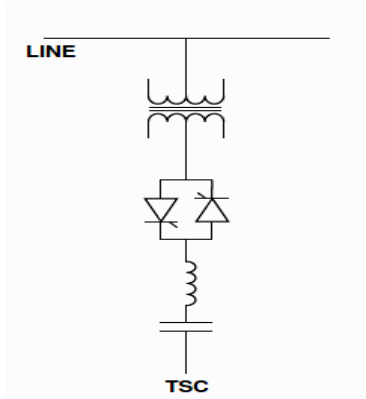


Figure.3 Thyristor switched capacitor

TSC supplies the capacitive reactive power to compensate the reactive power due to industrial loads connected to the supply. TSC is mainly used for the reactive power compensation.

When the line voltage is equal to the voltage across the thyristor, the thyristor pair is switched on. Techniques such as zero-crossing detectors can be used to pre-charge the capacitors before switching for the improved transient response. Many topologies are available for TSC configuration. Some of them are delta connected capacitors, star topology and connection with thyristor-diode combination.

TSCs were historically used for the voltage regulation for the arc suppression. Progressively, TSCs has been applied in variety of applications, including the reactive power compensation systems [10]. In the proposed system, Thyristor switched capacitor (TSC) is connected in parallel for compensating the reactive power.

5. Solid state circuit breaker

A solid state circuit breaker works based on voltage comparator. The comparator compares the voltages supplied on the sources pin. A 1 kW resistor, R_{TH} , mirrors and returns the the current supplied on threshold pin. This in turn sets the tip voltage of the comparator. The internal current latch is set, when a fault occurs. The power field effect Transistor (FET) is turned off by the latch. After the fault is rectified, the control input pin has to be turned low and then to high, before switching on FET.

The purpose of 330kW resistor is to keep the input at low level and keep the FET status in off condition, until the circuit is reset. The benefits of this topology include the simple construction and the cost reduction [11]. Solid State Circuit breaker is used in the proposed system during fault condition and fault isolation condition.

6. Simulation Results

The power system with shunt active filter (ASF) and thyristor switched capacitor (TSC) is modelled and simulated using Matlab as shown in Figure 4. Shunt active filter is used to reduce the harmonics in the alternator. Thyristor switched capacitor is added to improve the voltage and transmission ability of the power system. The sending end voltage is shown in Figure 5.

The switching pulses for M1, M3 and M5 are shown in Figure6. The delta connected Thyristor switched capacitor is shown in Figure7. The voltage and current waveforms at the receiving end are shown in Figure.8 and Figure.9 respectively. The signatures of the real and reactive power components at the load end are shown in Figure.10 and Figure.11 respectively. The spectrum of source current is shown in Figure.12. THD is 5.4% and it is clearly evident that the voltage reaches a normal value due to the addition of TSC.

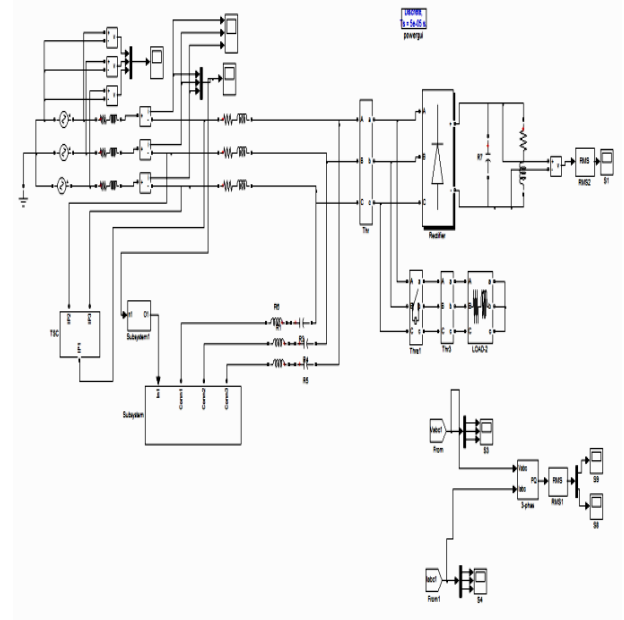


Figure.4 Circuit Model of SAF and TSC

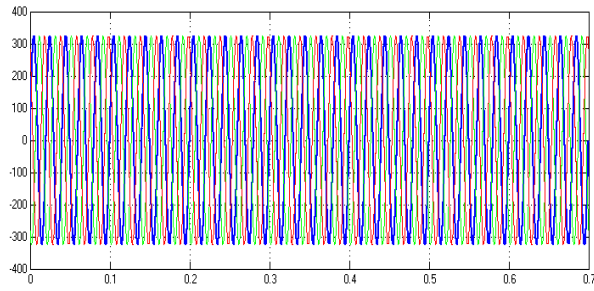


Figure.5 Sending end voltage

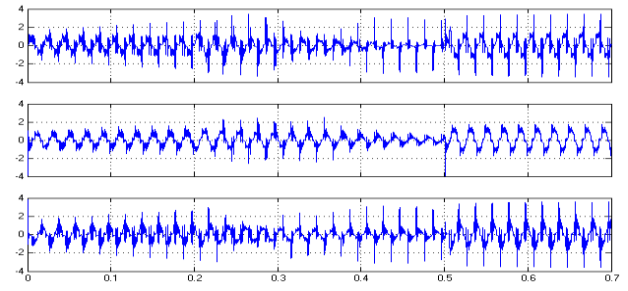


Figure.9 Output current

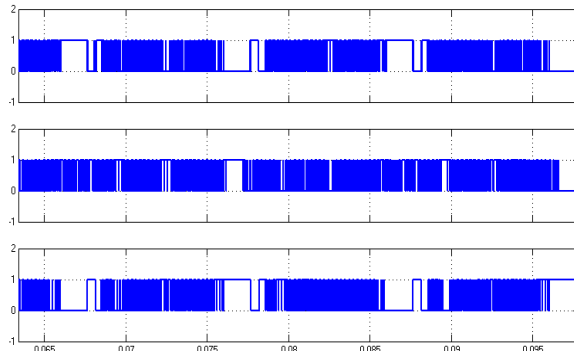


Figure.6 Switching pulse for (M1, M3, M5)

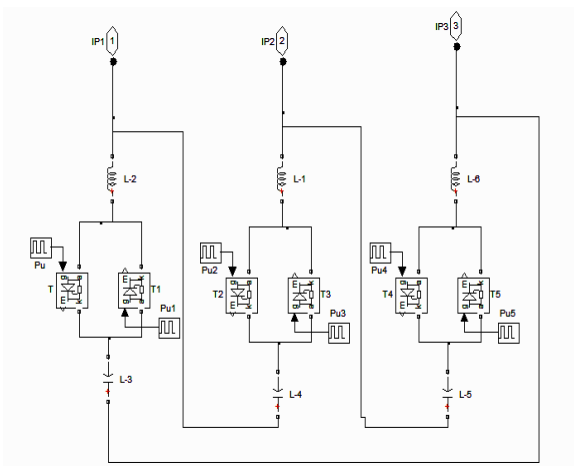


Figure.7 Matlab Model of Delta connected TSC

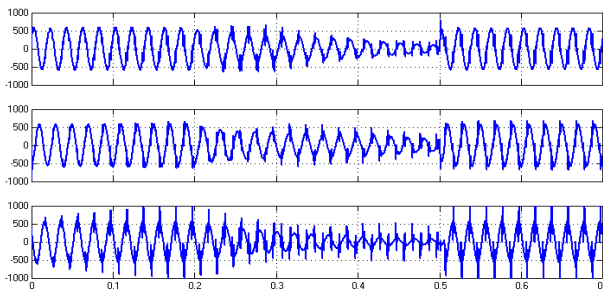


Figure.8 Output voltage

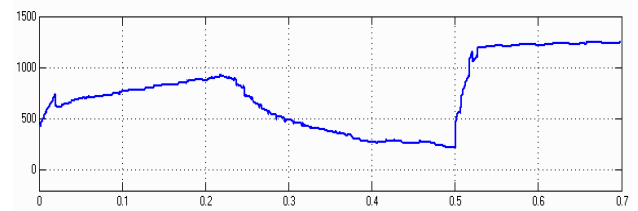


Figure.10.Real power

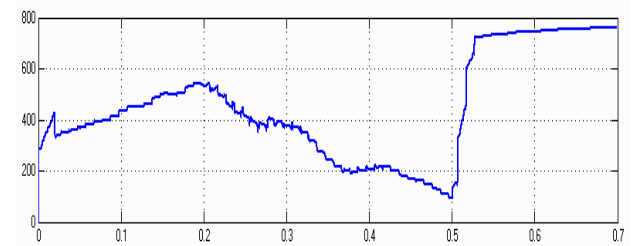


Figure.11.Reactive power

The real and reactive power are shown in the Figure.11 and Figure.12. They are brought to the desired range by introducing Shunt Active Filter and Thyristor Switched Capacitor. The THD level will reduce and to meet the power quality by an ASF as shown in Figure.12.

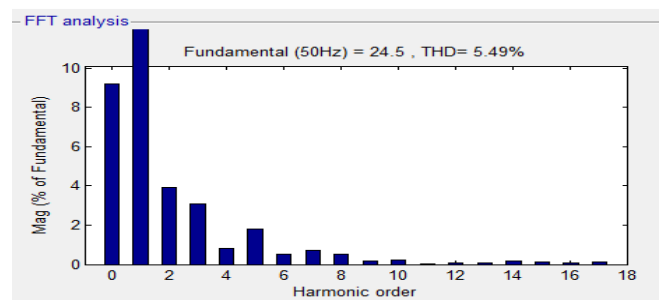


Figure.13.Spectrum for source current

6.1 During fault condition

The Simulink model of two bus systems with a shunt active filter and Thyristor switched capacitor during fault condition is shown in Figure.13. The sending end voltage is shown in Figure.14.

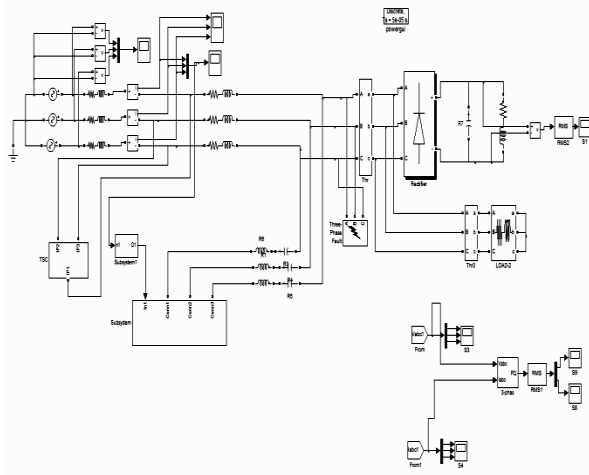


Figure.13. Matlab Model of Two bus systems with SAF and TSC during fault condition

The fault is created at $t=0.3$ Sec. The voltage decreases as shown in Figure.16. The load current decreases since the terminal voltage reduces to zero as shown in Figure.17. The real and reactive power components are shown in Figure.18 and Figure.19 respectively. The decrease is due to the reduction in the voltage

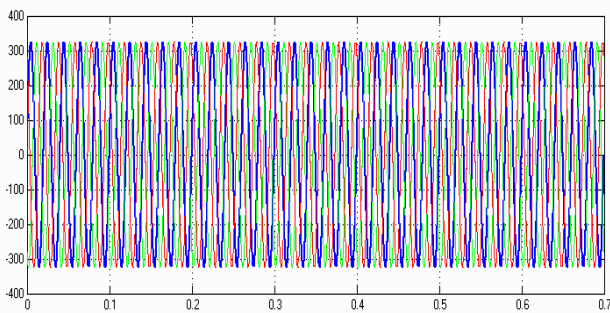


Figure.14. Sending end voltage

Figure.15 and Figure.16, shows in a fault condition, the output voltage and current will start out of distortion and it can be reduced and can get instant clear and by improving the power quality through an ASF and TSC.

Figure.17 and Figure.18 shows that, at fault condition the real and reactive power, performance will be worst and it should be clear by a reducing harmonic and improving the power quality.

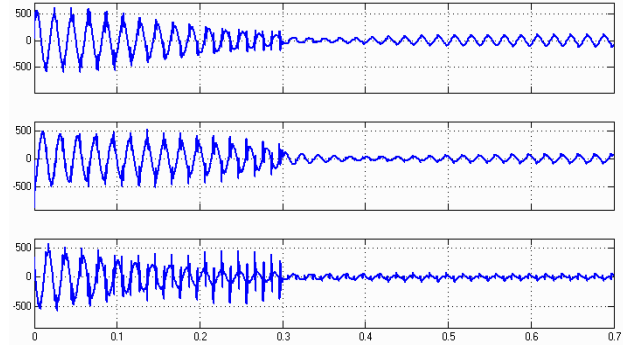


Figure.15. Output voltage with fault triggered at 0.3 Sec

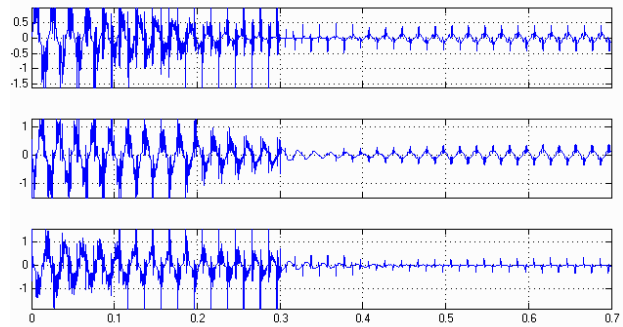


Figure.16. Output current with fault triggered at 0.3 Sec

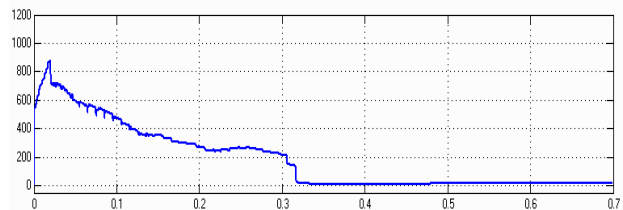


Figure.17. Real power with fault triggered at 0.3 Sec

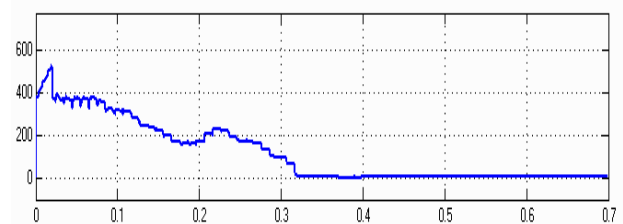


Figure.18. Reactive power with fault triggered at 0.3 Sec

6.2 Fault Isolation condition

The Simulink model with the fault being isolated is shown in Figure19. The fault is isolated using a solid state circuit breaker (SSCB). The sending end voltage is shown in Figure20. The output voltage and current are shown in Figure.21 and Figure.22 respectively. The voltage and current resume to

normal value after the fault. The real and reactive power are shown in Figure.23 and Figure.24 respectively.

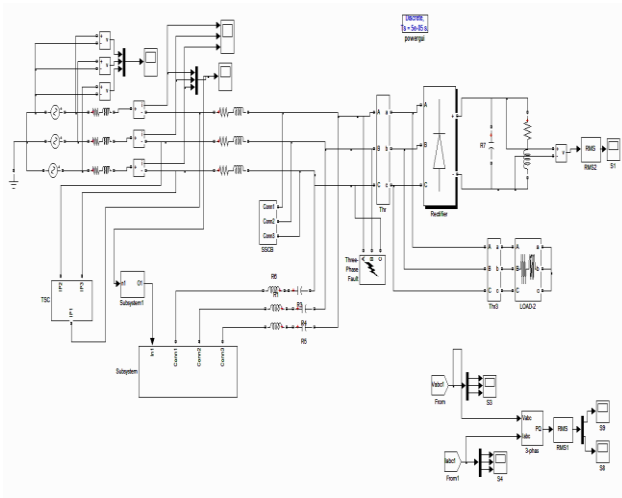


Figure.19.Two bus system with SAF and TSC during fault isolation condition

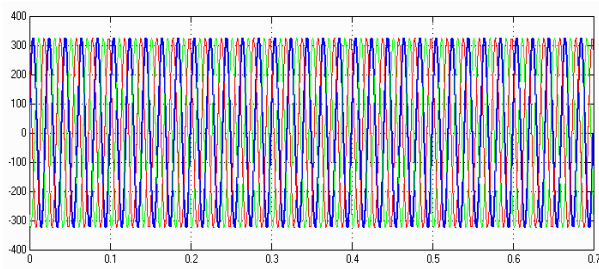


Figure.20.Sending end voltage

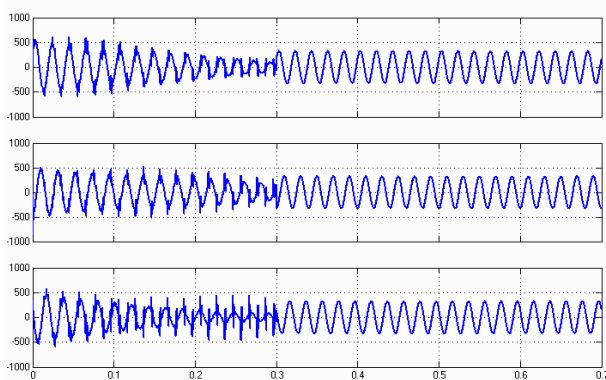


Figure.21. Output voltage with fault isolated at 0.3 Sec

The Figure.21 and Figure.22 shows that the output voltage and current will come out of distortion and reach the stable value after isolating the fault.

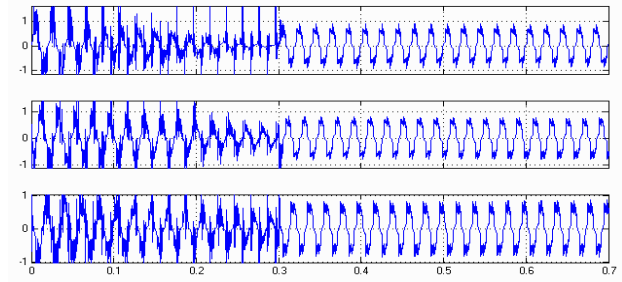


Figure22.Output current with fault isolated at 0.3 Sec

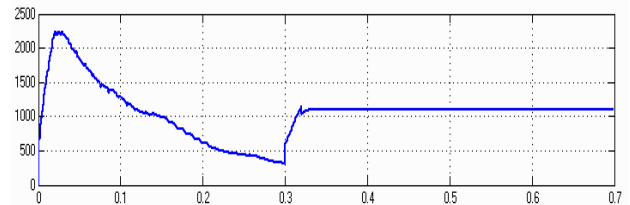


Figure.23 Real power with fault isolated at 0.3 Sec

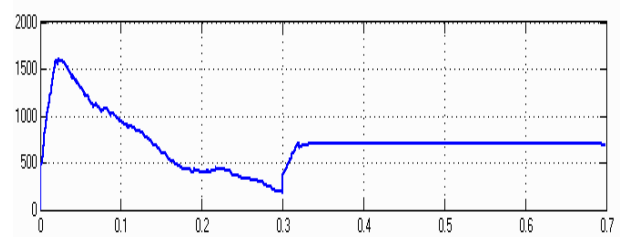


Figure.24. Reactive power with fault isolated at 0.3 Sec

The real and reactive power at isolated condition are shown in Figure.23 and Figure.24. It is clearly projected the real and reactive power will improve by making a fault condition to be isolated. The total harmonic distortion levels are shown in Figure 25.

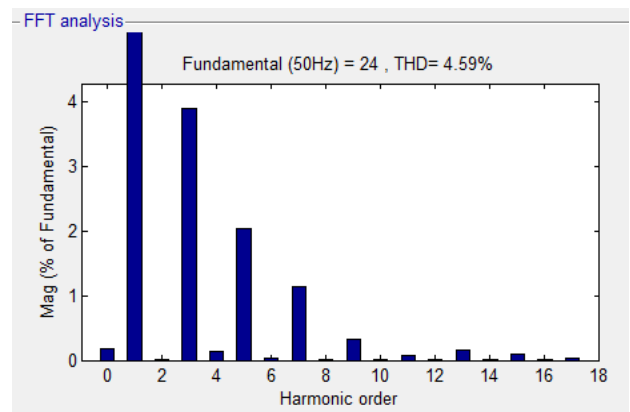


Figure.25.Spectrum for source current

7. Hardware Setup

The Hardware setup for the proposed system is shown in Figure 26. It has two major circuits, namely Control circuit and Power circuit. Control circuits consist of a power supply, PIC IC 16F84A and Driver IC IR2110. PIC IC 16F84A is a 18 pin IC and it is used to control the Circuit. Driver IC IR2110 is a 14 pin IC. It consists of a high pulse current buffer stage which minimizes the driver cross conduction. The driver IC is used to drive the MOSFET (switches). The accuracy is high and it is used to amplify the pulses. In the hardware setup, three way toggle switch is used, in place of SSCB. The switch is used to trigger the fault condition.

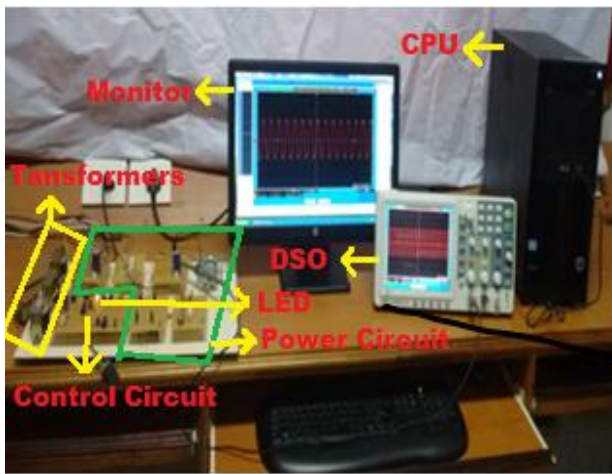


Figure.26. Hardware setup

The other significant circuit in Hardware diagram is power circuit that consists of Rectifier, RL Load, RLC Load, MOSFET (switches). Rectifier converts the AC into DC. RL Load acts as a Load at the output end. The applied voltage determines the active and reactive powers of the load. MOSFET (switches) which is a voltage controlled device is used for controlling the circuit.

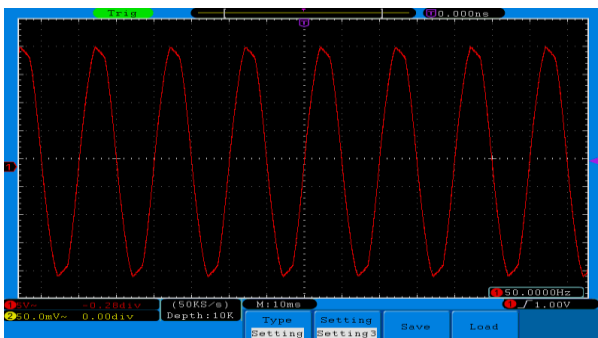


Figure.27. Input Voltage

Figure.27 shows the 230V single Phase Input sinusoidal voltage of a waveform measured at the input end of the rectifier.

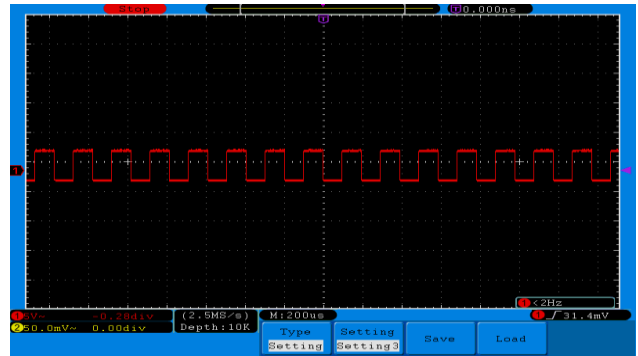


Figure.28. Switching Pulse at 5V

The switching pulse at 5V applied to the MOSFET switches is shown in Figure.28. But this generated 5V pulse can not be applied directly, as the MOSFET switches require the minimum pulse voltage of 10V. The driver IC IR2110 is used to amplify the switching pulse train to the required level.

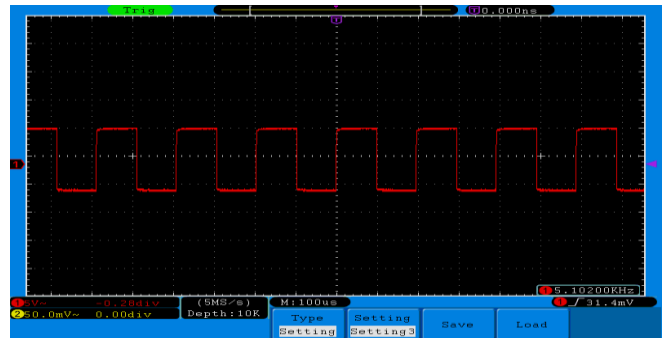


Figure.29. Switching Pulse at 10V

After the amplification by the driver IC to 10V, the regenerated pulse pattern is measured and displayed in Figure.29.

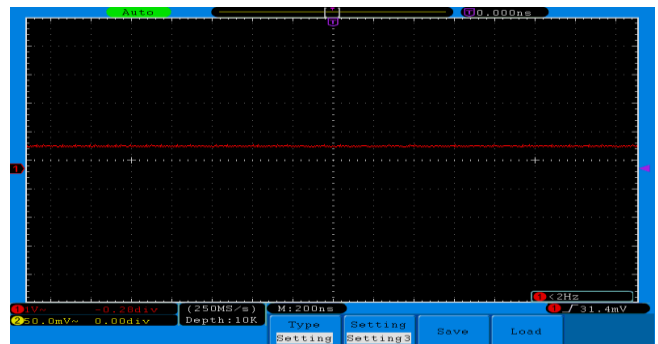


Figure.30. Output Voltage at Fault Condition

When the fault is triggered, the output voltage is measured and displayed in Figure 30. It is clear that the output voltage is disrupted by the fault. This measurement was taken, when the shunt active filter and Thyristor Switched Capacitor (TSC) are inactive.

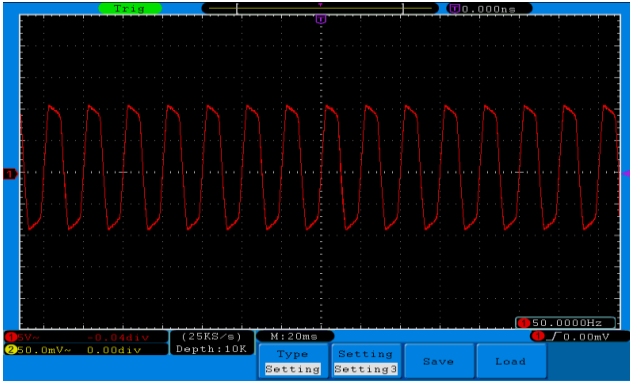


Figure.31. Output Voltage at Fault Isolation Condition

After Shunt Active filter and TSC are applied, the output voltage was regained back, after the fault isolation, as shown in Figure. 31. The voltage level was thus increased to the adequate level to drive the output load. The above observations strongly validate our claim that the proposed system reduces the current harmonics and improves the power factor. Further, the measured results are strongly correlated with the simulated results.

8. Conclusion

Thus dynamic system for power quality improvement and protection of power converters connected to the grid was developed to reduce the currents harmonics and enhance the power factor during fault occurrence. The proposed Two bus systems with shunt active filter and Thyristor switched capacitor were modelled and simulated successfully. The fault condition was triggered at desired duration and the results were examined. The simulated results were further validated with the hardware setup. The results indicate that the proposed system recovers the converter from the fault condition by fault isolation. The improvement in the powerfactor and the reduction in currents harmonics is thus clearly observed due to the proposed system. The use of SAF and TSC help to isolate the fault and regain the output voltage without the interrupt to the load. However, the cost of the power system will increase marginally due to the addition of SAF, TSC and SSCB. But, this cost is justified, when the benefits are considered. The

proposed system can also be extended to multiple bus system.

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