A NEW PWM MODULATED MULTILEVEL INVERTER TOPOLOGY WITH REDUCED SWITCH COUNT IN CONDUCTION PATH

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Abstract: *Multilevel Inverters proved its predominance in high voltage and medium power applications especially drive and renewable applications. Multilevel inverters have the capability of spawning stepped voltage from series of capacitor banks or isolated voltage sources through clamping diodes or capacitors. However the multilevel inverters endure huge number of power components and become complexity in control with increase in higher number of levels. A novel three phase multilevel inverter is developed to overcome aforementioned problems. The architecture is constituted using several bidirectional devices, series of isolated dc sources and high frequency transformers. The proposed structure claims minimal usage of conducting switches and one third of isolated dc sources in comparison with CHBMLI. The feasibility of the proposed MLI is validated in symmetric configurations. The simulation and experimental results are shown to prove the effectiveness of the proposed topologies under both modes.*

Key words: *Multilevel inverter, symmetrical, reduced switch count, Power loss, PWM.*

1. Introduction

Multilevel inverters have been acknowledged for high power applications with major privileges to produce high quality and lower distortion of the output voltage and low blocking voltage of semiconductor compared to the classical voltage source inverter. The other area for effective utilization for multilevel inverters is the renewable photovoltaic energy systems [29]. The power quality can be improved with increasing the number of levels with small voltage steps, while it imposes significant expense due to circuit complexity, inability to realize modularization in the structure, failure management and implementation cost [1, 2, 3]. The first edition of multilevel inverter is Neutral point or diode clamped inverter introduced in 1981 [4] that utilize several split capacitor banks and clamping diodes. The application of this inverter is limited due to excessive use of clamping diodes with different voltage ratings. Later, the flying capacitor is designed to operate within dependent capacitors in order to clamp the device voltage to one capacitor voltage level and it requires a large number of bulk capacitors to clamp the voltage [5].

The Cascaded H-Bridge (CHB) inverter based on series connection of single-phase inverters with isolated dc sources. Each arm of the CHB produces output voltage with three steps following positive, negative and zero voltages. The output voltage of CHB is synthesized by summation of each H- bridge output voltage [6]. Several remarkable innovations have been paid in design of multilevel inverter topologies. The design has been focused to optimize the number of switches, gate drivers and isolated voltage sources, number of voltage levels, efficient control algorithm, power losses, device voltage stress and standing voltage on the switches and Total Harmonic Distortion (THD) for output voltage waveform. Several remarkable innovations have been proposed continuously by the researchers for the past decades.

A new symmetrical topology based on arrangement of dc sources with opposite polarities in laddered structure is developed in [7]. The working principle of the proposed topology is demonstrated with the help of a single-phase five-level inverter. The topology claims reduced power component requirements compared to classical inverter.

A new multilevel inverter is constituted in [8] which is a derived version of multilevel dc link inverter using half bridge cells. The topology utilizes split capacitors instead of isolated dc sources. The developed topologies lead unbalanced dc-link voltages and switching devices with higher blocking voltage in the polarity reversal side that requires large number of switching devices.

The new structures for symmetric, asymmetric and hybrid multilevel inverter are recommended in [9] which composed of a single dc sources in connection with an array of semi half bridge cells (dc source and a diode) configuration. The determination of magnitudes of voltage sources

using different algorithm are presented. The topology falls on non-regenerative converters and cannot be used for bidirectional power control operation.

A new topology for multilevel inverter is formulated using series connection of fundamental block [10]. The proposed topology is generalized using series connection of the fundamental blocks. The fundamental block is constituted using two series connected dc sources and two sets of four diodes with a single switch arrangement at the tie point on inner sides of an H-bridge inverter. The proposed multilevel inverter requires numerous clamping diodes for higher number of voltages levels.

A topology using half bridge cells connected in cross fashion for achieving reduced switch count is suggested in [11]. The topology is validated for nine and seventeen levels and supported with both simulation and experimental results. However, the topology suffers from more number of devices in conduction path.

A new topology of semi-cascaded multilevel inverter with a series of half bridge cells and H-bridge inverter is constituted in [12]. The developed topology is similar to [7] except series connection of half bridge cells. The major drawback of this topology is switching device with high blocking voltages at H-6 inverter is required when increasing the number of levels.

A topology based on series connection of dual voltage source module to H-bridge inverter is constructed in [13]. The synthesizing of stepped voltage waveform is achieved by appropriately switching the dual source module in crisscross fashion. The major drawback of this topology is to block high dc link voltages at the H-bridge inverter.

A novel transformer based cascaded multilevel inverter to extract multistep voltage waveform is presented in [14]. The suggested inverter can operate in both symmetric and asymmetric configurations and however bulkier transformers are required that added to its disadvantage.

A topology for cascaded multilevel inverter constituted using a module composed of H- and half bridges, two isolated equal dc sources and a bidirectional auxiliary circuit is suggested in [15]. The topology is designed in such a way that one leg of the H-bridge and the half-bridge are cut and the corresponding terminals are connected to the both ends of an equal split dc source, while the other ends of the half bridge are connected together to form a common output node of the inverter.

A multilevel voltage source inverter that has been designed from transistor clamped multilevel inverter and six switch inverter [16]. Some bidirectional switches in the proposed unit are made to function in the optimized mode in which their operations are divided among the three phases. The presence of the optimized mode considerably reduces the number of power switches while increasing the number of levels increases.

Several remarkable attempts have been recently addressed such as the topologies which utilize low-switching frequency and high-power devices [17]–[28].

In this paper, an attempt has been made to design a new three phase MLI structure for cascaded multilevel inverters with a higher number of steps associated with a low number of power switches and dc voltage sources. The proposed topology is desired to operate for five level in the phase voltage. The experimental results are included to validate the viability of the proposed topology.

2. Proposed Topology

The generalized three phase structure of the proposed topology is depicted in Fig.1 which is constituted using a series of electrically isolated dc sources or capacitor banks ($V_{dc1} - V_{dc(m-1/2)}$), switching devices ($S_{a1} - S_{a(m+1/2)}$, $S_{a1}' - S_{a(m+1/2)}$) and high frequency isolation transformer to synthesize staircase pole voltage waveform per phase. The switching devices used in the proposed topology are bidirectional one which can be available with several arrangements likely one IGBT with four diodes or two IGBTs along with body diode connected in common emitter configuration. In this work, bidirectional switch with common emitter configuration is used that requires single driver unit. The purpose of the bidirectional switch used in the proposed topology to block voltage and conducting current in both the directions while extending the basic unit. The basic unit shown in Fig.2 for each phase constituted using a single dc source with four bidirectional IGBTs which can produce three level output voltage and then applied across primary side of high frequency transformer. The secondary side of transformer in each phase is connected in star connection to synthesize stair case pole voltage waveform. To produce V_{dc} in the output voltage, the switches S_{a1} and S_{a2}' to be conducted and similarly the switches S_{a1}' and S_{a2} are conducted for negative level respectively. The basic unit can be extended in series to produce required number of levels.

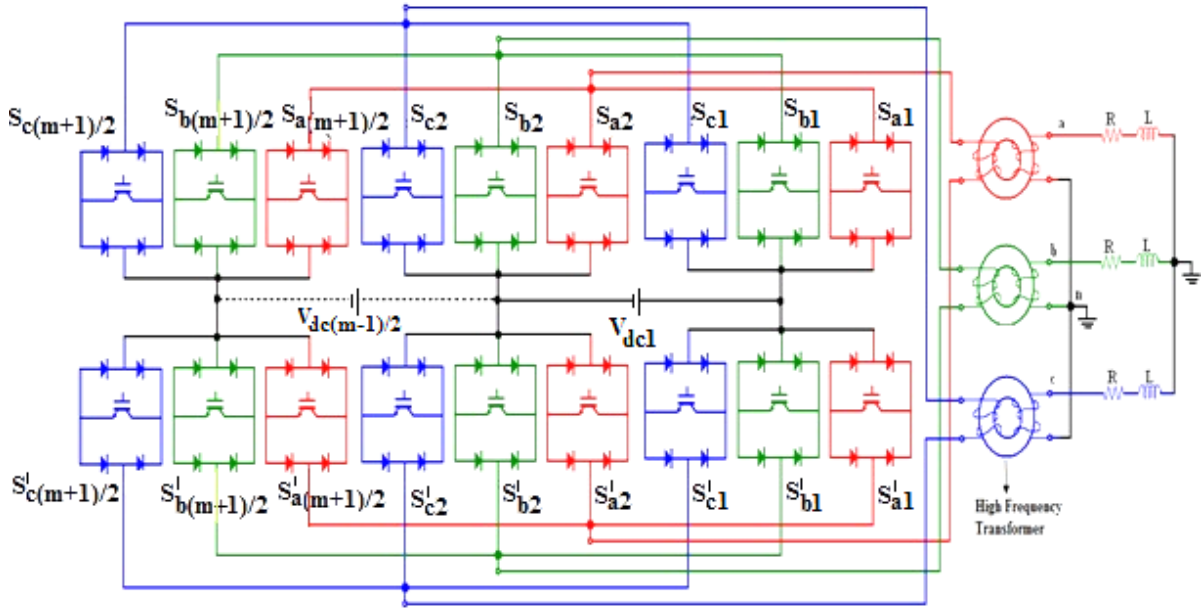

Fig. 1 Generalized structure of the proposed topology

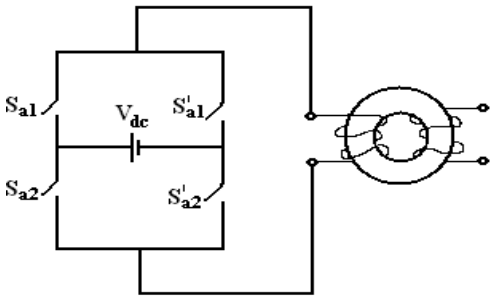

Fig. 2 Basic of bidirectional Switch with high frequency transformer

The entries in Table 1 tabulate switching sequence to extract various levels in five level inverter. For instance shown in Figs.3 the switches (S_{a2}' , S_{a3} , S_{a3}'), (S_{b1} , S_{b2} , S_{b3}') and (S_{c1}' , S_{c2}' , S_{c3}) to produce (V_{an} = V_{dc}, V_{bn}=-2V_{dc} and V_{cn} =2V_{dc}) . The main advantage of this topology is only three switching devices are in conduction path for different levels of output voltage for five level. The number of switches in the path of conducting current also plays an important role in the efficiency of overall inverter. For example, a seven-level CHBMLI has eight switches, and half of them, i.e., four switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from two switches (for generating level 0) to three switches conducting for other levels. Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the CHBMLI and hence it has a better efficiency. This topology requires isolated dc sources which do not have voltage balancing problems that add to its merit. Also in comparison with a cascaded H-bridge MLI (CHBMLI), it requires only one-third of isolated power supplies used in a CHBMLI. This topology requires fewer components in comparison to conventional inverters. The number of switches required to produce m level in the phase voltage is given by 6(n+1), where 'n' is the number of dc sources.

The multilevel inverter topologies avails various control strategies like multicarrier PWM, space vector modulation and fundamental switching methods to synthesize PWM modulated output voltage. For simplicity, in the proposed topology, the MCPWM method is employed to drive the switching pattern for each switch to attain variable output voltage. The proposed topology is reformed for five levels in the pole voltage which utilize only two carrier and three sinusoidal modulating signals. The proposed topology offers half the total number of carrier signals used in CHBMLI and minimum number of devices in the current path for same number of levels. The logical representation of pulse generation methodology is portrayed in Fig.4 and the pulse mapping for each switching device is tabulated in Table 2.

Table.1 Symmetrical Operating modes per cycle

Modes	Output Phase Voltages			Conducting Switches		
	V_{an}	V_{bn}	V_{cn}	V_{an}	V_{bn}	V_{cn}
1	0	$-2V_{dc}$	$2V_{dc}$	S_{a3} , S_{a3}'	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
2	V_{dc}	$-2V_{dc}$	$2V_{dc}$	S_{a2}' , S_{a3} , S_{a3}'	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
3	V_{dc}	$-2V_{dc}$	V_{dc}	S_{a2}' , S_{a3} , S_{a3}'	S_{b1} , S_{b2} , S_{b3}'	S_{c2}' , S_{c3} , S_{c3}'
4	$2V_{dc}$	$-2V_{dc}$	V_{dc}	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c2}' , S_{c3} , S_{c3}'
5	$2V_{dc}$	$-2V_{dc}$	0	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c3} , S_{c3}'
6	$2V_{dc}$	$-2V_{dc}$	$-V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b1} , S_{b2} , S_{b3}'	S_{c2} , S_{c3} , S_{c3}'
7	$2V_{dc}$	$-V_{dc}$	$-V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b2} , S_{b3} , S_{b3}'	S_{c2} , S_{c3} , S_{c3}'
8	$2V_{dc}$	$-V_{dc}$	$-2V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b2} , S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
9	$2V_{dc}$	0	$-2V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
10	$2V_{dc}$	V_{dc}	$-2V_{dc}$	S_{a1}' , S_{a2}' , S_{a3}	S_{b2}' , S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
11	V_{dc}	V_{dc}	$-2V_{dc}$	S_{a2}' , S_{a3} , S_{a3}'	S_{b2}' , S_{b3} , S_{b3}'	S_{c1} , S_{c2} , S_{c3}'
12	V_{dc}	$2V_{dc}$	$-2V_{dc}$	S_{a2}' , S_{a3} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
13	0	$2V_{dc}$	$-2V_{dc}$	S_{a3} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
14	$-V_{dc}$	$2V_{dc}$	$-2V_{dc}$	S_{a2} , S_{a3} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c1} , S_{c2} , S_{c3}'
15	$-V_{dc}$	$2V_{dc}$	$-V_{dc}$	S_{a2} , S_{a3} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c2} , S_{c3} , S_{c3}'
16	$-2V_{dc}$	$2V_{dc}$	$-V_{dc}$	S_{a1} , S_{a2} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c2} , S_{c3} , S_{c3}'
17	$-2V_{dc}$	$2V_{dc}$	0	S_{a1} , S_{a2} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c3} , S_{c3}'
18	$-2V_{dc}$	$2V_{dc}$	V_{dc}	S_{a1} , S_{a2} , S_{a3}'	S_{b1}' , S_{b2}' , S_{b3}	S_{c2}' , S_{c3} , S_{c3}'
19	$-2V_{dc}$	V_{dc}	V_{dc}	S_{a1} , S_{a2} , S_{a3}'	S_{b2}' , S_{b3} , S_{b3}'	S_{c2}' , S_{c3} , S_{c3}'
20	$-2V_{dc}$	V_{dc}	$2V_{dc}$	S_{a1} , S_{a2} , S_{a3}'	S_{b2}' , S_{b3} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
21	$-2V_{dc}$	0	$2V_{dc}$	S_{a1} , S_{a2} , S_{a3}'	S_{b3} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
22	$-2V_{dc}$	$-V_{dc}$	$2V_{dc}$	S_{a1} , S_{a2} , S_{a3}'	S_{b2} , S_{b3} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
23	$-V_{dc}$	$-V_{dc}$	$2V_{dc}$	S_{a2} , S_{a3} , S_{a3}'	S_{b2} , S_{b3} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}
24	$-V_{dc}$	$-2V_{dc}$	$2V_{dc}$	S_{a2} , S_{a3} , S_{a3}'	S_{b1} , S_{b2} , S_{b3}'	S_{c1}' , S_{c2}' , S_{c3}

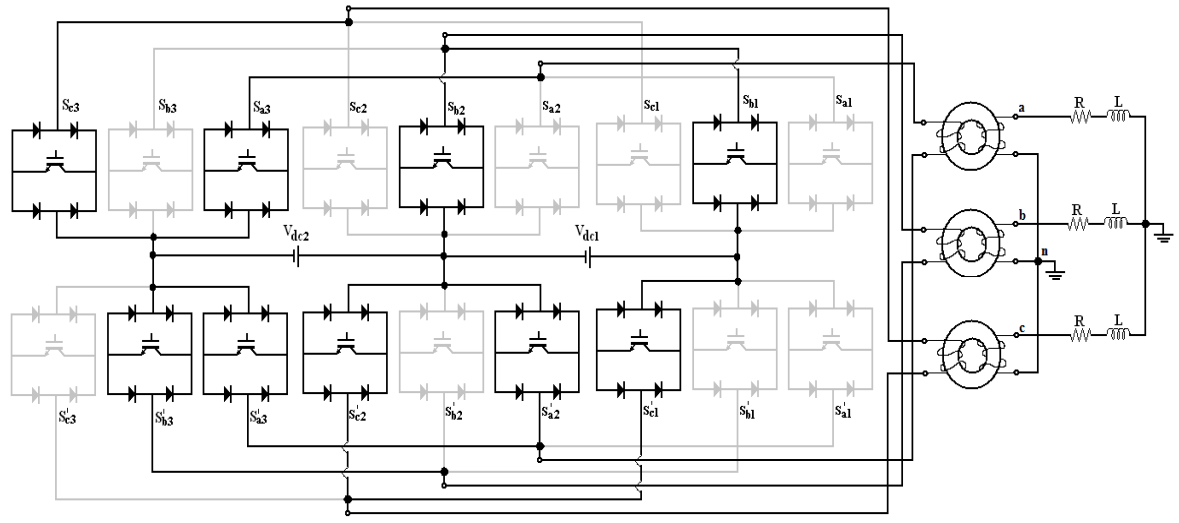

Fig. 3 Five level inverter with mode diagram for $V_{an} = V_{dc}$,$V_{bn} = -2V_{dc}$ and $V_{cn} = +2V_{dc}$

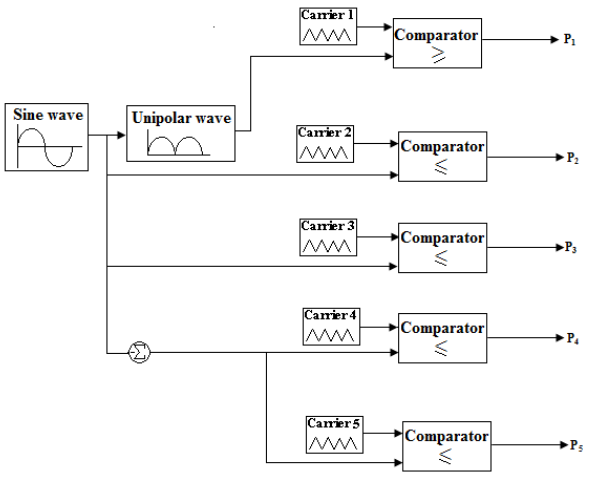

Fig. 4 Pulse generation methodology per phase

Table.2 Digital process of control signals

Switches	Control Signals
S_{a1}	P_5
S_{a1}'	P_3
S_{a2}	P_4 XOR P_5
S_{a2}'	P_2 XOR P_3
S_{a3}	P_3 OR (P_2 XOR P_3) OR P_1
S_{a3}'	P_5 OR (P_4 XOR P_5) OR P_1

The Figs. 5 and 6 portray plot between switch count, dc sources and the number of voltage levels for symmetric topologies. It is inferred from the Fig.5, the proposed structure avails lower number of switches for a particular number of voltage levels in comparison with CHBMLI and the topology cited in [17, 18, 19]. For instance in seven level inverter, the proposed topology uses 8 switches while the CHBMLI topology and the topologies cited in [17, 18, 19] use 10 switches per phase respectively. The H-Bridge topologies depicted in [17, 18] require switches with high standing voltage which is equal to rated output voltage of the inverter. This factor decides the important merit that aims to distribute the operating voltage among the switches so that low-voltage switches can be used to synthesize a high voltage output in multilevel inverter. The proposed topology offers low standing voltage switches to synthesize the stepped voltage while increasing the higher number of levels compared to other topologies. Therefore both number of switches and their voltage ratings are considered very important factors in MLI technology. The other specific advantage in the proposed topology is the number of dc sources required to synthesize various output level is one third of total source count compared to CHBMLI and other topologies as illustrated in Fig. 6. The efficiency of the MLI topology depends on the number of devices in the conduction path. The proposed topology utilize only two devices in the current path for any level of output voltage, therefore the proposed topology offers better efficiency.

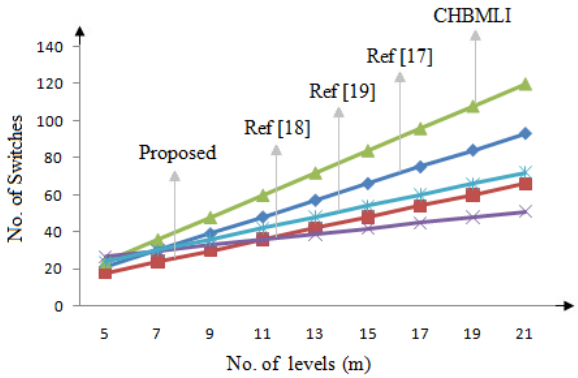

Fig. 5 Comparison of switch count against voltage levels

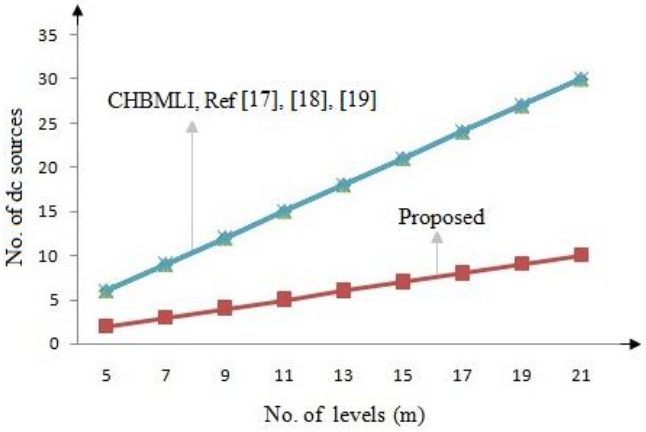

Fig. 6 Comparison of dc sources required against voltage levels

The switching loss of the proposed topology is computed by considering the energy lost during turn-on and turn-off interval of a switch. To simply the analysis, it is assumed that the voltage and current of a switch during switching varies linearly. Using this approximation, the energy lost during every turn-on and turn-off period of a switch can be obtained as

$$E_{on} = \int_0^{t_{on}} v(t)i(t)dt$$

$$= \int_0^{t_{on}} \left[\left(\frac{V_{sw}t}{t_{on}}\right)\left(-\frac{I}{t_{on}}(t - t_{on})\right)\right] dt$$

$$= \frac{1}{6} V_{sw} I t_{on}$$

$$E_{toff} = \int_0^{t_{off}} v(t)i(t)dt$$

$$= \int_0^{t_{off}} \left[\left(\frac{V_{sw} t}{t_{off}} \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt$$

$$= \frac{1}{6} V_{sw} I t_{off}$$

where E_{on} and E_{off} are the lost energy during turn-on and turn-off period of a switch and ton and t_{off} are the turn-on and turn-off time of the switch. V_{sw} and I are voltage on and current through the switch before turning on or after turning off. For the multilevel inverter, the switching power loss can be computed as follows

$$P_{sw} = \frac{1}{T} (N_{on} E_{on} + N_{off} E_{off})$$

Where T is a fundamental cycle and (N_{on} and N_{off}) is the number of times that the switches are turned on and off respectively. The total power loss of the switches can be obtained by adding the conduction and switching losses as shown in Fig. 7. The proposed topology offers lesser power loss in each switching devices compared to other topologies.

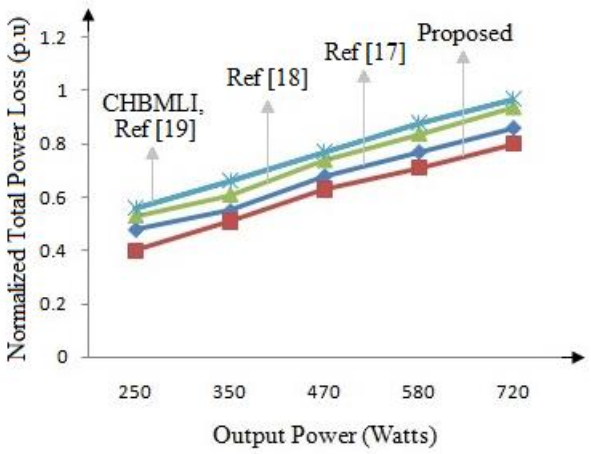

Fig. 7 Comparison of total power loss against output power

3. Simulation Results

The functionality of the proposed topology is simulated for five level output in Matlab R2013b with simulation specifications: V_{dc1}= V_{dc2}= 100V, switching frequency of 2 kHz and a RL load of 150Ω and 106mH respectively. The three phase voltage waveform with V_{AN}, V_{BN} and V_{CN} are shown in a single trace as Fig.8. The corresponding line voltage waveform with V_{AB}, V_{BC} and V_{CA} along with phase current waveform and phase and line voltage spectrum are portrayed in Figs.9, 10, 11 and 12 respectively.

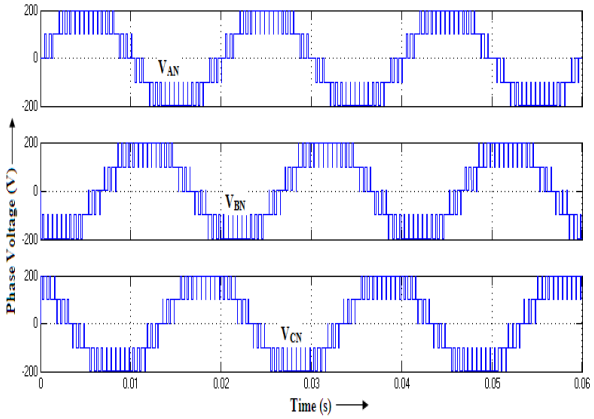

Fig. 8 Phase voltage waveform

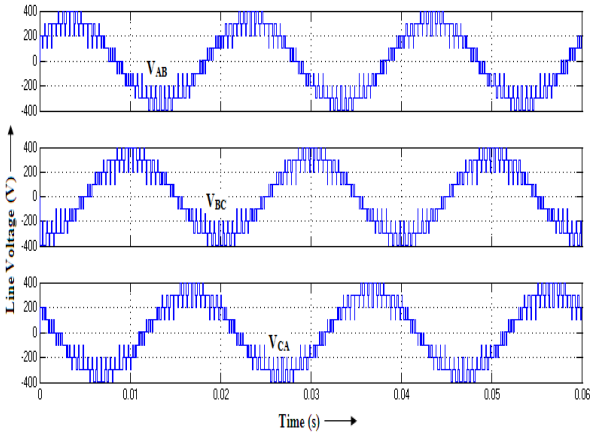

Fig.9 Line voltage waveform

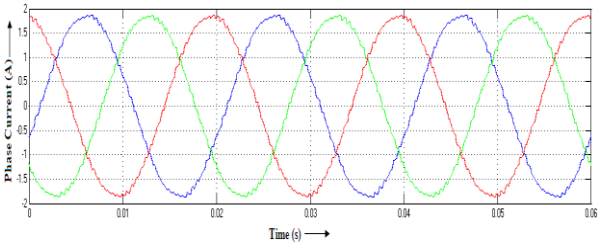

Fig. 10 Phase current waveform

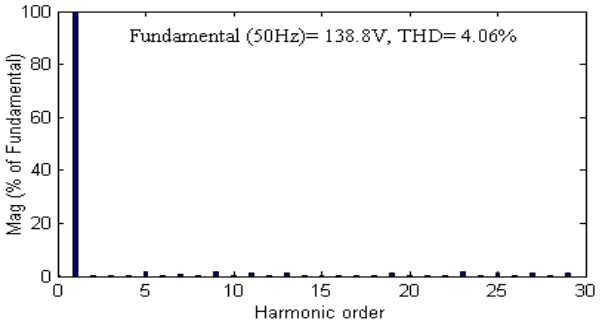

Fig. 11 Harmonic phase voltage spectrum

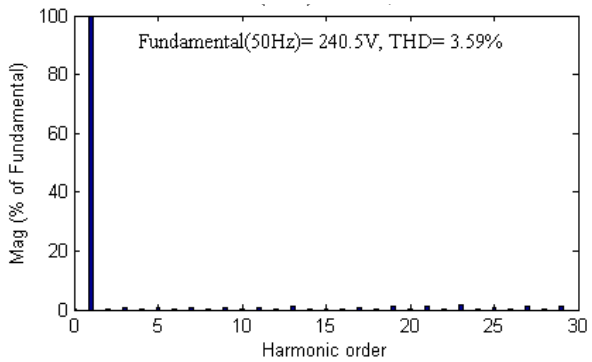

Fig. 12. Harmonic line voltage spectrum

4. Experimental Results

A hardware setup for the proposed inverter is developed for the similar specification as those used in simulation is shown in Fig.13. The gating pulses used to buffer the power switches to extract various levels of output voltage are generated in Spartan 3E-500 FG320 Xilinx FPGA processor using look up algorithm (LUTs) and captured through Agilent scope is shown in Fig.14. The bidirectional IGBT FIO 50-12BD is used for the proposed inverter with voltage and current rating of 1200 V and 50A respectively. The inverter is used to produce five levels in the phase and nine levels in the line voltage along with phase current waveform and harmonic spectrum are captured Yokogawa power scope depicted in Figs. 15, 16, 17, 18 and 19 respectively. From the hardware results, the inverter is capable of synthesizing desired voltage levels and justifies the simulation response.

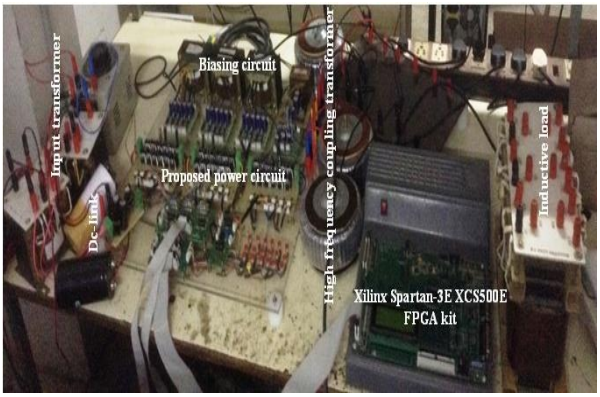

Fig. 13 Experimental prototype

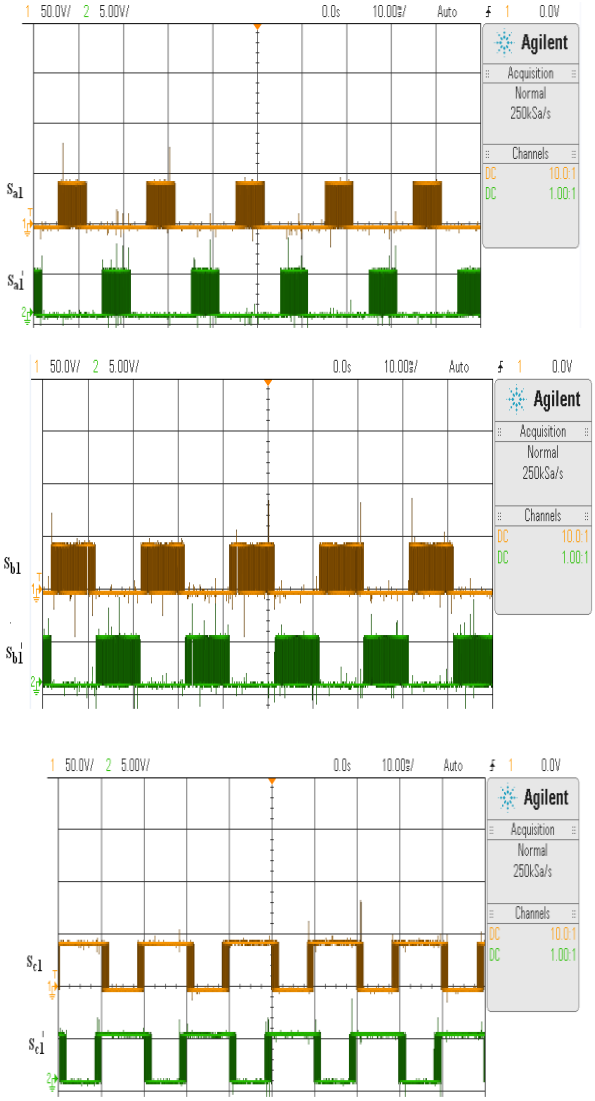

Fig. 14. Pulse pattern for per phase

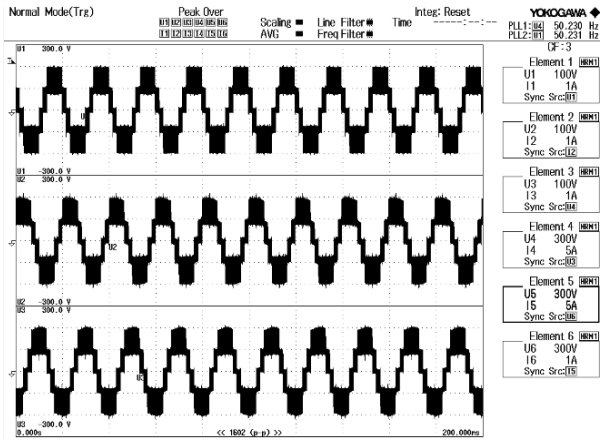

Fig. 15. Phase voltage waveforms

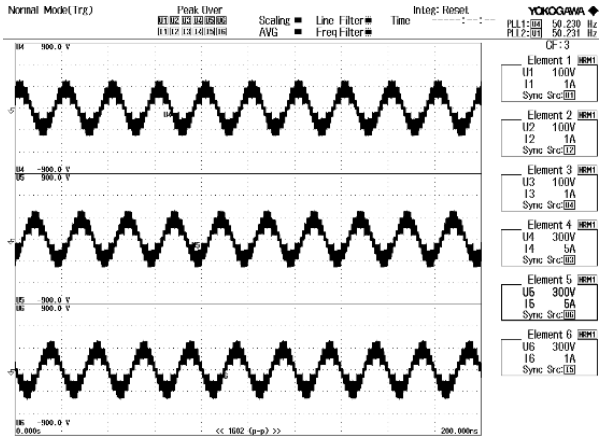

Fig. 16 Line voltage waveforms

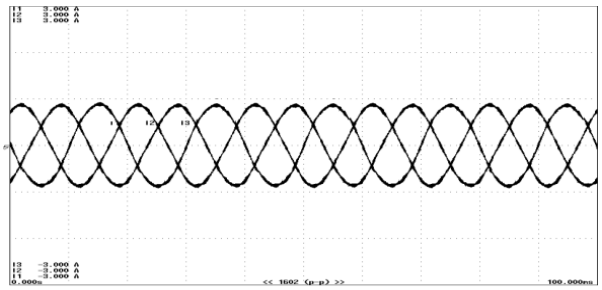

Fig. 17 Phase current waveform

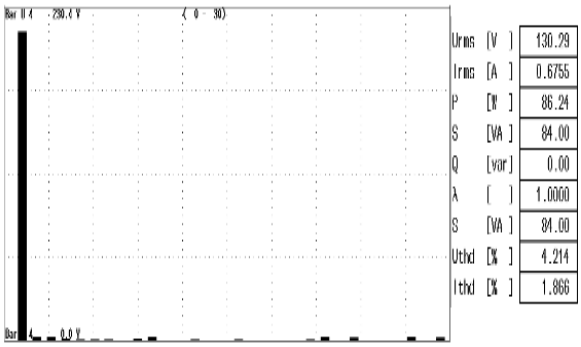

Fig. 18 Phase voltage harmonic spectrum

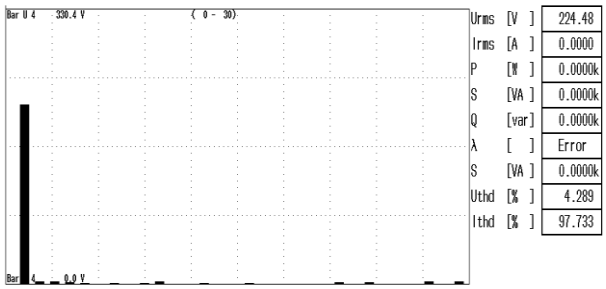

Fig. 19 Line voltage harmonic spectrum

5. Conclusion

A new three phase multilevel inverter topology is introduced with perspective of developing reduced component topologies for higher power drive applications. The proposed topology has given a lead to operate in asymmetrical configuration to meet enrichment for further innovation in MLI family. The proposed topology gleams its independency in terms of reduced number of switches, isolated dc sources and constant switches in the conduction path compared to recent topologies. The simulation and experimental results are carved out for five level that proves its viability in producing nearly sinusoidal output voltage.

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