INVESTIGATIONS ON EMBEDDED PROCESSOR ARCHITECTURES FOR THE SPEED CONTROL OF SWITCHED RELUCTANCE MOTOR DRIVE

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Abstract: *This paper examines the features of various digital processors for implementing an intelligent speed control algorithm for switched reluctance motor (SRM) drive. The Hybrid Self Tuned Fuzzy Logic -Proportional and Integral (HSTF-PI) control algorithm is used for the implementation of the speed controller in different processor architecture. The embedded architecture considered for the analysis is Digital Signal Processor (DSP) (fixed and floating point), Field Programmable Gated Array (FPGA) and Advanced Reduces Instruction Set Computing (RISC) Machine (ARM) architectures. The processors are compared in terms of type of architecture, code generation technique, and speed and memory utilization for realizing the algorithm. The experimental results indicates that the merits of the advanced architecture.*

Key words: *SRM, Fuzzy control, Embedded processors, Speed control.*

1. Introduction.

The application of embedded motor speed control covers a wide range from simple home automation to missile control. This emphasizes the role of embedded processors in the motor speed control system. Many of the motor control applications are hard real time systems which work on critical deadlines. This paper explores the application of various embedded processors for implementation of HSTF-PI algorithm as the performance of the algorithm depends on the choice of the processor.

Simple microcontrollers are major players in the field of embedded system design as they need low power at a low cost. Micro computer based four quadrant control of SRM has been implemented by Bose et al.,[1] using Intel 8751 and AM9513. However these controllers have lesser memory space, not capable of holding highly sophisticated algorithms [2].

A digital controller for SRM drive based on DSP, with internal Controlled Area Network (CAN) interface TMS320F2406 and Complex Programmable Logic Device (CPLD) EPM7128S has been proposed and tested for a battery operated vehicle application [3]. Neural network and Fuzzy based rotor position estimation techniques has been presented by [4] and verified in real time with DSP - TMS320F2812 processor. Neural network based sensorless speed control of two phase SRM drive [5] has been implemented using DSP-TMS320LF2407A. A digital controller for precise control and four quadrant operations of BLDC motor have been proposed and developed with dsPIC30F4011[6]. It combines the computation capability of DSP and controllability of Peripheral Interface Controller (PIC).

The conventional DSP processors come with the higher operating speed to meet the real time constraints of the systems. At the other side, these DSP consumes more power. To compensate on these limitations [7] currently, application specific DSP processors has been evolved. Texas instruments releases the family of C2000 series of DSP processors (www.ti.com) for motor control in automotive applications.

The other category of embedded processor is FPGA, which has significant features like re-configurability, high speed with parallel computations and flexible hardware design. An improved current feedback loop for SRM drive has been proposed [8]

and implemented in Xilinx XC3195A FPGA which performs well with reduced switching losses and increased drive efficiency. The challenge is to design an independent architecture specific to the control algorithm.

In recent years, there have been wider applications of ARM controller for embedded system applications [9]. This faster evolution of the processor happens because of its architectural enrichment, mainly of its multistage pipelining.

The analysis of literature reveals the possibility of doing digital implementation using processors like microcontrollers, DSP, FPGA and ARM. The implications of the intelligent speed control algorithm put forth the requirement of the embedded processors with high speed and larger onboard memory. With the wide range of choices in the usage of embedded processors for speed control applications, this research focuses on the comparison of three prominent processors, each from a different group. First, from the family DSP, a fixed point and a floating point processor from the Texas Instruments (TI) are taken up for the analysis. ARM, Cortex –M4 series has been considered under the category of currently evolving embedded processors. Finally, this research also explores a self-designed architecture for the optimized implementation of the proposed technique using reconfigurable FPGA. This research presents a brief discussion on the significant features of the processors and assesses their relative merits with respect to the implementation of the HSTF-PI control algorithm.

This paper is organised as follows section 2 explains the HSTF-PI speed control algorithm of SRM. Section 3 overviews and compares the different embedded processors architectures. Comparison of the implementation of HSTF-PI control algorithm is presented in section 4. In section 5, the experimental results and the discussion about the same is presented. Finally the proposed research is concluded in section 6.

2. Design of closed loop HSTF-PI speed control algorithm

The general control structure for SRM drive [10] is shown in Fig 1. The cascade control system for SRM drive consists of a hysteresis current controller in the inner loop, and a PI speed controller in the outer loop. As the parameters of the inner current loop and outer speed loop are affected with the change in the operating conditions, an adaptable fuzzy logic controller is implemented to improve the performance.

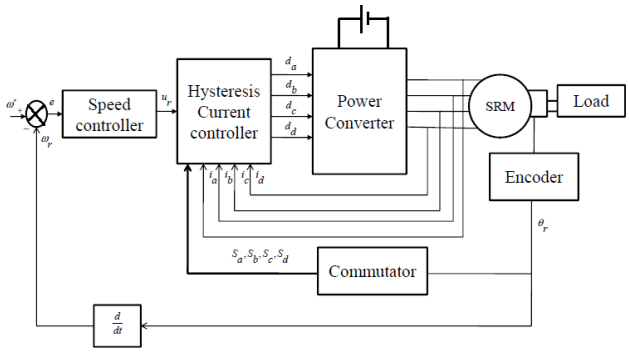


Fig. 1. Closed loop control system of SRM drive

The scaling factor tuning method has a significant impact on parameter variations [11] and hence it is explored in this proposed research. The block diagram for self tuned controller is shown in Fig 2.

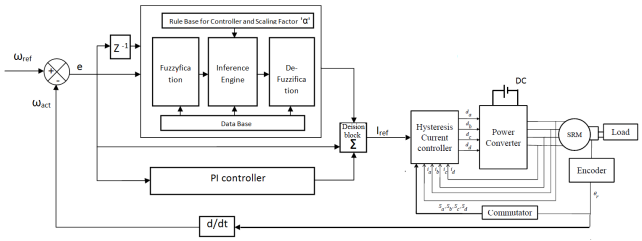


Fig. 2. HSTF-PI based speed controller

It includes one more rule base for the gain updating or scaling factor 'α' called Fuzzy Tuner [12], in addition to a conventional FLC. This fuzzy tuner adjusts the scaling factor in such a way, that the domain of the input and output variables are varied, so as to have faster settling time and fewer oscillations around the preset speed. The switching function Σ will decide based on the speed error of controller in action.

This HSTF-PI controller has a merit of combining the robustness of PI controller at steady state and the adaptability of the Self Tuning Fuzzy Logic-PI (STF-PI) Controller during transient state, for SRM speed control [13,14]. The flowchart of the proposed HSTF-PI controller is shown in Fig 3.

The hybrid controller consists of a simple comparator, in which a switching mechanism is employed, to change the control action from conventional PI controller to STF-PI controller, based on the speed error value.

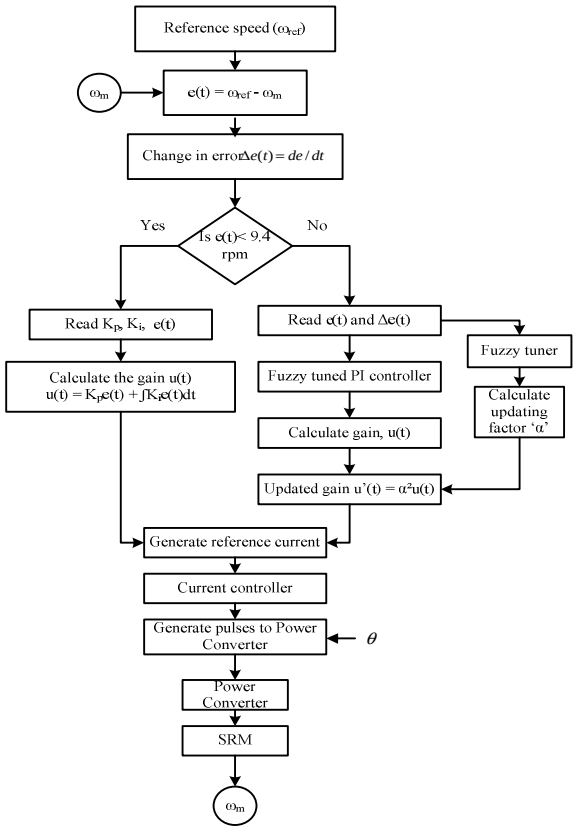


Fig. 3. Flowchart of Hybrid ST fuzzy PI speed control algorithm

The PI-controller is effective during steady state to reduce the steady state error of the system. When the absolute speed error is greater than 9.4 RPM, STF-PI takes over the control action, to get fast response and low overshoot, during transient state. Therefore the threshold value is set at 9.4 RPM.

3. Choice of Embedded Processors for speed control of SRM drive

TMS320F2812 is one of the high performances static CMOS technology based DSP from Texas instruments. The vital features of this processor form the support for atomic operations; fast interrupt response, processing time and unified memory programming model.

The significant feature of this processor related to the implementation of the speed control algorithm is the EVent Manager (EVM) module, which includes general purpose timers, capture unit, PWM units and Quadrature Encoder Pulse (QEP) unit. The General-purpose timers can be operated independently or synchronized with each other. The associated compare register can be used for comparison function and PWM-waveform generation. Each EVM can generate up to eight PWM waveforms simultaneously and also supports Double Update PWM mode, in which the position of the leading edge and the position of the trailing edge of a PWM pulse are modifiable independently. This EVM facilitates the embedded control drive of the two three-phase motor or four two-phase motor.

TMS320F28335 is a floating point processor with high performance static CMOS technology. The CPU supports 32-bit processing with 16x16 and 32x32 MAC operations, Harvard bus architecture, fast interrupt response and processing, and unified programming model. The processor has an enhanced control peripheral which includes 18 PWM output, 6 High Resolution PWM (HRPWM) outputs, event capture inputs, quadrature encoder interfaces and 32/16-bit timers. The enhanced PWM peripheral module supports independent and complementary PWM generation, and adjustable dead-band generation for leading and trailing edges. The High Performance PWM (HPPWM) module outperforms the conventionally derived digital PWM methods. This module extends the time resolution capability with the lowest of 9 or 10 bits, generating PWM frequencies greater than approximately 200 KHz, when using a CPU clock of 100 MHz. This module also supports finer time granularity control or edge positioning control. The ADC module consists of a built-in sample-and-hold circuit with a fast conversion rate of up to 80ns at 25-MHz clock. The module has the capability of auto sequence a series of conversion, to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results. Most importantly, the development support of the processor comes with the Digital Motor Control and Digital Power software packages.

ARM Cortex M4 is a 32-bit RISC core processor with floating point unit and adaptive real-time accelerator. It offers significant benefits like efficient processor core, ultra-low power consumption, with integrated sleep mode, platform security robustness and with optional integrated Memory Protection Unit (MPU). The significant feature of the ARM is the twelve 16-bit and two 32-bit timers with PWM, pulse counter and quadrature encoder input. Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture; making it suitable for evolving embedded applications. The processor includes high-end processing hardware, IEEE754 compliant single-precision floating point

computation, a range of single-cycle and SIMD multiplication, saturation arithmetic and dedicated hardware division.

The processor also features exceptional code-efficiency delivering the expected high performance. It also supports a set of DSP instructions which allow efficient signal processing and execution of complex algorithms. Its single precision Floating Point Unit (FPU) speeds up software development by using meta language development tools, while avoiding saturation. The differentiated bus architecture of ARM has Multi-ARM High speed Bus (AHB) which provides efficient operation when several high-speed peripheral are operated simultaneously. The advanced-control timers can be configured as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. Two PWM modules, with a total of 16 advanced PWM outputs for motion and energy applications. The modules also include eight fault inputs to promote low-latency shutdown and two Quadrature Encoder Inputs (QEI).

Artix-7 FPGA is an optimized architecture for high performance logic, and offers a higher capacity and hardware resources. For purpose of highlighting the architecture includes 15,850 logic slices, each with four 6-input Look Up Tables (LUTs) and 8 flip-flops, 4,860Kbits of fast block RAM, six clock management tiles, each with phase-locked loop, 240 DSP slices, Internal clock speeds exceeding 450MHz and an on-board analog-to-digital converter (XADC). A typical asynchronous SRAM with read and write cycle times of 70ns or as a synchronous memory with a 104MHz bus. The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1MSPS. The auxiliary analog input pairs connected via Dynamic Reconfiguration Port (DRP).

Pulse Density Modulation (PDM) module has two channels, with the possible signal generation in the range of 1MHz to 3 MHz. The analog to digital conversion module operates on the basis of the Delta sigma modulation technique. A PWM signal is a chain of pulses of fixed frequency, with each pulse potentially having a different width. The pulses are high for an average of 10% of the available pulse period, later an integrator produces an analog voltage, which is 10% of the Vdd voltage. The fidelity of the PWM signal is higher for the higher PWM signal frequency generation.

4. Implementation of HSTF-PI control algorithm

The major blocks involved in the realization of the HSTF-PI algorithm using MATLAB have been presented in the following Fig 4. This includes an additional rule base for scaling factor. Based on the speed error the embedded MATLAB function block decides the controller in action.

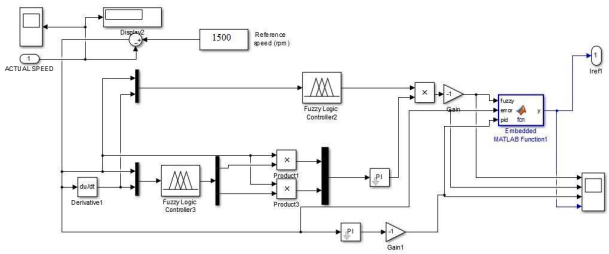
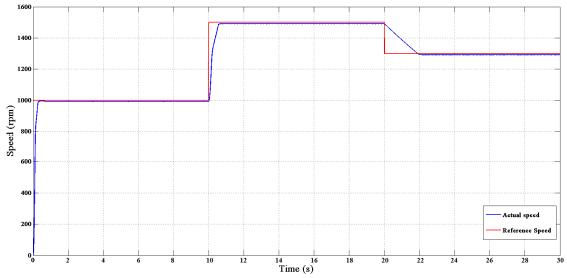
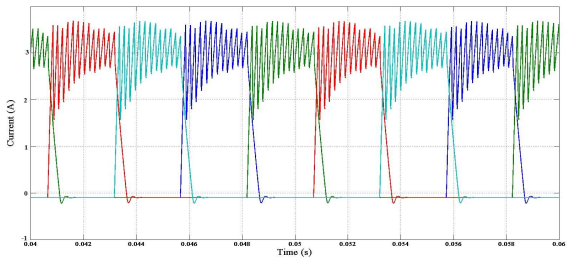


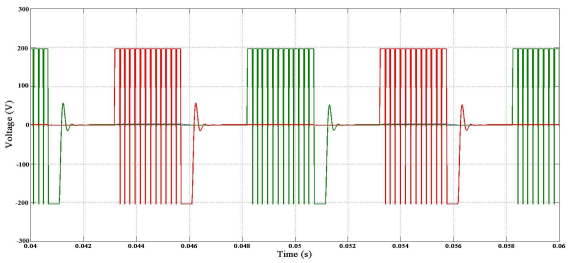
Fig. 4. MAT LAB -Simulink Block diagram of Hybrid Self -Tuned Fuzzy PI controller



(i)



(a)



(b)

(ii)

Fig. 5. (i) Speed response with different reference speeds (ii) Simulated (a) Current and (b) Phase Voltage with HSTF-PI speed controller

The simulation result shown in fig 5(i) depicts the inline performance of the proposed HSTF-PI controller with the change in speed. In fig 5(ii) the current and voltage response at the speed of 1500rpm and rated load is shown.

HSTF-PI algorithm has been realized in terms of set of script files and simulink model files in MATLAB, for its functional verfication. At the initial stage, the code density associated with the complete realization of the different modules of the algorithm is analyzed.

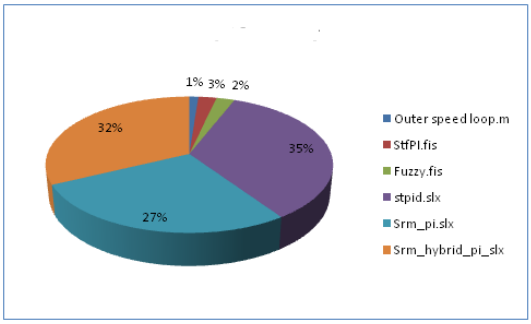


Fig. 6. Percentage of code space for each module

Fig 6 interprets the various percentages of memory space for each module of the proposed algorithm. The decision making modules of the algorithm makes a substantial contribution towards the functional execution of the proposed algorithm. Hence, more significantly, a detailed analysis of the decision blocks is presented as in Fig 7.

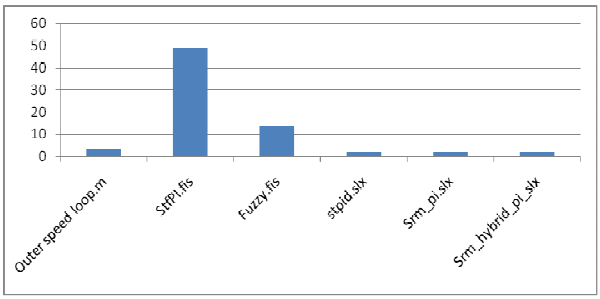


Fig. 7. Analysis of decision blocks

In the next phase, the functionally verified modules are targeted to the different processor including its supporting header files. The designed MATLAB files are fused into the different processors using different programming approaches. The integrated modules have been synthesized towards the processor using different softwares like, code composer studio for DSP processor, embedded coder for ARM, and system generator for FPGA.

The corresponding coder tool generates the c or bit map file, which could be compiled and fused in the processor. Table 1 lists the integrated code density for different processors. The nominal level of coding effeciency the table shows the variations in the code density involved in each processor. The different size of code density shows the different volume of header files for the processors

Table 1
Comparison of Code Density

Processor	Code Density (KB)
TMS320F2812	232
TMS320F28335	208
ARM Cortex – M4	238
Nexys-4 FPGA	202

This variation is infered in terms of supporting header files with respect to each processor.

5. Experimental results and Discussions

The experimental setup to validate system simulation model of SRM is shown in Fig 8, which consists of the following units.

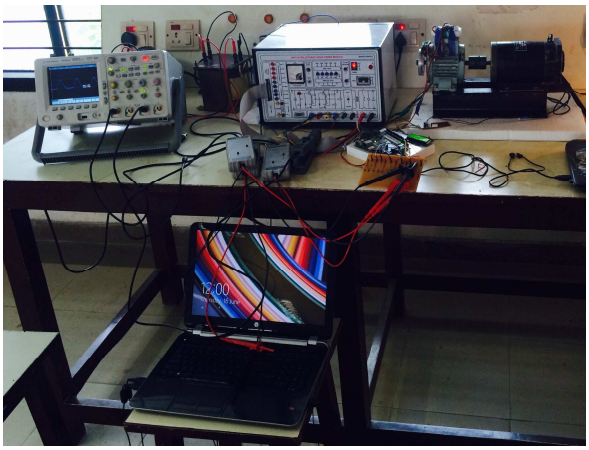


Fig. 8. Experimental Setup

- A four phase 8/6 pole SRM with the dimensions as given in appendix.
- A split DC supply converter
- Digital Storage Oscilloscope (DSO) with corresponding probes

The generated bitmap file for the proposed HSTF-

PI controller is fused in to the embedded controllers using the appropriate programming methods, with respect to each embedded processor. The performance of the speed control algorithm over the different embedded processor are evaluated with the complete hardware realisation. With the initial reference speed as 1500 rpm,the step response of the SRM is observed and plotted as shown in Fig 9.

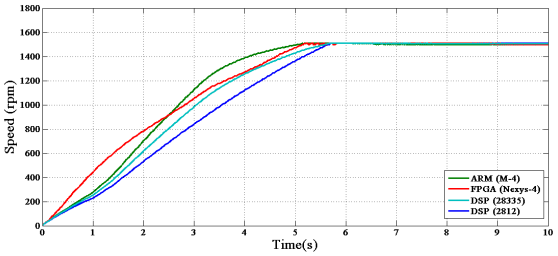


Fig. 9. Step response of SRM drive with different embedded controller

It could be observed that the settling time of the SRM drive with reference speed, is comparatively lesser for ARM M-4 controller. The speed response of SRM drive with the change in the reference speed from 1500 rpm to 2000rpm is shown in Fig 10.

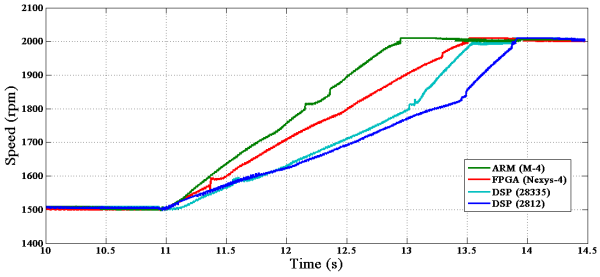


Fig. 10. Change in speed of SRM drive with different embedded controller

The above understanding from the performance of the ARM controller prevails the same even with the change in speed. The corresponding current and voltage waveform for the speed of 1500 RPM from the DSO is shown Fig 11.

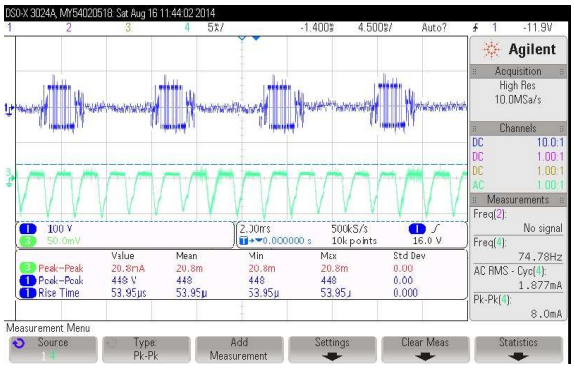


Fig. 11. Current and voltage waveform for the speed of 1500 RPM

The close correlation between the simulated and experimental results validates the proposed control algorithm.

6. Conclusion

The hardware implementation of the HSTF-PI speed control algorithm has been done with the choice of four different embedded processors. The vital features of the embedded processor which putforth the efficient implementation have been analyzed. The issues related to the experimental setup have been addressed and mitigated with the modified system components. The performance analysis of the proposed speed control algorithm over different embedded processor are evaluated in terms of code density, step response and change in speed. ARM Cortex M-4 based system have been seen as providing comparatively fast response with the effectiveness of its three-stage pipelined architecture. The research suggests theARM M-4 processor as a suitable choice in the implementation of hard real time strigent motor control applications.

Acknowledgement

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Appendix

Specifications of SRM

Design Parameters	Value
Stator diameter D0	90 mm
Bore diameter D	48 mm
Stack length L	40 mm
Air gap length g	0.5 mm
Stator back iron thickness C	11.25 mm
Stator pole arc β_s	21 degrees
Rotor pole arc β_r	24 degrees
Shaft diameter D_{sh}	8.5 mm
Height of stator pole h_s	9.25 mm
Height of rotor pole h_r	9 mm
Turns Per Phase	316
Current	4.5 A

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